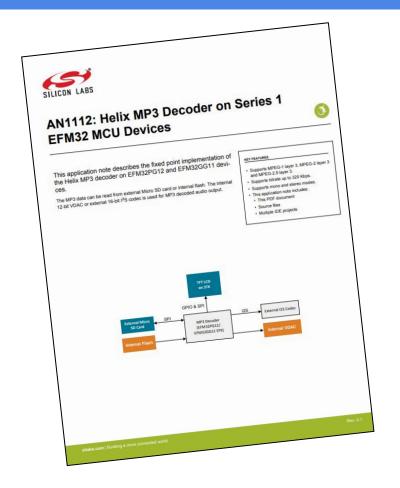
TP Final Protocolos CESE 6Co2018

Reproductor de MP3 con EduCIAA

Telmo Moya Grondona



Helix MP3 Decoder



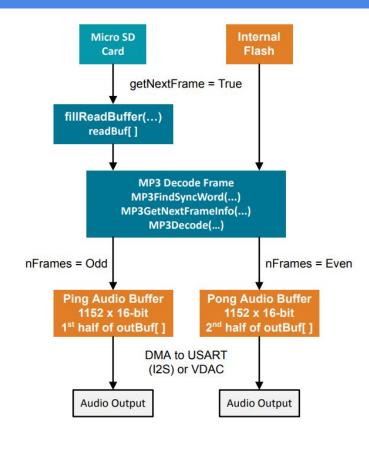
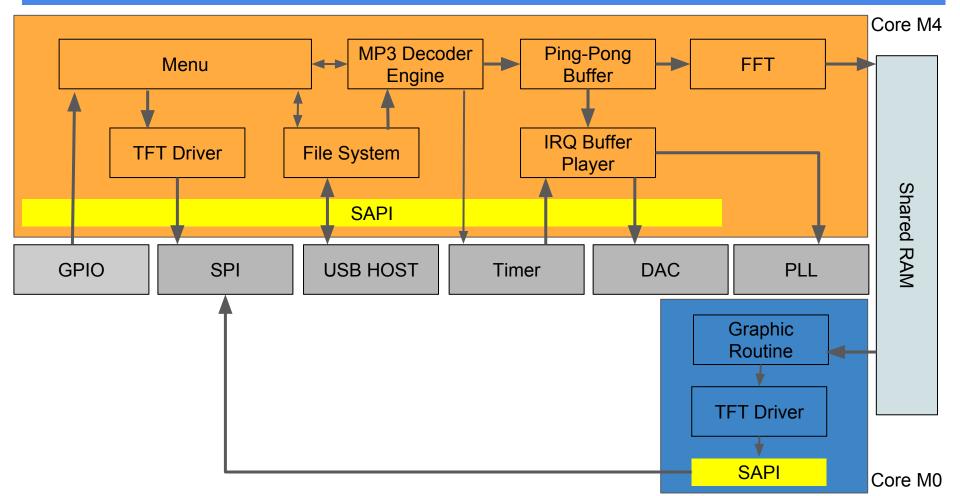
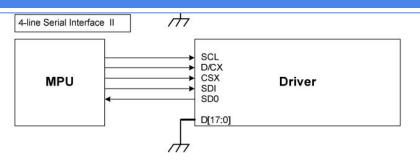


Figure 3.1. Block Diagram of Program Flow

Diagrama Bloques Reproductor MP3 EduCIAA Dual Core

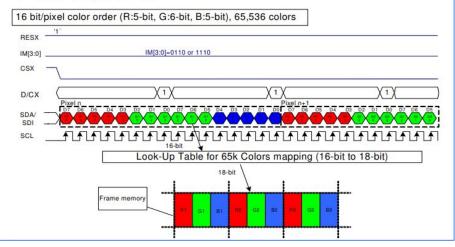


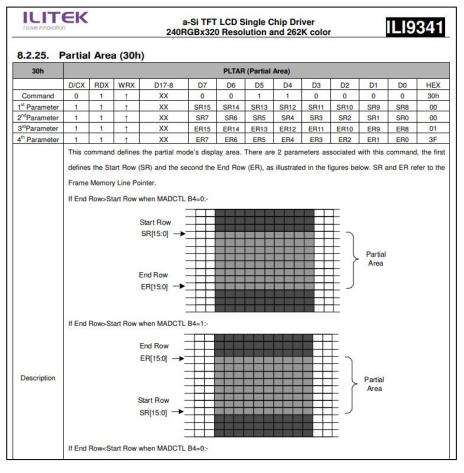
TFT LCD 240x320 Resolution, 262K colors



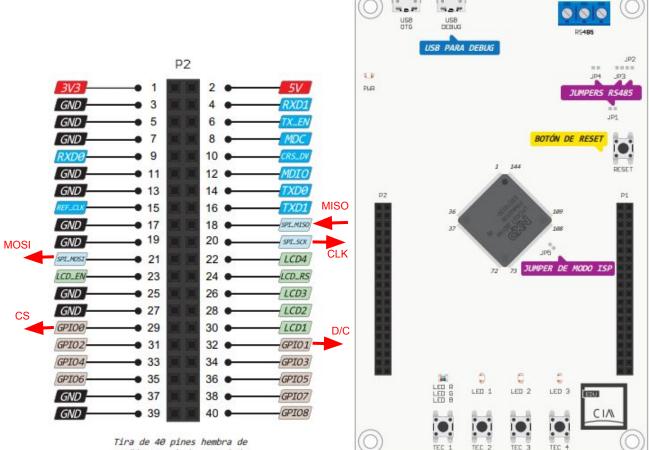
In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

- -65k colors, RGB 5, 6, 5 -bits input.
- -262k colors, RGB 6, 6, 6 -bits input.

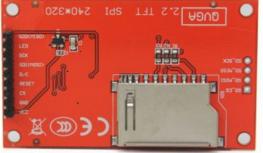




CONEXIÓN EDUCIAA - ILI9341

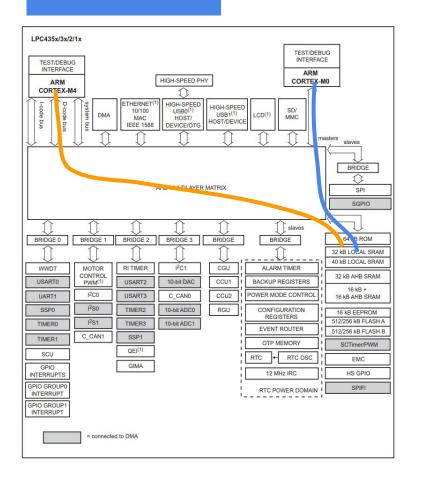






0.1"(2,54 mm) de espaciado

LPC 4337 RAM



32 kB LOCAL SRAM

40 kB LOCAL SRAM

32 kB AHB SRAM

16 kB + 16 kB AHB SRAM

16 kB EEPROM

512/256 kB FLASH A

512/256 kB FLASH B

Structs Secciones RAM EduCIAA

memory.h

```
32 kB LOCAL SRAM
40 kB LOCAL SRAM
 32 kB AHB SRAM
     16 kB +
 16 kB AHB SRAM
```

```
struct Loc32 {};
struct Loc40 {
     float32 t Input [SAMPLES];
     float32 t Output [SAMPLES/2];
     float32 t FFTOutput [SAMPLES/4];
struct AHB32{
     struct ipc sipc;
struct AHB16 {
     short outBuf0[2*DECODEBUF SIZE];
     short outBuf1[2*DECODEBUF SIZE];
struct AHB ETB16{};
```

IPC Struct

```
struct Loc32 {};
struct Loc40 {
     float32 t Input [SAMPLES];
     float32 t Output [SAMPLES/2];
     float32 t FFTOutput[SAMPLES/4];
};
struct AHB32{
     struct ipc sipc;
};
struct AHB16 {
     short outBuf0[2*DECODEBUF SIZE];
     short outBuf1[2*DECODEBUF SIZE];
};
struct AHB_ETB16{};
```

memory.h



main_m4.c

```
main_m0.c
```

```
// Play until end of file
 gpioWrite( LED3, ON );
        Enable DAC = 1;
        ipc->stop graph = 0;
                                // inicia dibujo en m0
do
        MP3Play Frame();
        static int skip = 0;
        if (++skip == 3)
                ipc->fft writting = 1;
                fft();
                ipc->fft_writting = 0;
                skip=0;
        Revisar teclas();
  if (tecla>1) break;
  } while (outOfData == 0);
```

```
while (1)
       while (ipc->stop graph == 1);
                                             // Dibuja el espectro si se lo permite M4
       /* Set cursor position */
       TM_ILI9341_SetCursorPosition(X0, Y0, X0+ANCHO-1, Y0+ALTO-1);
       /* Set command for GRAM data */
       TM_ILI9341_SendCommand(0x2C);
       Board SSP config(16,SSP_CLOCK_CPHA0_CPOL0,40000000);
       while (1)
               while(ipc->fft writting == 1);
                                             // Espero si se está calculando la fft
               int x,y;
               uint16_t color;
```

```
void TIMER0_IRQHandler(){
                                                                                                                                                       timer.c
         int32_t tmp;
         if (Chip_TIMER_MatchPending(LPC_TIMER0, 0))
                  static uint16_t indice = 0;
                  if (Enable_DAC)
                            if (indice >= mp3FrameInfo.outputSamps)
                                     tmp = outBuf0[indice-mp3FrameInfo.outputSamps]+32767;
                                     if (mp3FrameInfo.nChans == 2)
                                                                                                                          // Si es estereo promedio las muestras
                                               tmp = (tmp + outBuf0[++indice-mp3FrameInfo.outputSamps]+32767)/2;
                            else
                                     tmp = outBuf1[indice]+32767;
                                     if (mp3FrameInfo.nChans == 2)
                                                                                                                          // Si es estereo promedio las muestras
                                               tmp = (tmp + outBuf1[++indice]+32767)/2;
                            Chip_DAC_UpdateValue(LPC_DAC,(tmp>>6)/2);
                                                                                                                          // Mitad para no saturar line-in
                            FM_Play (tmp>>9);
                            indice++;
                            if (indice == mp3FrameInfo.outputSamps*2)
                                     indice=0;
                                     getNextFrame = true;
                            if (indice == mp3FrameInfo.outputSamps)
                                     getNextFrame = true;
                  else indice = 0;
                  Chip_TIMER_ClearMatch(LPC_TIMER0, 0);
```

FFT en Core M4 (FPU)

fft.c

```
/* ARM CFFT module */
arm cfft radix4 instance f32 S;
/* Initialize the CFFT/CIFFT module, intFlag = 0, doBitReverse = 1 */
arm cfft radix4 init f32(&S, FFT SIZE, 0, 1);
/* Process the data through the CFFT/CIFFT module */
arm cfft radix4 f32(&S, Input);
/* Process the data through the Complex Magniture Module for calculating the magnitude at each bin */
arm cmplx mag f32(Input, Output, FFT SIZE);
/* Calculates maxValue and returns corresponding value */
arm max f32(Output+30, (FFT SIZE/2), &maxValue, &maxIndex);
ipc->fft writting=1;
/* Escalo y copio los resultados pero como int para M0*/
for (i = 0; i < FFT SIZE/2; i++)
       FFTOutput[i]=(int16 t)(40*(float32 t)((float32 t)Output[i]/(float32 t)maxValue));
ipc->fft writting=0;
```

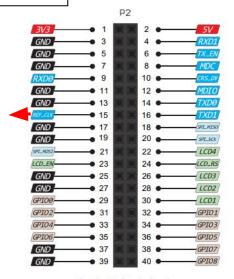
LPC 4337 PPL0Audio para FM

```
void FM Init PLL()
// FM con PLL0AUDIO
// IDIVA usa como fuente PPL1 (204MHz) y lo divide en 4
// PLLAUDIO en modo fraccional y usa como fuente a IDIVA (204/4=51MHz)
                                                                                                                                               fm.c
           LPC CGU->IDIV CTRL[CLK IDIV A] =
                                                                      // (Table 138) 0x4005 0048 - IDIVA control register
                                              (0x03<<2)|
                                                                      // divider value = 4
                                              (0x09<<24):
                                                                      // CLK SEL = PLL1;
           LPC CGU->PLL[CGU AUDIO PLL].PLL NP DIV =
                                                                     // (Table 134) 0x4005 0038 - PLL0AUDIO NP DIV - divider register
                                                                      // Post-Divider: [6:0] PDEC Decoded P-divider coefficient value
                                              (0<<12);
                                                          // Pre-Divider: [21:12] NDEC Decoded N-divider coefficient value
           LPC CGU->PLL0AUDIO FRAC = (uint32 t)(PLL FRAC);
                                                                      // (Table 135) 0x4005 003C bits 21:0 - PLL0AUDIO fractional divider register
           LPC CGU->PLL[CGU AUDIO PLL].PLL CTRL =
                                                                      // (Table 132) 0x4005 0030 - PLL0AUDIO control reg
                                                                                                                                    PLL0AUDIO
                                                                                                                                                                                                     Direct Output
                                                                                                                                                                                                                   Bypass
                                                                                                                                                                                                                    CTRL[1]
                                                                                                                                                                                                         CTRL[3]
                                                          (0 << 0)|
                                                                                 // PLL0 power UP
                                                          (0 << 1)I
                                                                                 // BYPASS
                                                          (1 << 2)
                                                                                 // DIRECTI
                                                                                                                          32kHz
                                                                                                                                                                                                                               FOUT
                                                                                                                            IRC
                                                          (0 << 3)
                                                                                 // DIRECTO
                                                                                                                    ENET_RX_CLK +
                                                          (1 << 4)
                                                                                 // CLKEN
                                                          (1 << 12)|
                                                                      // PLLFRACT_REQ
                                                                                                                       GP_CLKIN -
                                                                                                                                                                                           P-DIVIDER
                                                                                                                        CRYSTAL +
                                                                                                                                          N-DIVIDER
                                                          (0x0C<<24): // IDIVA (Clock source selection)
                                                                                                                           PLL1
                                                                                                                                    CLKIN
                                                                                                                          IDIVA +
                                                                                                                          IDIVB +
                                                                                                                          IDIVC +
                                                                                                                          IDIVD +
                                                                                                                                                                    Bandwidth Select P.I.R
                                                                                                                                                                                          NP_DIV[6:0]
                                                                                                                                       NP DIV[21:12]
                                                                                                                          IDIVE +
                                                                                                                                                                      MDIV[31:17]
void FM Play (uint8 t modulacion)
                                                                     // FM Modulator
                                                                                                                                                  Direct Input
                                                                                                                                                                        M-DIVIDER
                                                                                                                                                                                                                CLKEN
                                                                                                                                                 CTRL[2]
                                                                                                                                                                                                                CTRL[4]
                                                                                                                                CTRL[27:24]
  LPC_CGU->PLL0AUDIO_FRAC = (uint32_t)(PLL_FRAC + modulacion);
                                                                                                                                                    PLL0AUDIO
                                                                                                                                                 FRACTIONAL DIVIDER SEL_EXT -
  LPC_CGU->PLL[CGU_AUDIO_PLL].PLL_CTRL = // (Table 132) 0x4005 0030 - PLL04
                                              (0 << 0)
                                                                     // PLL0 power UP
                                                                                                                                                                           DECODER
                                              (0 << 1)
                                                                     // BYPASS
                                                                                                                                                                           ΣΔ MODULATOR
                                              (1<<2)
                                                                     // DIRECTI
                                              (0 << 3)
                                                                     // DIRECTO
                                                                                                                                                                            FRAC[21:0]
                                              (1 << 4)
                                                                     // CLKEN
                                                                                                                                                                            CTRL[12] (PLLFRACT REQ)
                                              (1 << 12)
                                                                     // PLLFRACT REQ
                                                                                                                                                                        MDIV[16:0]
                                              (0x0C<<24):
                                                                     // IDIVA (Clock source selection)
                                                                                                                   Fig 39. PLL0 with fractional divider
```

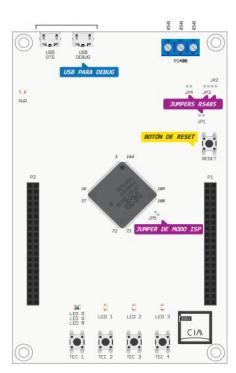
LPC 4337 PPL0Audio salida por Pin

REF_CLK •— 68 P1_19 ENET_TX_CLK SSP1_SCK R R CLKOUT R I2S0_RX_MCLK I2S1_TX_SCK

fm.c



Tira de 40 pines hembra de 0.1"(2,54 mm) de espaciado



Readme

Compilación

Para compilar y grabar el M4:

make

make download

Para compilar y grabar el M0

make TARGET=lpc4337_m0

make TARGET=lpc4337_m0 download

Readme

Utilización

Funciona sobre la EDU-CIAA-NXP. Conectar un pendrive al USB conteniendo archivos mp3 en el directorio raíz.

TEC2 y TEC3 para seleccionar archivo el "File Browser" y TEC1 para Play/Stop.

Las conexiones al TFT LCD ILI9341 son:

SD/MicroSD Card Reader --> EDU-CIAA-NXP

```
+ --> +3.3V

CS --> GPIO0

D/C --> GPIO1

DI --> SPI_MOSI

CLK --> SPI_SCK

DO --> SPI_MISO

G --> GND
```

Gracias por su atención!





https://github.com/telmomoya/educiaa-cese