Automated and Scalable Verification of Integer Multipliers

Mertcan Temel[1,2]
mert@utexas.edu

Anna Slobodova[2]
anna@centtech.com

Warren A. Hunt, Jr.[1]
hunt@cs.utexas.edu

[1]University of Texas at Austin, Austin, TX, USA

[2]Centaur Technology, Inc., Austin, TX, USA

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Introduction

- Wallace-tree and Booth Encoding define algorithms to design efficient integer multipliers for hardware.
- Verification of these multipliers is a difficult problem:
  - SAT Solvers and BDDs do not scale.
  - Equivalence checking requires structurally close specifications.
  - Computer algebra methods perform better but with limitations.
- We propose a more efficient, rewrite-based method that is:
  - widely applicable (tested for 75+ benchmarks),
  - scalable (1024x1024-bit multipliers proved under 10 minutes),
  - provably correct (verified using ACL2)
- Our method works with RTL-level hierarchical designs

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Overview

1. Review of Integer Multipliers
2. The Method
3. Experiments

Review: Integer Multipliers

$$\begin{array}{cccccccc} & a_2 & a_2 & a_2 & a_2 & a_1 & a_0 \\ \mathbf{x} & b_2 & b_2 & b_2 & b_2 & b_1 & b_0 \\ \hline \end{array}$$

- Goal: implement an efficient hardware module that multiplies two bit-vectors.
- Integer multipliers have two stages:
  1. Partial Product Generation (e.g., Baugh-Wooley, Booth Encoding)
  2. Partial Product Summation (e.g., Array, Wallace-tree, Dadda-tree)
- Even two designs following the same algorithm may have very different structures. Therefore, it is important to have an automated system for verification.

Wallace-tree multiplication on 3x3-bit signed numbers

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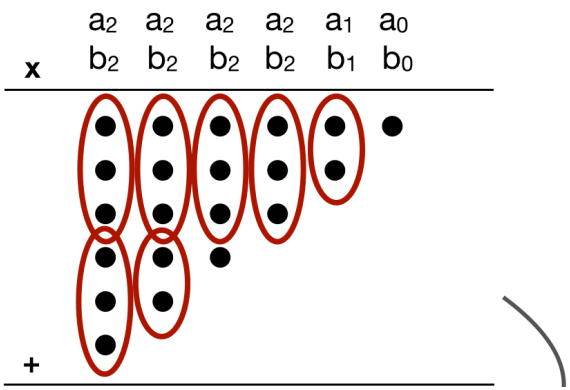

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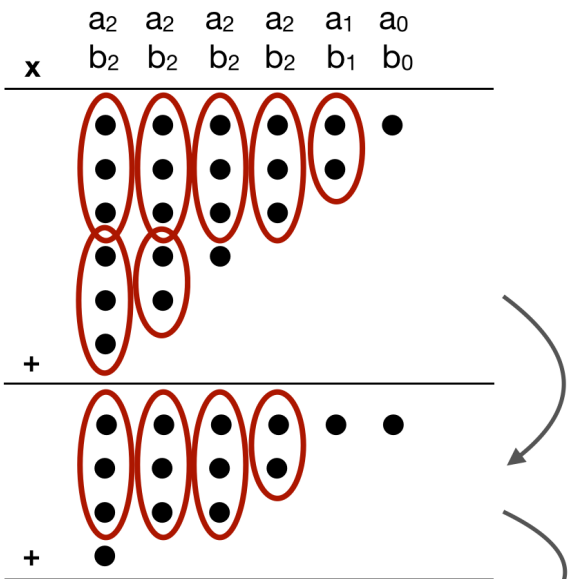

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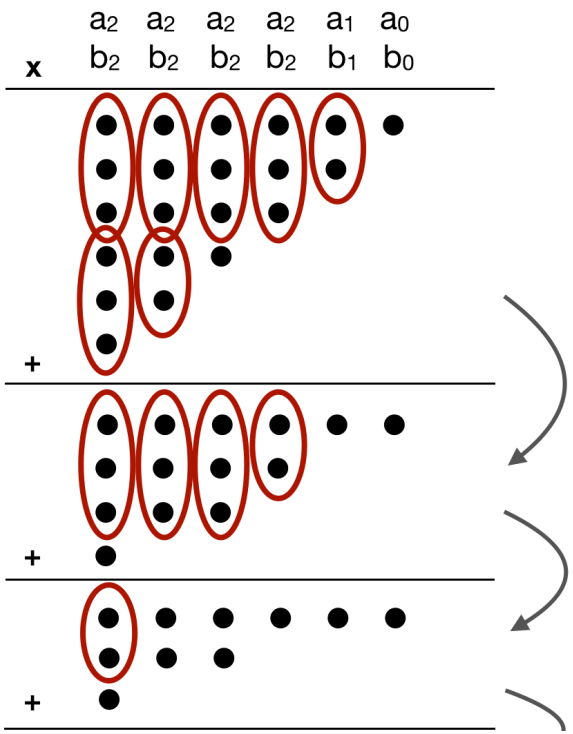

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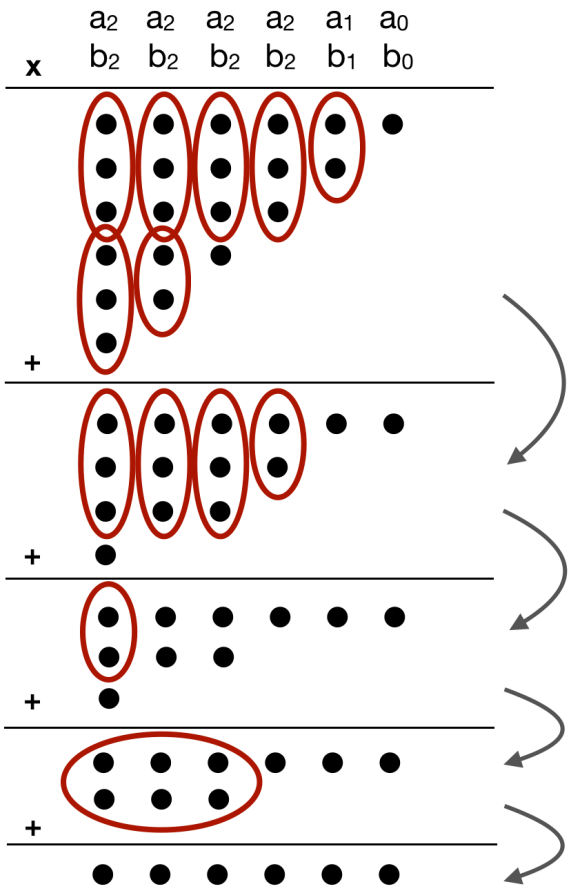

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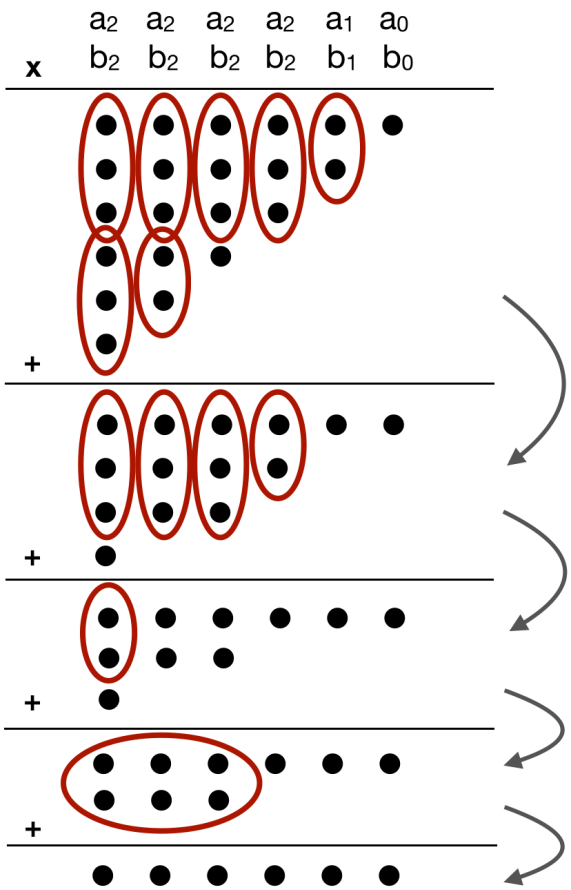

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Specification

Our goal is to prove such conjectures:

```
(defthm multiplier_is_correct
  (implies (and (integerp a)
                (integerp b))
           (equal (svl-run (list a b) <signed_mxn_mult>)
                  (truncate (+ M N)
                            (* (signext M a)
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- ACL2 is an interactive and automated theorem proving system.
- RTL Designs are translated from System Verilog to SVL format
- We prove that the circuit implements truncated multiplication of two sign-extended (or zero-extended) numbers.
- The mechanism we implemented to prove such conjectures are completely verified in ACL2.

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1. Before working on this conjecture, we reason about the adder modules
2. Then we submit the above event and:
   - Replace instantiations of adder modules with their specification from Step 1.
   - Simplify terms from summation tree algorithms.
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Step 1: Adder Module Proofs

Before the multiplier proof, a lemma for each adder module is proved:

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(defthm adder_module_is_correct
  (implies (and (integerp a)
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Specification for some adders per output bit:

Adder	out_3	out_2	out_1	out_0
Half-adder	-	-	$c(a+b)$	$s(a+b)$
Full-adder	-	-	$c(a+b+c_{in})$	$s(a+b+c_{in})$
Vector adders	$s(a_3+b_3 \; +c(a_2+b_2 \; +c(a_1+b_1 \; +c(a_0+b_0)))$	$s(a_2+b_2 \; +c(a_1+b_1 \; +c(a_0+b_0)))$	$s(a_1+b_1 \; +c(a_0+b_0))$	$s(a_0+b_0)$

where $s(x) = mod_2(x)$ and $c(x) = \left\lfloor \frac{x}{2} \right\rfloor$

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Both LHS and RHS should be rewritten to the same final form.

An example final form for the first 4 output bits of a multiplier:

out_3	out_2	out_1	out_0
$s(a_0b_3 + a_1b_2 + a_2b_1 + a_3b_0 + c(a_0b_2 + a_1b_1 + a_2b_0 + c(a_1b_0 + a_0b_1 + c(a_0b_0)))$	$s(a_0b_2 + a_1b_1 + a_2b_0 + c(a_1b_0 + a_0b_1 + c(a_0b_0)))$	$s(a_1b_0 + a_0b_1 + c(a_0b_0))$	$s(a_0b_0)$

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$s(a_0b_3 + a_1b_2 + a_2b_1 + a_3b_0$ $+c(a_0b_2 + a_1b_1 + a_2b_0$ $+c(a_1b_0 + a_0b_1$ $+c(a_0b_0)))$	$s(a_0b_2 + a_1b_1 + a_2b_0$ $+c(a_1b_0 + a_0b_1$ $+c(a_0b_0)))$	$s(a_1b_0 + a_0b_1$ $+c(a_0b_0))$	$s(a_0b_0)$

Step 2: Multiplier Module Proofs

Prove this conjecture:

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(defthm multiplier_is_correct
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Both LHS and RHS should be rewritten to the same final form.

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Step 2a: Simplify Summation Trees

The 4th LSB of the Wallace-tree multiplier
with simple partial products:

$$\begin{aligned} & s(\ s(\ s(a_3 b_0 + a_2 b_1 + a_1 b_2) \\ & \qquad + a_0 b_3 \\ & \qquad + c(a_2 b_0 + a_1 b_1 + a_0 b_2)) \\ & \quad + c(s(a_2 b_0 + a_1 b_1 + a_0 b_2) + c(a_1 b_0 + a_0 b_1))) \end{aligned}$$

Goal: Simplify such terms with a set of lemmas.

Nested instances of s can be cleared with the following lemma.

Lemma $\forall x, y \in \mathbb{Z}\ s(s(x) + y) = s(x + y)$

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Lemma $\forall x, y \in \mathbb{Z}\ c(x) + c(y) = d(x + y - s(x) - s(y))$
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Step 2b: Simplify Partial Products

Booth Encoding creates more complicated terms for partial products.

For example:

$$s([\neg b_1 b_0 a_1 \vee b_1 \neg b_0 \neg a_0 \vee b_1 b_0 \neg a_1] + c([b_1 b_0 \vee b_1 \neg b_0] + [b_1 \neg b_0 \vee \neg b_1 b_0 a_0 \vee b_1 b_0 \neg a_0]))$$

First, we perform algebraic rewriting to get rid of $\oplus$, $\vee$ and $\neg$.

Lemma $\forall x \in \{0,1\}\ \neg x = 1 - x$
Lemma $\forall x, y \in \{0,1\}\ x \vee y = x + y - xy$
Lemma $\forall x, y \in \{0,1\}\ x \oplus y = x + y - xy\ \ - xy$

When these lemmas are applied to the example above, we get:

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Step 2b: Simplify Partial Products (cntd.)

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Lemma $\forall x, y \in \mathbb{Z}\ s((-x) + y) = s(x + y)$
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Let's see the experiment results!

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Lemma $\forall x, y \in \mathbb{Z}\ d(x + x + y) = x + d(y)$

When these lemmas are applied to the example above, we get:

$$s(b_0 a_1 + b_1 a_0 + c(b_0 a_0))$$

Let's see the experiment results!

Experiments

Our method is tested for various integer multipliers with:

- Signed/unsigned simple or Booth Encoded partial products.
- Summation trees such as Wallace-tree, Dadda-tree, 4:2 compressor trees...
- Final stage adders such as Brent-Kung, Ladner-Fischer, Carry-lookahead...

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