Project Gantt Chart

Week columns (T0+):

#	Week	Date
1	1	October 1-5
2	2	October 8-12
3	3	October 15-19
4	4	October 22-26
5	5	Oct 29 - Nov 02
6	6	November 05-09
7	7	November 12-16
8	8	November 19-23
9	9	November 26-30
10	10	December 03-07
11	11	December 10-14
12	12	December 17-21
13	13	December 24-28
14	14	Dec 31 - Jan 04
15	15	January 7-11
16	16	January 14-18
17	17	January 21-25
18	18	January 28-31
19	19	February 4-7
20	20	February 11-14
21	21	February 18-21
22	22	February 25-28
23	23	March 4-7
24	24	March 11-14
25	25	March 18-21
26	26	March 25-28
27	27	April 1-4
28	28	April 8-11
29	29	April 15-18
30	30	April 22-25
31	31	Apr 22 - May 05
32	32	May 09-12
33	33	May 12-15

Top Summary

	Task	Timeline (weeks T0+)
	1. Semester	1 – 14
	Holiday	17 – 18
	2. Semester	20 – 33
1	Concept Development Phase (3 Weeks)	1 – 3
2	Assessment of System Requirement Phase (3 Week)	3 – 5
3	Conceptual Design and Preliminary Design Phase (4 Weeks)	4 – 7
4	Critical Design Phase (17 Weeks)	6 – 23
5	Test & Evaluation Phase (20 Weeks)	10 – 26
6	Implementation & Finalization Phase (8 Weeks)	26 – 33
7	Project Ending (T0+33 Weeks)	33

Detailed Schedule

#	Task	Timeline (weeks T0+)
1	**Concept Development Phase**	1 – 4
1.1	Activities	1
1.1.1	Literature Research and Determination and Similar Platform Specifications	2 – 4
1.1.2	Feasibility Works	1
2	**Assessment of System Requirement Phase**	3 – 5
2.1	Activities	3 – 5
2.1.1	Determination of Team Logo and Vision & Mission	3
2.1.2	Problem Define State for All Projects	3 – 4
2.1.3	Solve Defined Problem State for All Projects	4
2.1.4	General Component Research	3 – 4
2.2	Outcomes	
2.2.1	Business Statement Report	
3	**Conceptual Design and Preliminary Design Phase**	4 – 7
3.1	Activities	4 – 7
3.1.1	Preliminary Electrical System Design	4 – 7
3.1.1.1	Preliminary Sensing Unit Design	4 – 7
3.1.1.2	Preliminary Computational Unit Design	4 – 7
3.1.1.3	Preliminary Driving Unit Design	4 – 7
3.1.2	Preliminary Mechanical System Design	7
3.1.2.1	Preliminary Motion Unit Design	7
3.1.2.2	Preliminary Structure Design	7
3.2	Outcomes	
3.2.1	Preliminary Report	

ID	Task	T0+ 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33
	Date	Oct 1-5	Oct 8-12	Oct 15-19	Oct 22-26	Oct 29-Nov 02	Nov 05-09	Nov 12-16	Nov 19-23	Nov 26-30	Dec 03-07	Dec 10-14	Dec 17-21	Dec 24-28	Dec 31-Jan 04	Jan 7-11	Jan 14-18	Jan 21-25	Jan 28-31	Feb 4-7	Feb 11-14	Feb 18-21	Feb 25-28	Mar 4-7	Mar 11-14	Mar 18-21	Mar 25-28	Apr 1-4	Apr 8-11	Apr 15-18	Apr 22-25	Apr 22-May 05	May 09-12	May 12-15
4	**Critical Design Phase**							█	█	█	█	█	█	█	█	█	█	█	█	█	█	█	█	█										
4.1	**Subsystem Design Phase**	█	█	█	█	█	█	█	█	█	█	█	█	█	█																			
4.1.1	Sensing System Desing							█	█	█	█	█					█	█	█	█	█	█												
4.1.1.1	Lane Detection Subsystem Design							█	█	█	█	█																						
4.1.1.2	Vehicle Detection Subsystem Design																█	█	█	█	█	█												
4.1.2	Computation System Desing										█	█			█	█	█	█	█	█	█	█												
4.1.2.1	Data Proccesing Subsystem Design										█	█																						
4.1.2.2	PID Controller Subsystem Design														█	█	█	█	█	█	█	█												
4.1.3	Communication System Design											█	█	█	█																			
4.1.3.1	Internal Communication Subsystem Design												█																					
4.1.3.2	External Communication Subsystem Design											█	█	█	█																			
4.1.4	Driving System Design														█	█	█	█	█	█	█													
4.1.4.1	Direction Subsystem Design														█	█	█	█																
4.1.4.2	Speed Subsystem Design																	█	█	█	█													
4.1.5	Structure System Design						█	█	█	█	█	█							█	█	█	█	█	█										
4.1.5.1	Chassis Subsystem Design						█	█	█	█	█	█																						
4.1.5.2	PCB Subsystem Design																		█	█	█	█	█	█										
4.1.6	Motion System Design											█	█	█			█	█	█															
4.1.6.1	Wheels Subsystem Design											█	█	█																				
4.1.6.2	Motors Subsystem Design												█	█			█	█	█															
4.2	**Critical Design Outputs**							█	█	█	█	█	█	█	█	█	█	█	█	█	█	█	█	█										
4.2.1	Standards Report																																	
4.2.2	Module Test Demo												█																					
4.2.3	Conceptual Design Report													█																				
4.2.4	Presentations													█	█																			
4.4.1	Critical Design Review Report																							█	█									

ID	Task	Timeline (shaded weeks)
5	**Test & Evalution Phase**	Dec 03-07; April 8-11 to April 15-18
4.1	**Subsystem Test Phase**	Dec 17-21 to March 18-21
4.1.1	Sensing System Testing	Dec 17-21 to January 14-18; February 11-14 to March 18-21
4.1.1.1	Lane Detection Subsystem Testing	Dec 17-21 to January 14-18
4.1.1.2	Vehicle Detection Subsystem Testing	February 11-14 to March 18-21
4.1.2	Computation System Testing	Dec 24-28 to March 4-7
4.1.2.1	Data Proccesing Subsystem Testing	Dec 24-28 to February 4-7
4.1.2.2	PID Controller Subsystem Testing	January 21-25 to March 4-7
4.1.3	Communication System Testing	January 14-18 to March 4-7
4.1.3.1	Internal Communication Subsystem Testing	January 14-18 to February 4-7
4.1.3.2	External Communication Subsystem Testing	February 11-14 to March 4-7
4.1.4	Driving System Testing	January 21-25 to March 11-14
4.1.4.1	Direction Subsystem Testing	January 21-25 to February 25-28
4.1.4.2	Speed Subsystem Design	February 11-14 to March 11-14
4.1.5	Structure System Testing	Dec 24-28 to February 11-14; March 25-28 to April 15-18
4.1.5.1	Chassis Subsystem Testing	Dec 24-28 to February 4-7; March 25-28 to April 15-18
4.1.5.2	PCB Subsystem Testing	March 25-28 to April 15-18
4.1.6	Motion System Testing	November 12-16 to November 26-30; February 11-14 to March 4-7
4.1.6.1	Wheels Subsystem Testing	November 12-16 to November 26-30; February 11-14 to February 25-28
4.1.6.2	Motors Subsystem Testing	November 12-16 to November 26-30; February 11-14 to March 4-7
6	**Finalization Phase**	March 25-28 to May 12-15
6.1	Activities	March 25-28 to May 12-15
6.1.1	To be detailed	
6.2	Outcomes	April 1-4 to May 12-15
6.2.1	Finalized Product	April 15-18
6.2.2	Final Report	May 09-12
6.2.3	Final Demo	May 12-15
7	**Project Ending**	