

MIDDLE EAST TECHNICAL UNIVERSITY

ELECTRICAL & ELECTRONICS ENGINEERING DEPARTMENT

EE400 SUMMER PRACTICE REPORT

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1.Introduction

I have performed my summer practice (SP) (EE400) in ASELSAN from 18 June to 13 July. I have worked in analog design department of Communication and Information Technologies Vice Presidency. In this department, I have worked on two DC-DC converter designs, and I have observed working environment. I had change to work from simulations to practical tests and analysis of a converter section of a power card. I have started to my SP with theoretical research and studying from power electronics written by Mohan because converter topologies was a new concept for me, and at first building a theoretical background was a must to make a design. Secondly, I have studied data sheets of LTC3779 (IC), DC2456A (Demo Board). After this stage, I have moved on with simulations, and finally, I have made experiments on the demo board to analyze design. I preferred ASELSAN because I liked military designs and works.

In this report, I begin with introduction of the ASELSAN. After that, main part covers what I have done and my observations during my summer practice.

2. General Description of the company

ASELSAN was established after Cyprus peace operation in 1975 to provide Turkish Forces' telecommunication requirements. Since then, ASELSAN is the biggest defense company of the Republic of the Turkey, and an important player in this industry globally. Today, ASELSAN employed almost 5000 personal and 70% of them are engineers.

2.1. Organizational Structure of the company

ASELSAN has five main departments which are Communication and Information Technologies Vice Presidency (HBT), Microelectronics, Guidance and Electro-Optics Vice Presidency (MGEQ), Radar and Electronic Warfare Systems Vice Presidency (REHIS), Defense Systems Technologies Vice Presidency (SST) and Transportation, Security, Energy and Automation Systems Vice Presidency (UGES). HBT is in Macunköy and METU Technopolis, MGEQ is in Akyurt, REHIS is in Gölbaşı, and SST and UGES are in Macunköy.

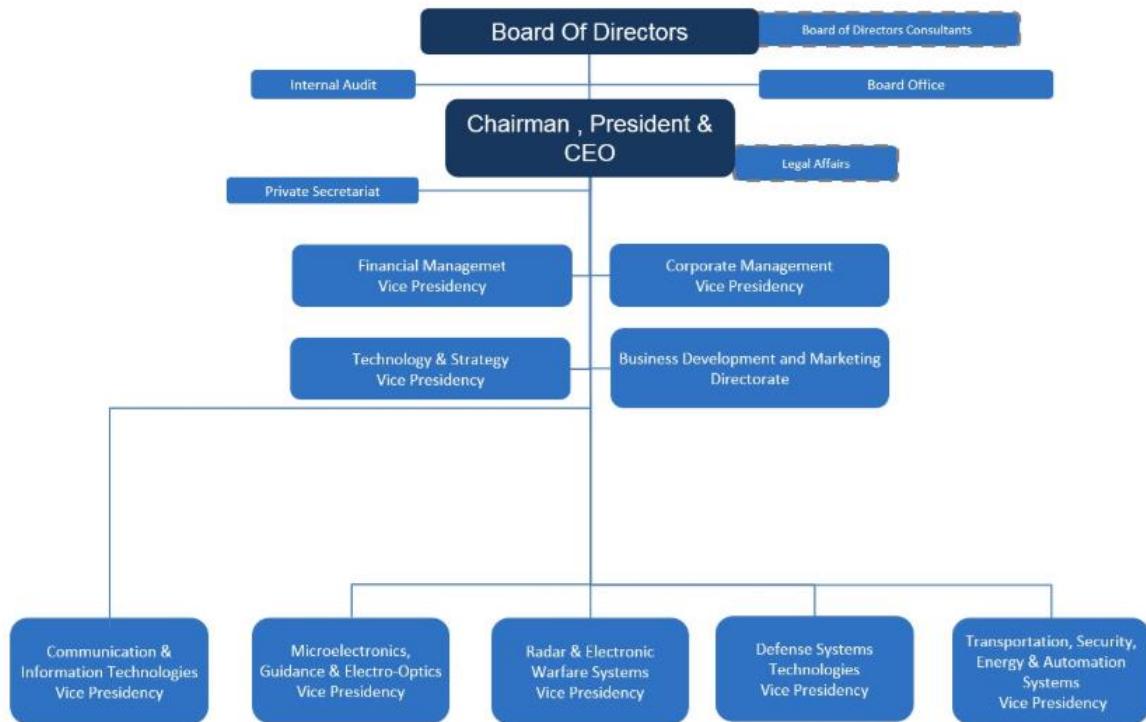


Figure 1: Organizational Structure of the Company

I spent my summer practice at HBT's Technopolis facility. I worked under Analog design Subgroup which is under Electronic hardware subgroup. This section is responsible from power cards and supplies of the telecommunication systems. They design these parts according to specific requirements and make initial tests of the power designed section up to mass production.

2.2. History

Askeri Elektronik Sanayi (ASELSAN) was founded in 1975 because of a sad event which was happened at Cyprus peach operation. In 1980, the first manpack and tank wireless radios were delivered to the Turkish Armed Forces. Field Telephones, Computer Controlled Central Systems and Laser Distance Measurement Appliances were added to the inventory between the years 1982-1985. In 1990, ASELSAN was restructured in the 3 groups according to its fields of activity. In 1992, ASELSAN improved its product range with Radar Systems. In 1997, ASELSAN 1919 Cell Phone was launched to the market. In 2007, MILGEM war system supply project was executed. From past to now, ASELSAN works on improving and producing new technologies.

3.DC-DC converters brief information

3.1 Some application area of this type converters

- Output regulation: generally, systems demand steady voltage and current, but because of some external effects, such as changing total demand etc., main source cannot handle with conditions. To eliminate decrease or increase in the main source, DC-DC converters is a solution.
- Convert input supply according to sub-unit requirement: In overall system, input voltage may not be suitable for sub-unit or current requirement may be different, so by using these converters, one source is enough for all system.
- Increase input voltage to decrease the transmission loss in the system: to eliminate current effect on the card for thermal and efficiency purposes, stepping up the input voltage can be necessary solution.

3.2 Buck- Boost Converter Topology

Buck-Boost converter is designed to set output to a specific value. It works as combination of buck and boost converters, according to input value. When input is lower than required value, it turns into a boost converter, or vice-versa.

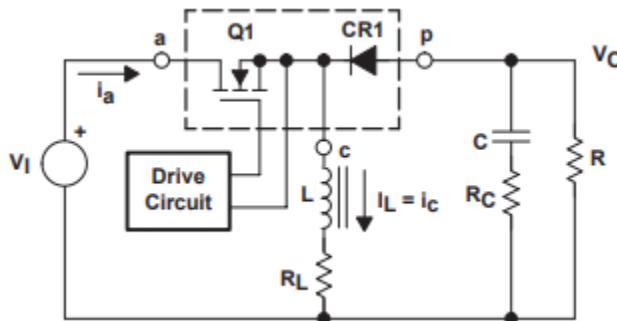


Figure 2: Basic Buck-Boost topology[x]

Figure 2 shows basic topology of this type converter, on the figure 2 R_C represent Equivalence Series Resistance (ESR) of capacitor and R_L is dc resistance of the inductor. Q_1 is the switch which keeps the output voltage steady by turning on and off.

In action Q_1 and CR_1 work reverse, when one is on, the other is off. Thanks to that, input and output never be short circuit in this structure. According to figure, when Q_1 is on inductor is charged by input source, otherwise it is discharged by the load. Basically, inductor is the storage element, and according to action of Q_1 , it gives its power to output or store power from input. Output voltage is regulated by the Q_1 . When Q_1 's on time increase, storage increase, so off time power delivery is also increase. Because of these, output voltage increase. To eliminate ripples and obtain continuous wave form at the output C is used. Thanks to charging characteristic of the capacitors, we obtain smooth output voltage as the following parts of the report.

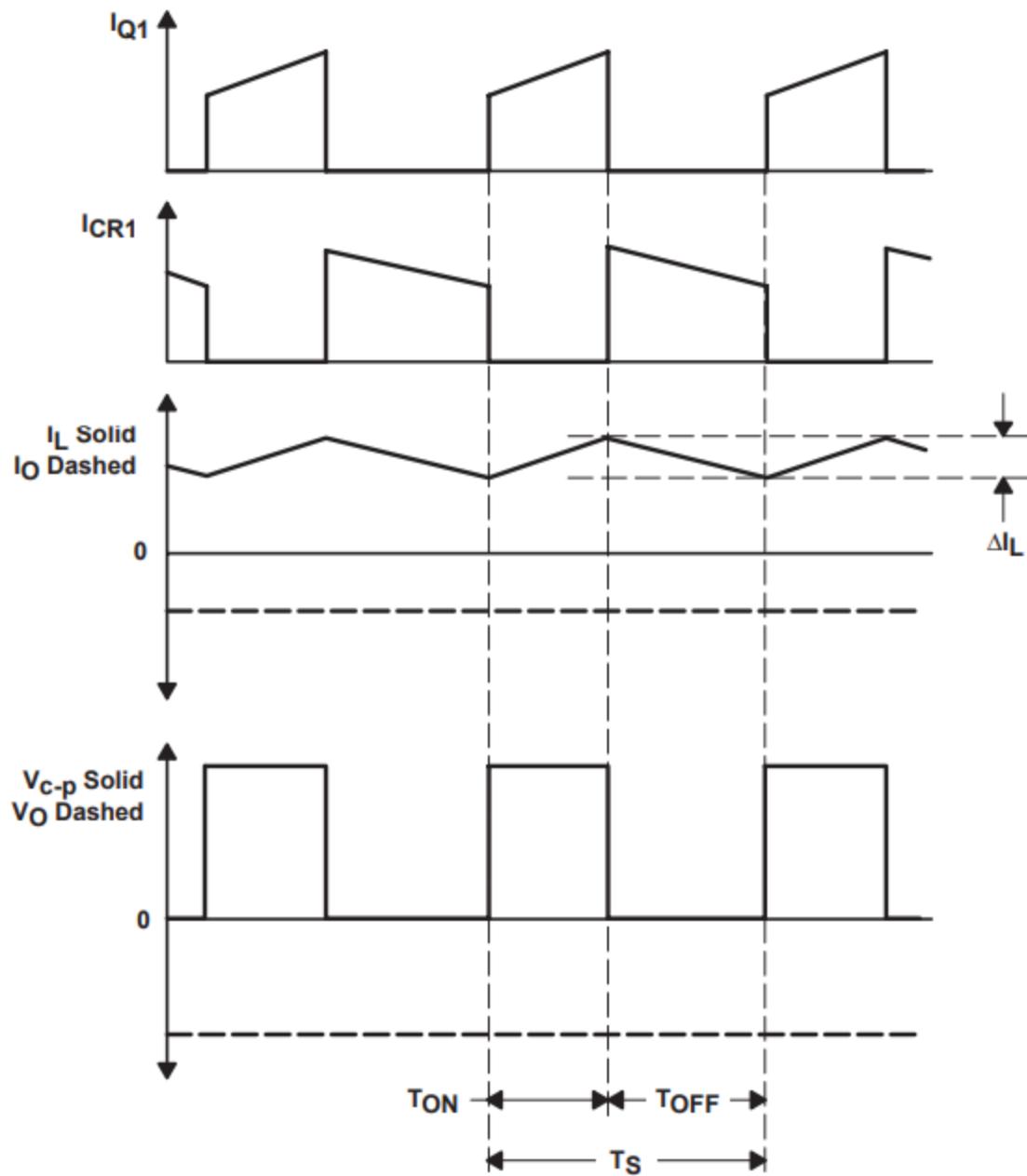


Figure 3: Wave forms of the Buck-Boost converter[x]

Today's applications Integrated Circuits and 4-switches topology are used. The reason of this is that high switching frequency demand small component, and by using that, thermal loss lowered. Basic circuit schema is like Figure 4. Therefore, I worked on this structure during my summer practice. I used LTC 3779 IC and different external components, according to my design requirements.

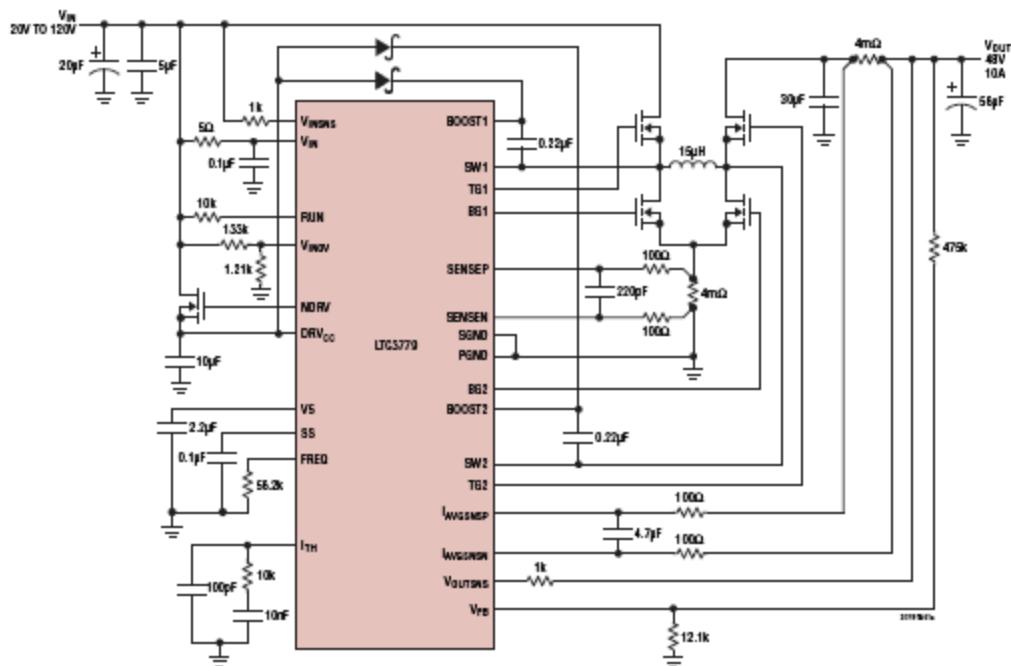


Figure 4: 4- switches buck-boost converter LTC 3779 basic topology. []

4. Demo Board

Demo boards are good way to introduce a product to consumers. They are generally basic card with example setup for an advertising IC. During my SP, I worked on a demo board and tested in different condition and with different components. Although they are simple cards, there is still crucial part of their design which should consider during design. As expectation, I did not design card during my SP because of limited time and that my work was just a small part of a complicated power unit, so my design would be meaningless. However, if I had a chance to design my card, as demo board design considered, I needed to be aware of some important location of some components.

At first, Thermal issues are the most important part. During a card design, thermal heat loss and high heat dense components should be placed properly for cooling and not affecting other parts. As we can see from my demo board in Figure 5 switching transistors and Inductor placed away from IC.

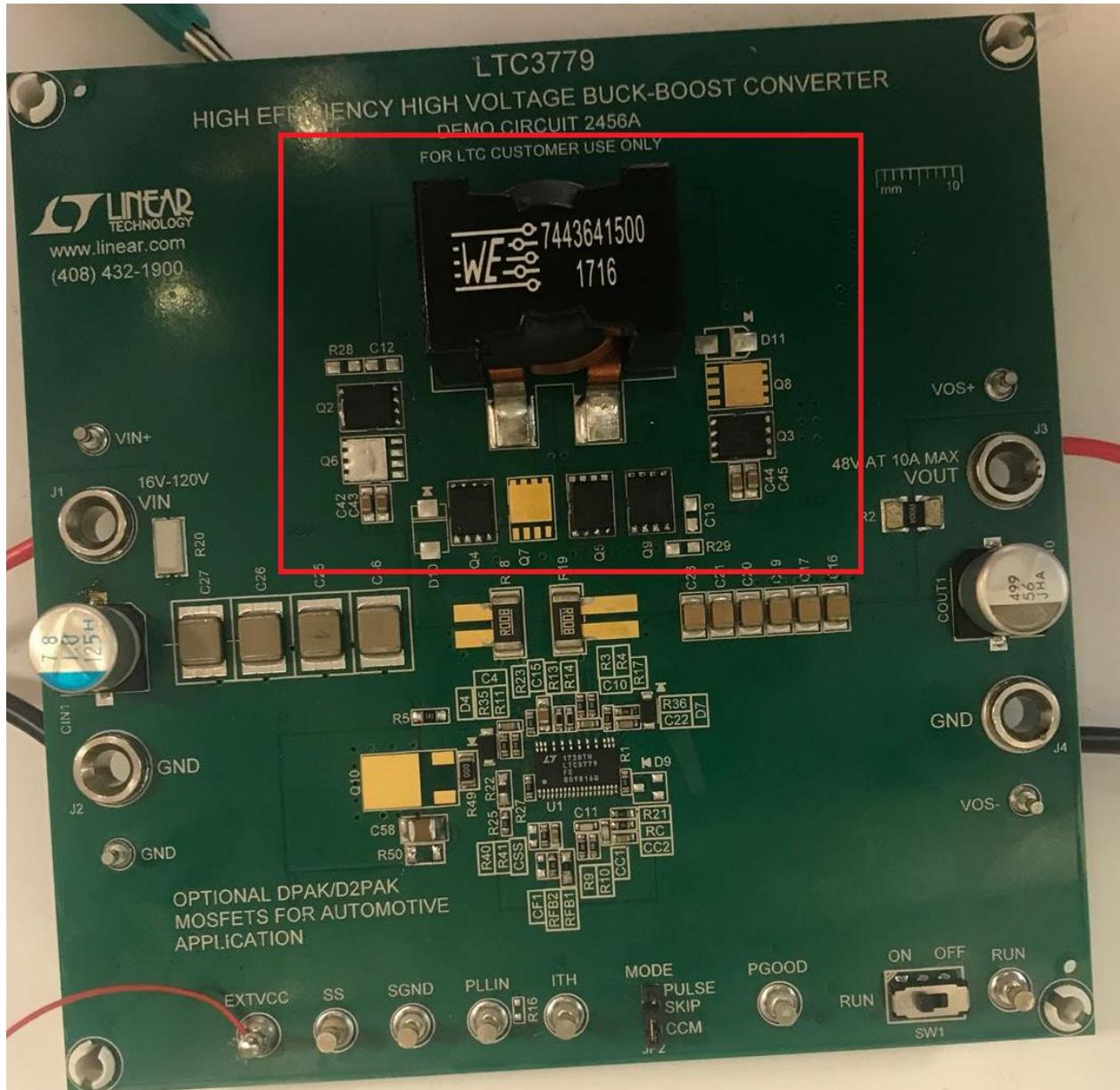


Figure 5: Picture of the Demo board with labeling switching transistors and Inductor

Another important part of the design is component location. As we can see from Figure 5 and Figure 6, some of the resistors and capacitors or transistors located extremely close to IC (even for this purpose, some of the components placed other side of the card as we can see from figure 6) to reduce losses and increase efficiency.

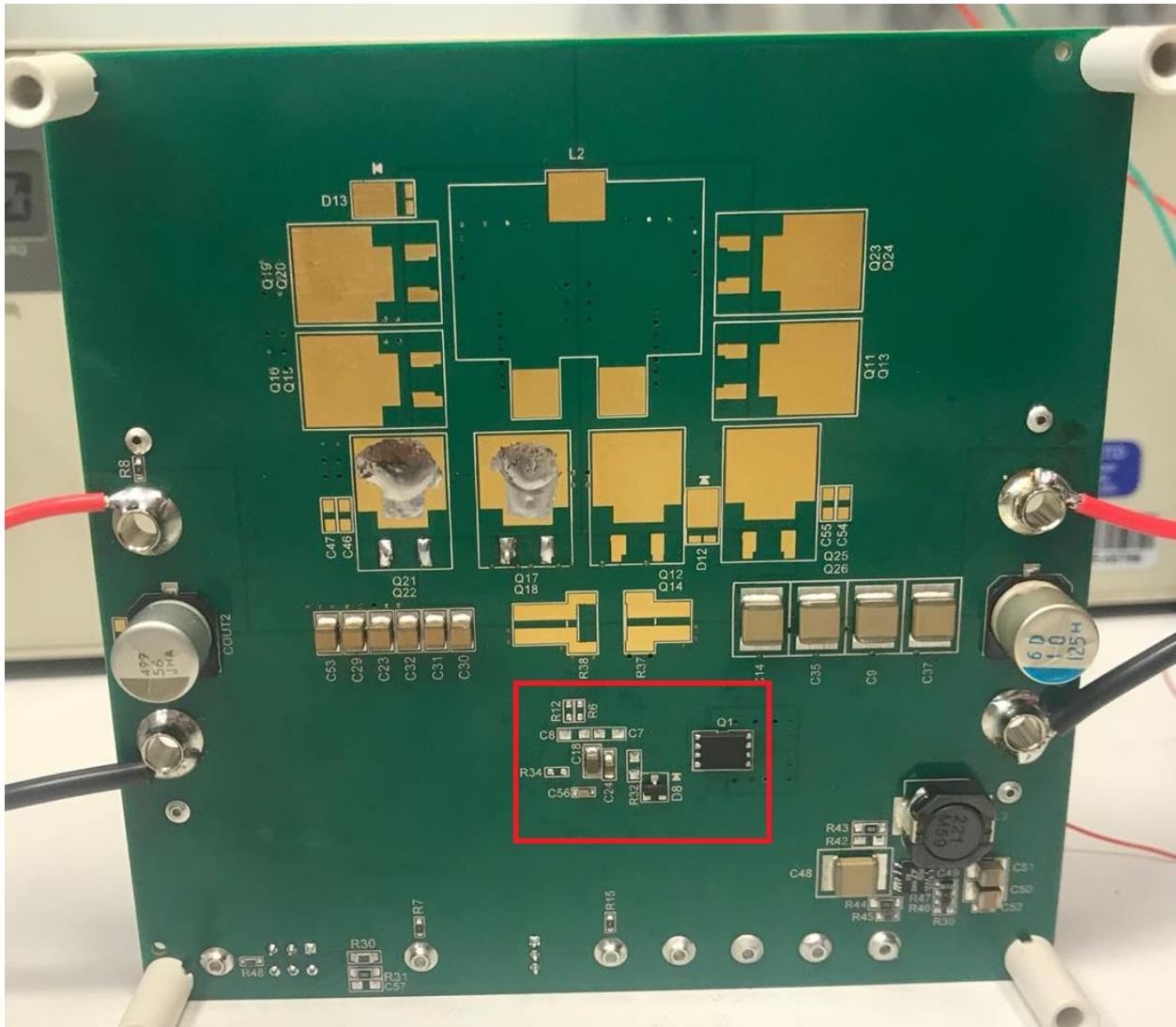


Figure 6: Picture of the Demo board with labeling components which placed behind of the card to be able to locate close to IC

5. Vin = 10.5-36 V, O/P 50 V 330W/200W Boost Dc-Dc converter

I have two different converter tasks to design during my summer practice, first one has 50V/330W output and second one has 22V/145W output. My summer practice supervisor has already decided to my IC which is LTC3779. In this section we consider first design. Input of these designs are in the range of 10.5-36V. However, there is a trick in this range which is that 10.5-17V range controller decrease the output current to decrease the stress of the converter because for low input case, by decreasing efficiency, thermal problems occur as we consider following parts.

Requirements:

$$V_{in} = 10.5-36 \text{ V}$$

$$V_{out} = 50\text{V}/6.6\text{A}$$

$$f_s = 250\text{-}500 \text{ KHz}$$

$$\Delta V_{\text{ripple}} = V_{\text{out}}/100$$

To satisfy these requirements, I start to my design by selection switching frequency. I choose 400KHz because increasing frequency gives me a chance to use small components and using small area on the card, but because of the increasing frequency switching loss increase, and I try to choose around to center frequency because according to result of my first analysis, I can modify frequency better (if I choose lower part of the range of frequencies, I needed to sweep whole area, but thanks to this choose half range sweep is enough).

5.1. Component Selection

While making a design, I need to choose components according to datasheet of the converter (LTC3779) since every Integrated Circuit (IC) has different algorithm and equation for components which determine by internal design of the IC. In this section equations are taken from datasheet of the LTC3779.

a.) Inductor

$$L_{\text{BOOST}} > \frac{V_{\text{IN(MIN)}}^2 \cdot (V_{\text{OUT}} - V_{\text{IN(MIN)}}) \cdot 100}{f \cdot I_{\text{OUT(MAX)}} \cdot \% \text{Ripple} \cdot V_{\text{OUT}}^2} \text{ H}, \quad (1)$$

Equation (1) is gives the minimum value of the Inductor. In this equation, I choose Ripple is 40% since generally ripple set to 20% to 40%. After calculation, result is $L > 1.65 \mu\text{H}$. After this result, I pick $L = 2.2 \mu\text{H}$ because it was the closest value of my calculation and small value means small size.

Also, current and resistance properties of the inductor should consider. Minimum resistance increases efficiency of the design, but it, also, increase size of the coil.

b.) Capacitor

$$\Delta V_{\text{RIPPLE(BOOST,CAP)}} = \frac{I_{\text{OUT(MAX)}} \cdot (V_{\text{OUT}} - V_{\text{IN(MIN)}})}{C_{\text{OUT}} \cdot V_{\text{OUT}} \cdot f} \text{ V} \quad (2)$$

$$\Delta V_{(\text{BOOST},\text{ESR})} = I_{\text{OUT(MAX,BOOST)}} \cdot \text{ESR} \quad (3)$$

Equation (2) gives me the approximate value of the output capacitance according to output voltage ripple. Equation (3) is gives me the Equivalence Series Resistance (ESR) of the output capacitance should have in the same condition with previous case. Acceptable condition of my design is 1% output voltage ripple, so when calculation is made, results are $C_{\text{out}} = 26 \mu\text{F}$ and $\text{ESR} = 75.75 \text{ m}\Omega$.

c.) Power MOSFET

While choosing these components, I consider $R_{ds(on)}$ value which is related with current loss. For boost region, main load is on the MOSFET A, C and D and MOSFET, so we consider their values.

$$P_{A,BOOST} = \left(\frac{V_{OUT}}{V_{IN}} \cdot I_{OUT(MAX)} \right)^2 \cdot \rho_\tau \cdot R_{DS(ON)} \quad (4)$$

$$P_{C,BOOST} = \frac{(V_{OUT} - V_{IN})V_{OUT}}{V_{IN}^2} \cdot I_{OUT(MAX)}^2 \cdot \rho_\tau \\ \cdot R_{DS(ON)} + k \cdot V_{OUT}^3 \cdot \frac{I_{OUT(MAX)}}{V_{IN}} \cdot C_{RSS} \cdot f \quad (5)$$

$$P_{D,BOOST} = \frac{V_{IN}}{V_{OUT}} \cdot \left(\frac{V_{OUT}}{V_{IN}} \cdot I_{OUT(MAX)} \right)^2 \cdot \rho_\tau \cdot R_{DS(ON)} \quad (6)$$

To solve these equations, I set $P_{max}=2W$ as a suggestion of my summer practice supervisor (He considers card design and his cooling approach). Also, I choose $\rho_\tau=1.5$ which is based on worst case assumption for junction temperature = 125 degree Celsius according to figure 7.

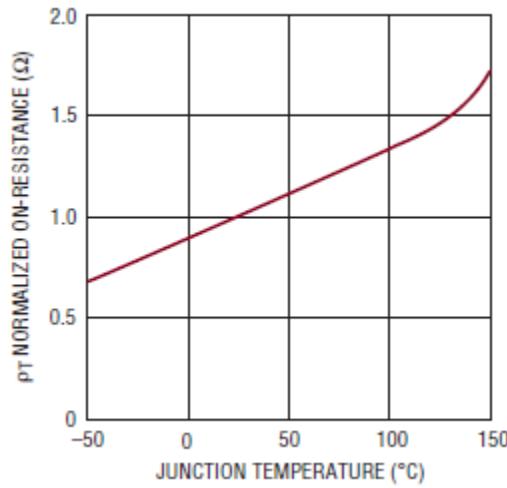


Figure 7: Normalized $R_{ds(on)}$ vs Temperature

Under these conditions;

$$R_{ds(on), A} < 1.35 \text{ m}\Omega$$

$$R_{ds(on), D} < 9.94 \text{ m}\Omega$$

I cannot solve the equation (5) because there are two unknowns with one equation. I approach to this MOSFET experimentally.

There is another important parameter which is Vds value of transistor. Basically, is represent that voltage value of the transistor can handle.

d.) Sense Resistor

$$R_{SENSE(MAX,BOOST)} = \frac{2 \cdot V_{RSENSE(MAX,BOOST,MAXDC)} \cdot V_{IN(MIN)}}{(2 \cdot I_{OUT(MAX,BOOST)} \cdot V_{OUT(MIN)}) + (\Delta I_{L(MAX,BOOST)} \cdot V_{IN(MIN)})} \Omega \quad (7)$$

$$\Delta I_{L, BOOST} = \frac{V_{IN}}{f \cdot L} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}} \right) \quad (8)$$

According to equation (7) and (8), $R_{sense} = 3.876 \text{ m}\Omega$

The main components are selected by these methods from library of the LTspice after this part my design shapes like figure 8.

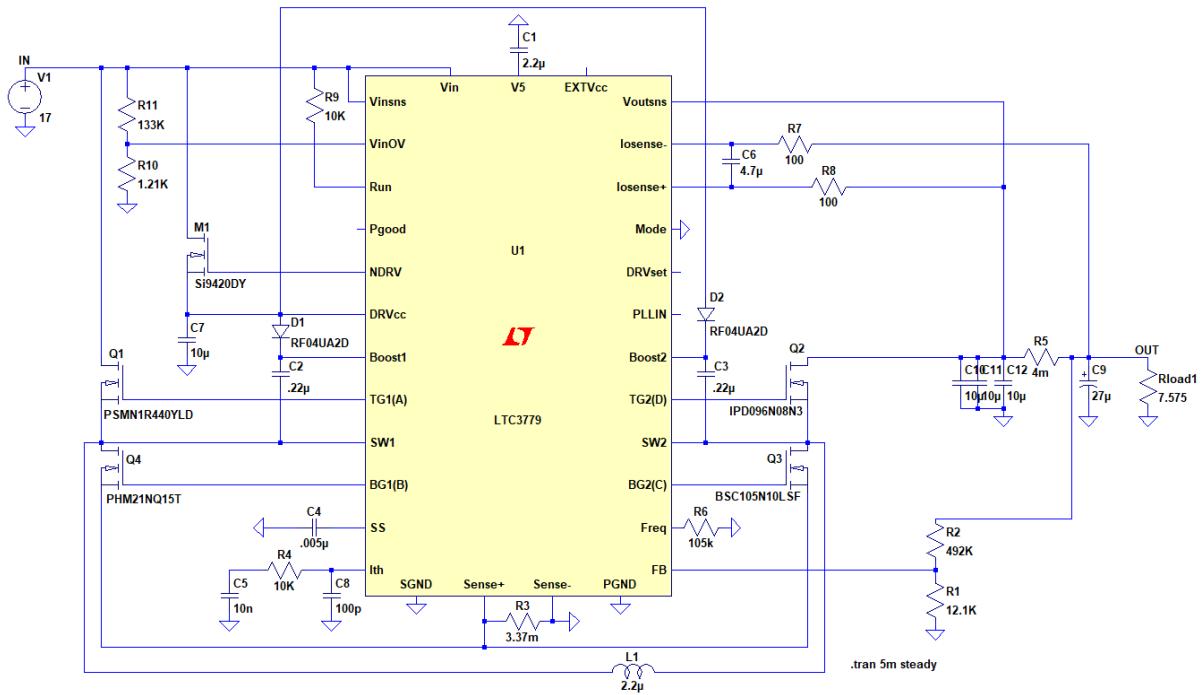


Figure 8: Overall design

Additionally, some of the components are not mentioned above because selection of them is straightforward, but if to be superficially mentioned, Freq pin's resistor selected according to datasheet curve to obtain 400KHz, approximately 105K Ω resistor should be selected. SS pin determines speed of the IC with relation of this equation $t_{ss} = C_{ss} * \left(\frac{1.2V}{5\mu A}\right)$. To speed up, 0.005uF selects. FB pin's voltage division resistors are chosen by equation which is $V_{out} = 1.2V * (1 + R_B/R_A)$.

5.1.1 Simulation and Modifications

I start with output analysis of the design. During my simulation, I use 17V input because lower limit of 330W output is 17V. When input gets lower than 17V output is drop to 200W. Firstly, I start to my analysis 17V input/330W output condition, and following wave forms are obtained:

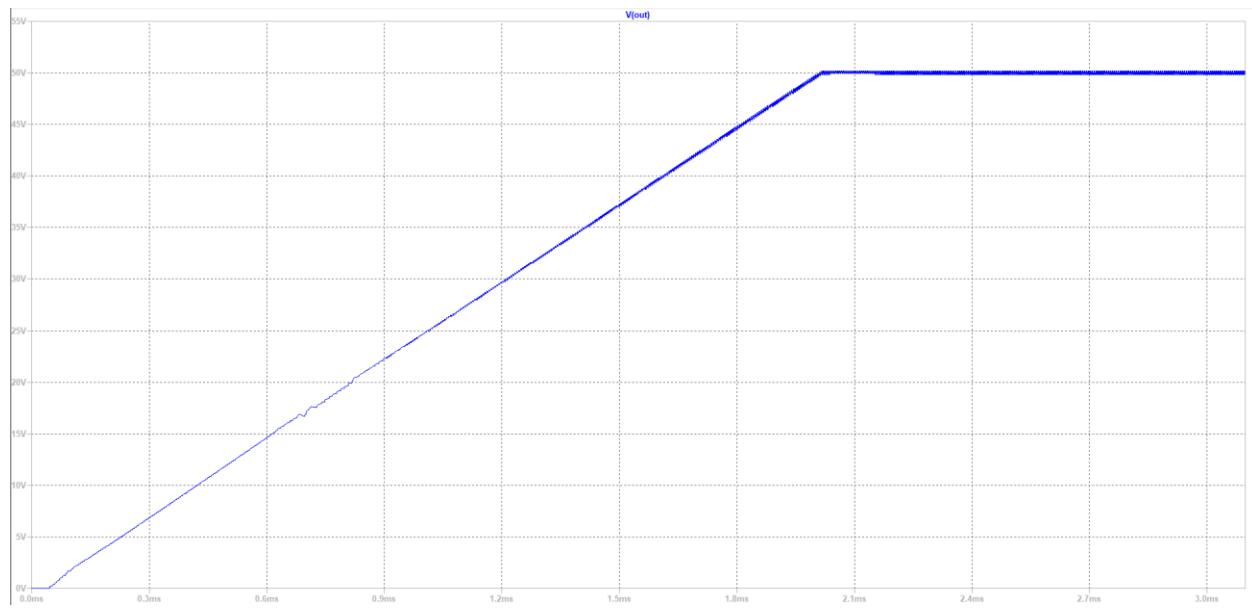


Figure 9: Output wave form of figure 8

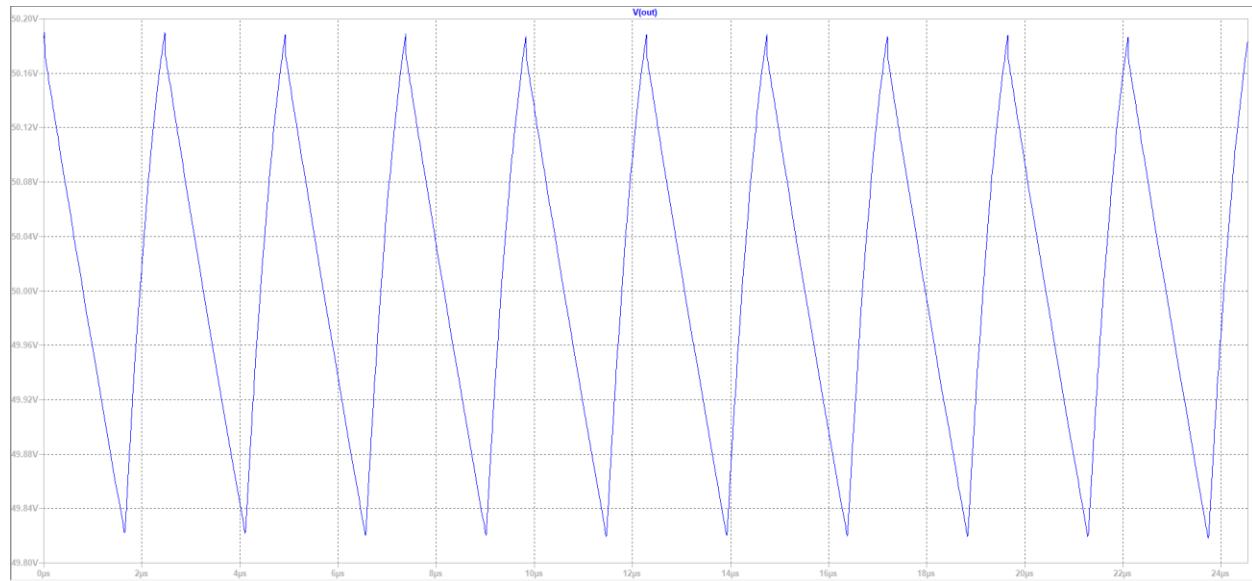


Figure 10: Steady state simulation of figure 8

According to figure 9 and figure 10, output is good and smooth (output voltage ripple is less than 500mV). After this point, I check efficiency of my design on the LTspice efficiency report.

--- Efficiency Report ---			
Efficiency: 95.0%			
	Input: 347W @ 17V	Output: 330W @ 50V	
Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	0mA	2mA	0mW
C3	68mA	1025mA	0mW
C4	0mA	0mA	0mW
C5	0mA	0mA	0mW
C6	0mA	0mA	0mW
C7	110mA	1280mA	0mW
C8	0mA	0mA	0mW
C9	245mA	429mA	26mW
C10	3735mA	90570mA	0mW
C11	3735mA	90570mA	0mW
C12	3735mA	90570mA	0mW
D1	0mA	2mA	-0mW
D2	15mA	169mA	5mW
L1	20725mA	26602mA	1354mW
M1	23mA	25mA	202mW
Q1	20725mA	26696mA	403mW
Q2	13012mA	264691mA	1766mW
Q3	17864mA	278953mA	12164mW
Q4	11mA	4763mA	-0mW
R1	0mA	0mA	119µW
R2	0mA	0mA	5mW
R3	17867mA	279544mA	1076mW
R4	0mA	0mA	0µW
R5	6605mA	7051mA	175mW
R6	0mA	0mA	42µW
R7	0mA	0mA	0µW
R8	0mA	0mA	0µW
R9	0mA	0mA	0µW
R10	0mA	0mA	19µW
R11	0mA	0mA	2mW
Rload1	6601mA	6625mA	330100mW
U1	158mA	1724mA	146mW

Figure 11: Efficiency report of the figure 8 design

When we analyses efficiency results in figure 10, overall efficiency (input and output powers) seems well. However, when numbers are detailed analyze, power dissipation is localized few components, so this is not acceptable for our case because cooling cannot handle with more than 2 W dissipation. Therefore, Q3 switching transistors are in danger. When we check detail dissipation characteristic Q3 and Q2 (Q2 is, also, close to 2W), we obtain figure 11.

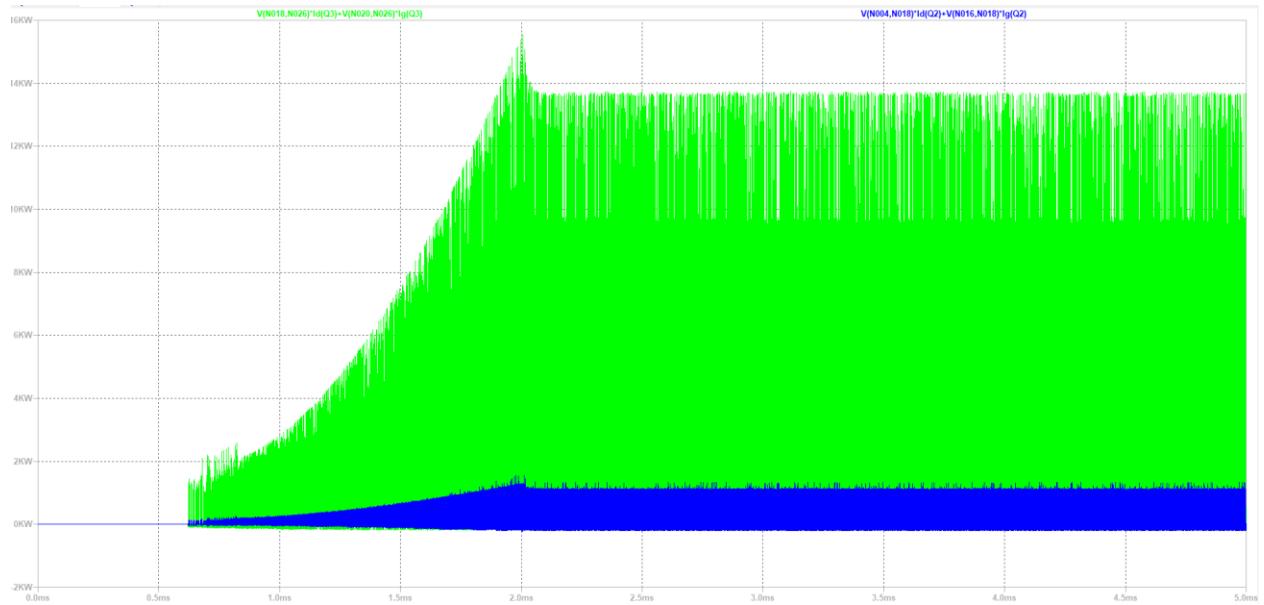


Figure 12: Power dissipation of Q3 and Q2 MOSFETS

To eliminate this high dissipation, we decide to be doubling these transistors. Thanks to that, we decrease load on a single transistor. Besides, R3 resistor has 1W dissipation. We, also, want to decrease this value because increasing dissipation increases cost and system temperature. Therefore, we add 3 parallel resistors instead of single resistor. After these steps, overall design looks like figure 12.

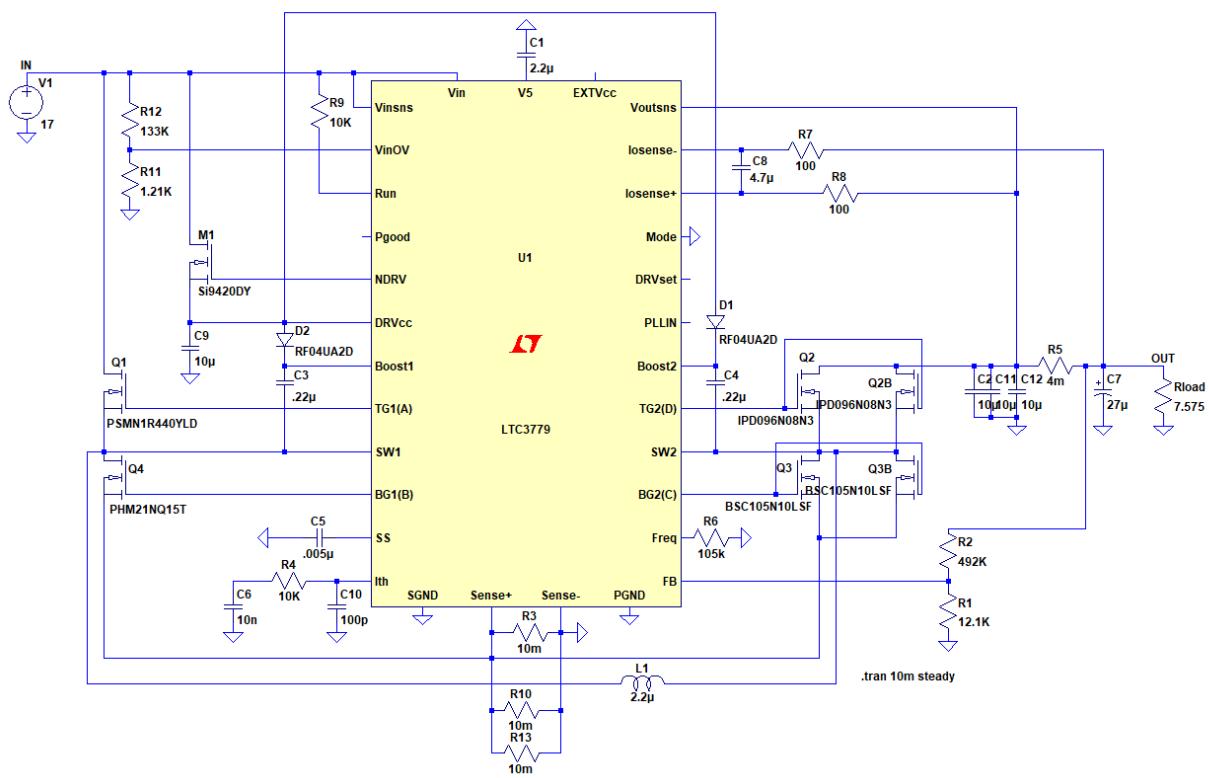


Figure 13: Modified overall design

--- Efficiency Report ---
Efficiency: 95.1%

Input: 347W @ 17V
Output: 330W @ 50V

Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	3735mA	88070mA	0mW
C3	0mA	1mA	0mW
C4	123mA	1629mA	0mW
C5	0mA	0mA	0mW
C6	0mA	0mA	0mW
C7	246mA	430mA	26mW
C8	0mA	0mA	0mW
C9	185mA	1899mA	0mW
C10	0mA	0mA	0mW
C11	3735mA	88070mA	0mW
C12	3735mA	88070mA	0mW
D1	35mA	475mA	11mW
D2	0mA	1mA	-0mW
L1	20706mA	26598mA	1352mW
M1	44mA	51mA	386mW
Q1	20706mA	26598mA	402mW
Q2	6507mA	128597mA	550mW
Q2B	6507mA	128597mA	550mW
Q3	8922mA	135688mA	6191mW
Q3B	8922mA	135688mA	6191mW
Q4	8mA	3390mA	-0mW
R1	0mA	0mA	119µW
R2	0mA	0mA	5mW
R3	5949mA	90744mA	354mW
R4	0mA	0mA	0µW
R5	6606mA	7056mA	175mW
R6	0mA	0mA	42µW
R7	0mA	0mA	0µW
R8	0mA	0mA	0µW
R9	0mA	0mA	0µW
R10	5949mA	90744mA	354mW
R11	0mA	0mA	19µW
R12	0mA	0mA	2mW
R13	5949mA	90744mA	354mW
U1	261mA	2564mA	289mW

Figure 14: Efficiency report of modified design

According to figure 13, as we expected, load on the transistors (Q2 and Q3) and resistor (R3) drop. However, drop on the Q3 is not enough and this value considered as horrible from my SP advisor. To solve this problem, my first approach is decreasing Rds(on) value of transistors and eliminate dc loss on the components. Addition to this, I learn that rule of thumb of choosing transistor of the system. This is like multiplication of gate charge and Rds(on) value of the transistor and consider in this sense. Thanks to this, we optimize switching loss and dc loss on the component. Gate charge will be my second approach.

I change Q3 transistors (C). Because of this, $R_{ds(on)}$ value decrease to $11\text{m}\Omega$ to $2\text{ m}\Omega$. This makes dissipation worst because current on this resistor increase dramatically, and addition to this, gate charge of this transistor is increase because of reverse relation as figure 14.

--- Efficiency Report ---			
Efficiency: 81.7%			
Input: 404W @ 17V Output: 330W @ 50V			
Ref.	I_{rms}	I_{peak}	Dissipation
Q2	9524mA	116445mA	12457mW
Q2B	9524mA	116445mA	12457mW
Q3	12478mA	131326mA	21424mW
Q3B	12478mA	131326mA	21424mW

Figure 15: important changes of efficiency report

To reduce dissipation, gate charge will be considered. To observe logic completely, I try extremely low gate charge transistor which is Fairchild BSS123. It has only 1nC gate charge, but 6Ω $R_{ds(on)}$ value. Result is not surprise design cannot reach to 50V output because of high resistance of the transistors as figure 15.

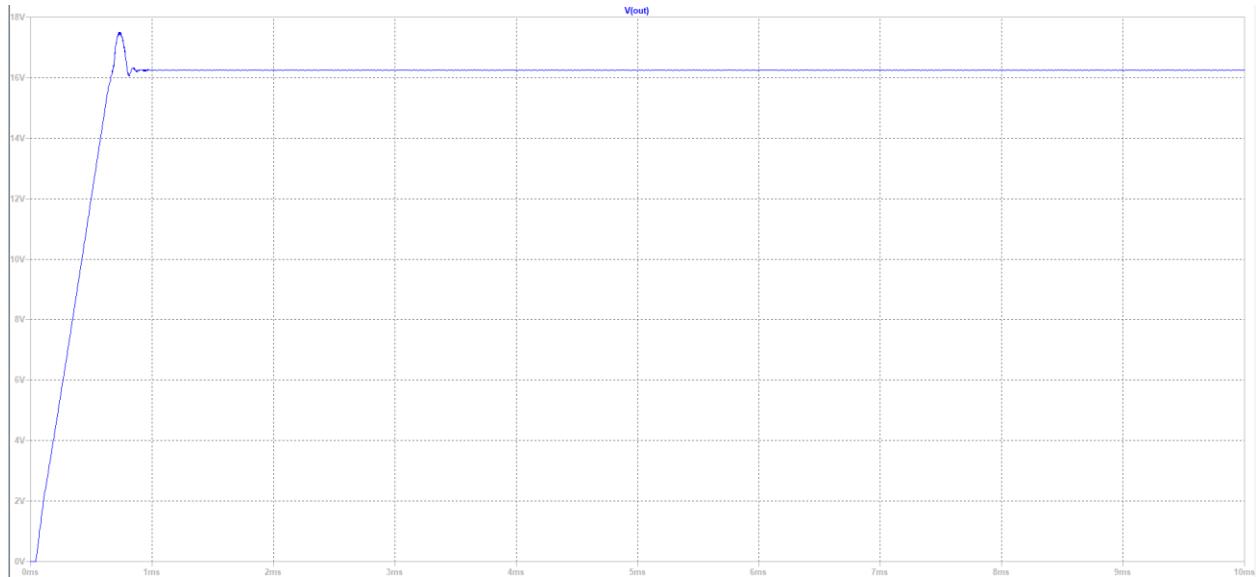


Figure 16: output wave form with low gate charge transistor combination

After these results, we decide that this operation frequency is not possible for our requirements. Therefore, we decrease the operation frequency, so I modified my design to 200KHz and 100KHz.

5.2. 100KHz DESIGN

a.) Inductor

According to equation (1), minimum value of Inductor is $14.45\mu\text{H}$. Therefore, I pick Inductor as $22\ \mu\text{H}$ because library of the LTspice options are limited, so most suitable one is that.

b.) Capacitor

Equation (2) gives me the $87\mu\text{F}$. Equation (3) is gives me the same result because equation terms are related to design requirements. Therefore, I choose $82\mu\text{F}$ and $150\text{m}\Omega$ ESR capacitor from library.

d.) Power MOSFETs

These equations are, also, related to design requirements, so results are same. Therefore, I use double transistors for Q2 and Q3.

e.) Sense Resistor

According to equation (7) and (8), $R_{\text{sense}} = 5.464 \text{ m}\Omega$

After these steps, my overall design looks like figure 18.

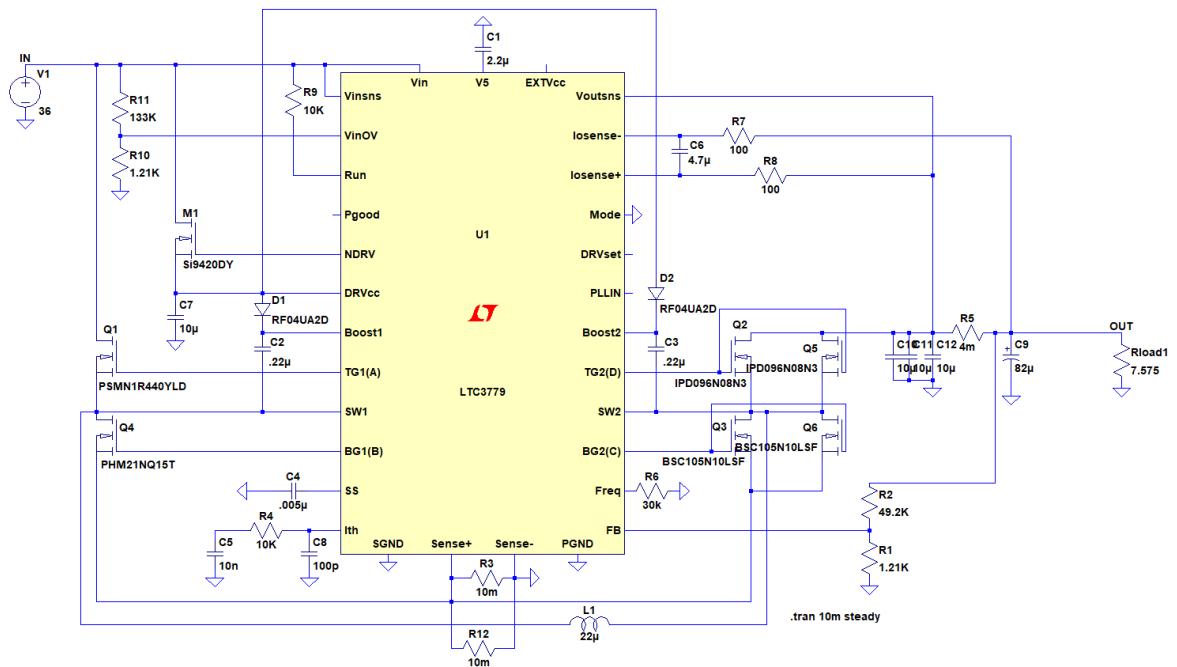


Figure 17: Overall 100KHz design

5.2.1 Simulation and Modifications

After selecting components, I start to simulations and obtain following results:

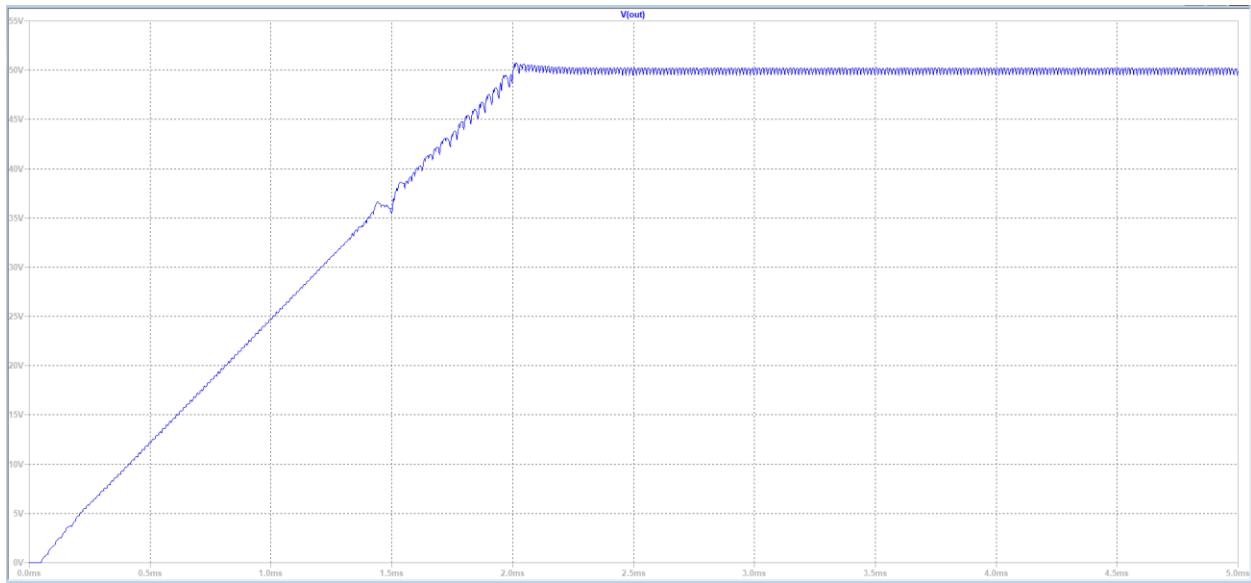


Figure 18: output waveform of 100KHz design

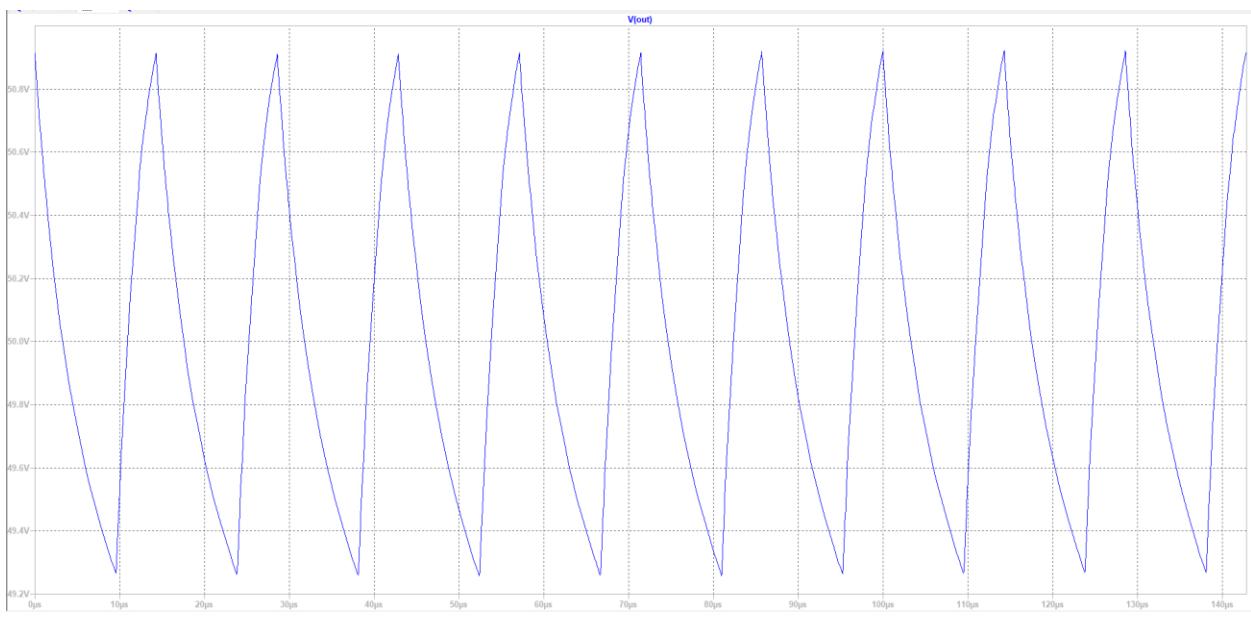


Figure 19: steady state output waveform of 100KHz design

--- Efficiency Report ---
Efficiency: 0.0%

Input: 339W @ 17V
Output: 0W @ 0V

Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	0mA	1mA	0mW
C3	50mA	1650mA	0mW
C4	0mA	0mA	0mW
C5	0mA	0mA	0mW
C6	0mA	0mA	0mW
C7	72mA	1790mA	0mW
C8	0mA	0mA	0mW
C9	3301mA	5896mA	1635mW
C10	2911mA	90208mA	0mW
C11	2911mA	90208mA	0mW
C12	2911mA	90208mA	0mW
D1	0mA	1mA	-0mW
D2	8mA	170mA	2mW
L1	20067mA	23617mA	1398mW
M1	11mA	16mA	90mW
Q1	20067mA	23809mA	379mW
Q2	5900mA	129082mA	341mW
Q3	8293mA	137216mA	1581mW
Q4	5mA	4468mA	0mW
Q5	5900mA	129082mA	341mW
Q6	8293mA	137216mA	1581mW
R1	1mA	1mA	1mW
R2	1mA	1mA	48mW
R3	8294mA	137525mA	688mW
R4	0mA	0mA	3µW
R5	7411mA	12619mA	220mW
R6	0mA	0mA	12µW
R7	0mA	0mA	0µW
R8	0mA	0mA	0µW
R9	0mA	0mA	0µW
R10	0mA	0mA	19µW
R11	0mA	0mA	2mW
R12	8294mA	137525mA	688mW
Rload1	6601mA	6722mA	330091mW
U1	108mA	2566mA	83mW

Figure 20: Efficiency Report of 100KHz design

Note: The previous report does not calculate output and efficiency. I cannot solve the problem, but by using report's values Rload1/Input = 97.35% is efficiency, and average of output is 50.001V.

When we analyze result of this design, load on transistors is solved (Q3 and Q6 has dissipation under 2W). This shows that problem is switching loss in 400KHz design. However, output voltage ripple is 1.65 V which should be 0.5V. To solve this problem, first approach is that I modify output capacitance. To see the results, I use .step param command and sweep the capacitance value from 100µF to 800 µF with 100 µF steps, and I obtain figure 21.

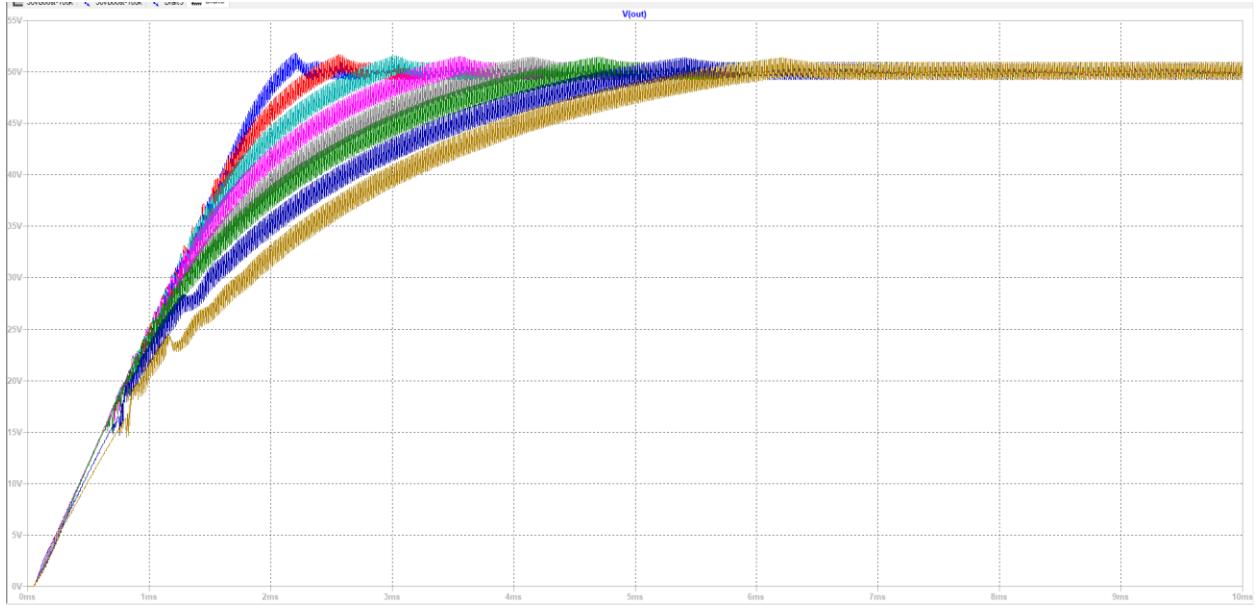


Figure 21: capacitance sweep from $100 \mu\text{F}$ to $800 \mu\text{F}$

According to figure 21, capacitance variation has no much effect on ripple. Therefore, to eliminate this, we should use low ESR capacitances, even to decrease ESR of capacitance, we can use parallel.

After using two parallel capacitors which have $470 \mu\text{F}$ and $20\text{m}\Omega$ ESR, figure 22 is obtained.

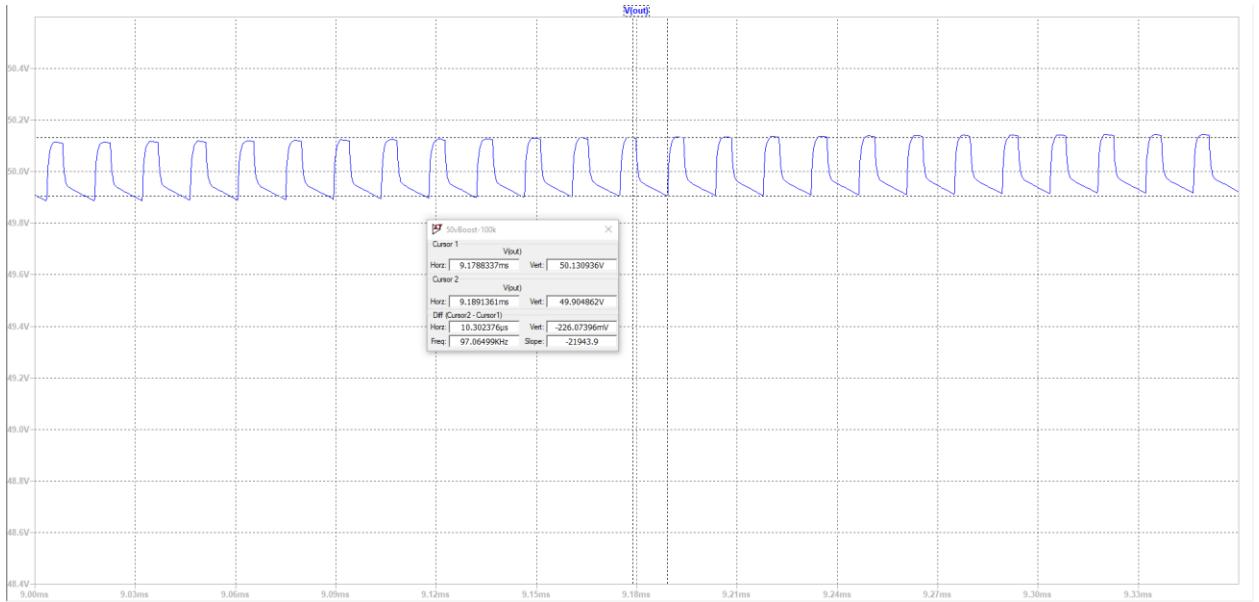


Figure 22: Modified 100KHz design

As we can see output voltage ripple decrease to 226mV which is enough. After this solution, Efficiency report is seen like figure 23.

--- Efficiency Report ---
Efficiency: 97.5%

Input: 338W @ 17V
Output: 330W @ 50V

Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	1407mA	91119mA	0mW
C3	0mA	1mA	0mW
C4	49mA	1638mA	0mW
C5	0mA	0mA	0mW
C6	0mA	0mA	0mW
C7	4210mA	7106mA	354mW
C8	0mA	0mA	0mW
C9	75mA	1787mA	0mW
C10	0mA	0mA	0mW
C11	1407mA	91119mA	0mW
C12	1407mA	91119mA	0mW
C13	4210mA	7106mA	354mW
C14	0mA	0mA	0mW
D1	8mA	167mA	2mW
D2	0mA	1mA	-0mW
L1	19934mA	23516mA	1376mW
M1	11mA	16mA	91mW
Q1	19934mA	23736mA	369mW
Q2	5755mA	128958mA	330mW
Q2B	5755mA	128958mA	330mW
Q3	8328mA	137086mA	1630mW
Q3B	8328mA	137086mA	1630mW
Q4	5mA	4326mA	-0mW
R1	1mA	1mA	1mW
R2	1mA	1mA	48mW
R3	8329mA	137396mA	694mW
R4	0mA	0mA	13μW
R5	10546mA	20829mA	445mW
R6	0mA	0mA	12μW
R7	0mA	0mA	3μW
R8	0mA	0mA	3μW
R9	0mA	0mA	0μW
R10	8329mA	137396mA	694mW
R11	0mA	0mA	19μW
R12	0mA	0mA	2mW
U1	108mA	2558mA	82mW

Figure 23: Efficiency report of the final 100KHz design

When we analyze values, in this frequency operations have high efficiency, which means low power dissipations. However, cost of this high efficiency is huge component sizes.

5.3. 200KHz DESIGN

a.) Inductor

According to equation (1), $L > 7.225\mu\text{H}$. Therefore, I pick Inductor as $10\mu\text{H}$ because library of the LTspice options are limited, so most suitable one is that in terms of current capability and resistance.

b.) Capacitor

Equation (2) gives me the $43.5 \mu\text{F}$. Equation (3) is gives me the same result because equation terms are related to design requirements. Therefore, I choose $47\mu\text{F}$ and $150\text{m}\Omega$ ESR capacitor from library.

a.) Power MOSFETs

These equations are, also, related to design requirements, so results are same. Therefore, I use double transistors for Q2 and Q3.

b.) Sense Resistor

According to equation (7) and (8), $R_{\text{sense}} = 5.255 \text{ m}\Omega$. To obtain required value and decrease the dissipation on single component, I used 2 resistors parallel.

After these steps, my overall design looks like figure 24.

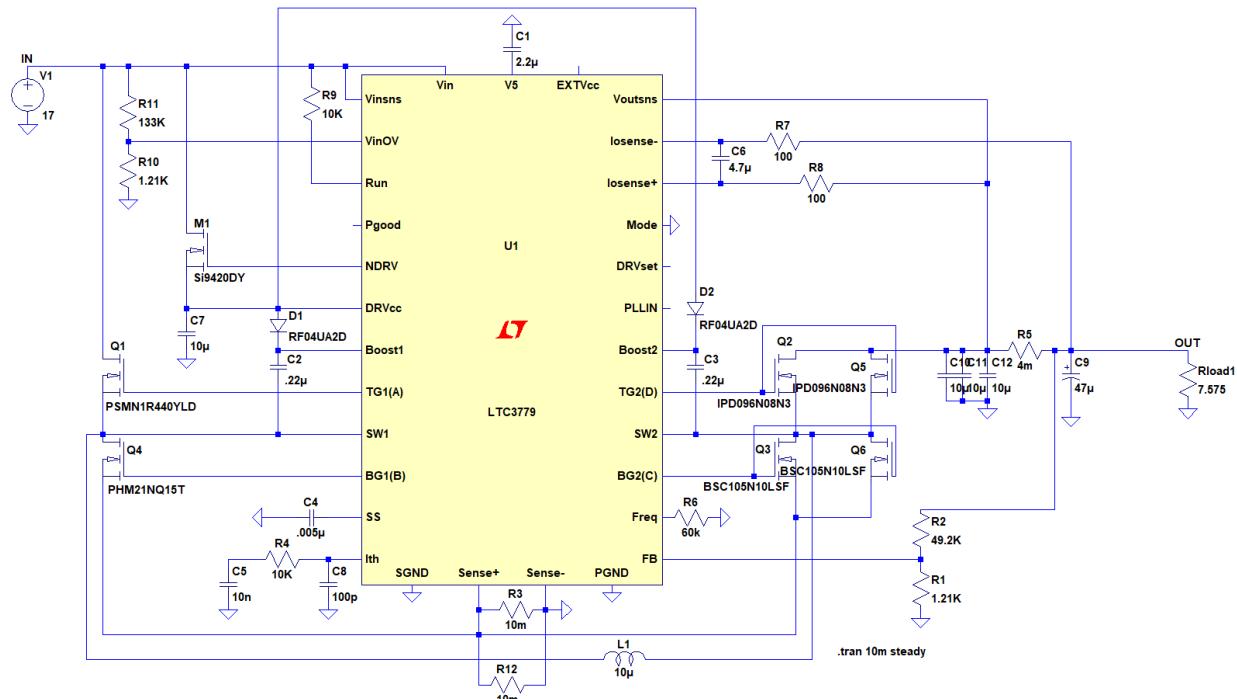


Figure 24: 200KHz overall design

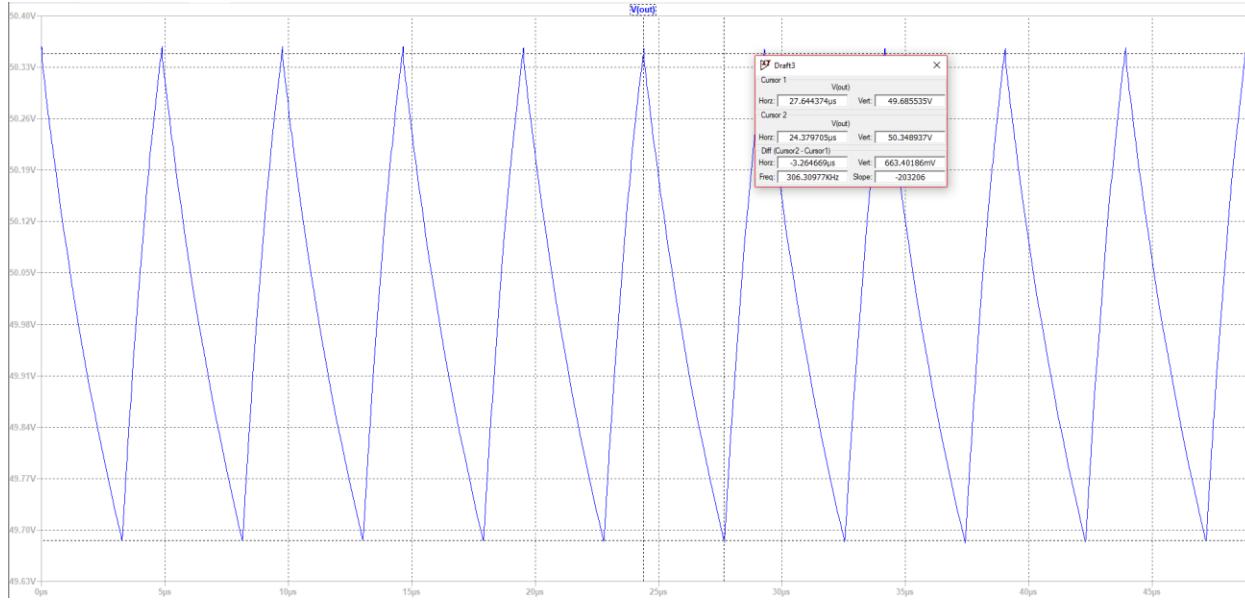


Figure 25: Steady state wave form of the figure 24

As the 100KHz design same ripple problem occurs (Voltage swing is around 663mV as we can see on the figure 25), so to solve this problem, I try to use the previous capacitor.

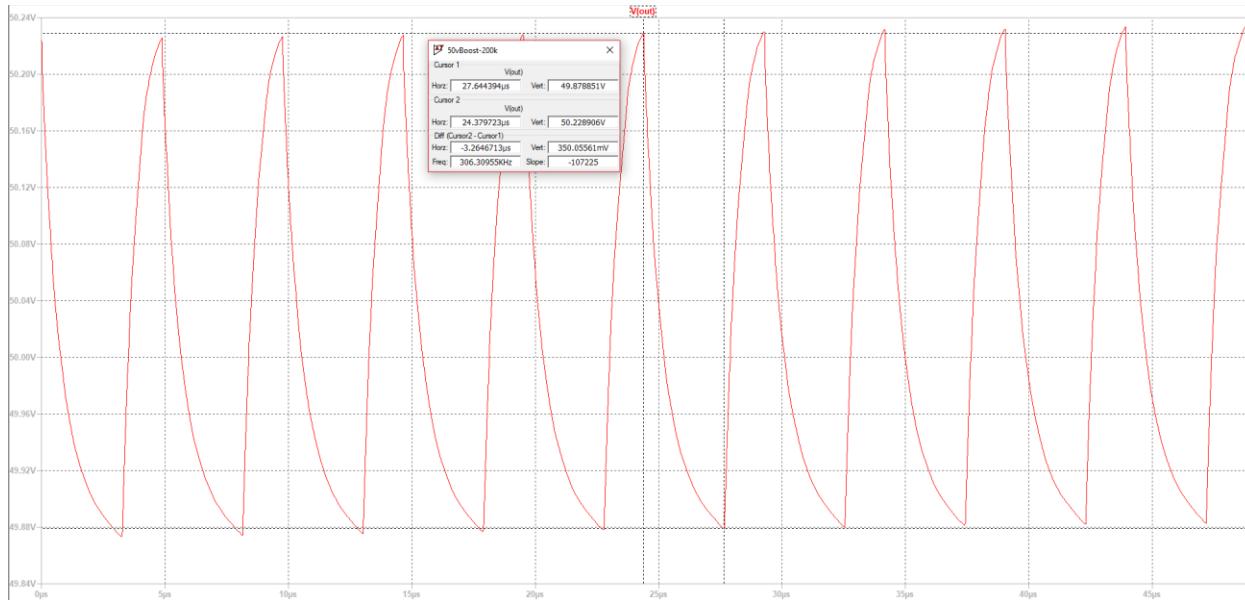


Figure 26: Solved ripple problem output wave form

--- Efficiency Report ---
Efficiency: 96.0%

Input: 344W @ 17V
Output: 330W @ 50V

Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	2846mA	95781mA	0mW
C3	0mA	1mA	0mW
C4	86mA	1643mA	0mW
C5	0mA	0mA	0mW
C6	0mA	0mA	0mW
C7	5966mA	10515mA	712mW
C8	0mA	0mA	0mW
C9	126mA	1781mA	0mW
C10	0mA	0mA	0mW
C11	2846mA	95781mA	0mW
C12	2846mA	95781mA	0mW
C14	0mA	0mA	0mW
D1	17mA	245mA	5mW
D2	0mA	1mA	0mW
L1	20594mA	23299mA	1780mW
M1	24mA	31mA	208mW
Q1	20594mA	23384mA	391mW
Q2	6293mA	135473mA	429mW
Q2B	6293mA	135473mA	429mW
Q3	8732mA	144371mA	3882mW
Q3B	8732mA	144371mA	3882mW
Q4	9mA	4791mA	0mW
R1	1mA	1mA	1mW
R2	1mA	1mA	48mW
R3	8735mA	144684mA	763mW
R4	0mA	0mA	2μW
R5	8989mA	17146mA	323mW
R6	0mA	0mA	24μW
R7	0mA	0mA	1μW
R8	0mA	0mA	1μW
R9	0mA	0mA	0μW
R10	8735mA	144684mA	763mW
R11	0mA	0mA	19μW
R12	0mA	0mA	2mW
U1	184mA	2558mA	165mW

Figure 27: Efficiency Report of 200KHz design without ripple problem

When we check dissipation results, Q3 and Q3B transistor pair over 2W dissipation. According to our previous discussion, it is problem for our design. However, when I talk with my supervisor, He said we can check practical result under these conditions because it was worst case result, and he, also, say this result can tolerate on the card.

After this point, I consider overshoot and undershoot characteristic of the design. It is important because load can be sensitive about voltage swing over or under cases. To improve overshoot and undershoot of the design, a capacitor connected parallel to RFB1 resistor. Thanks to this capacitor, feedback pins voltage changes smoother, so output stability increase. I sweep the capacitor value from 10pF to 40pF with 5pF increment and I obtain the following results.

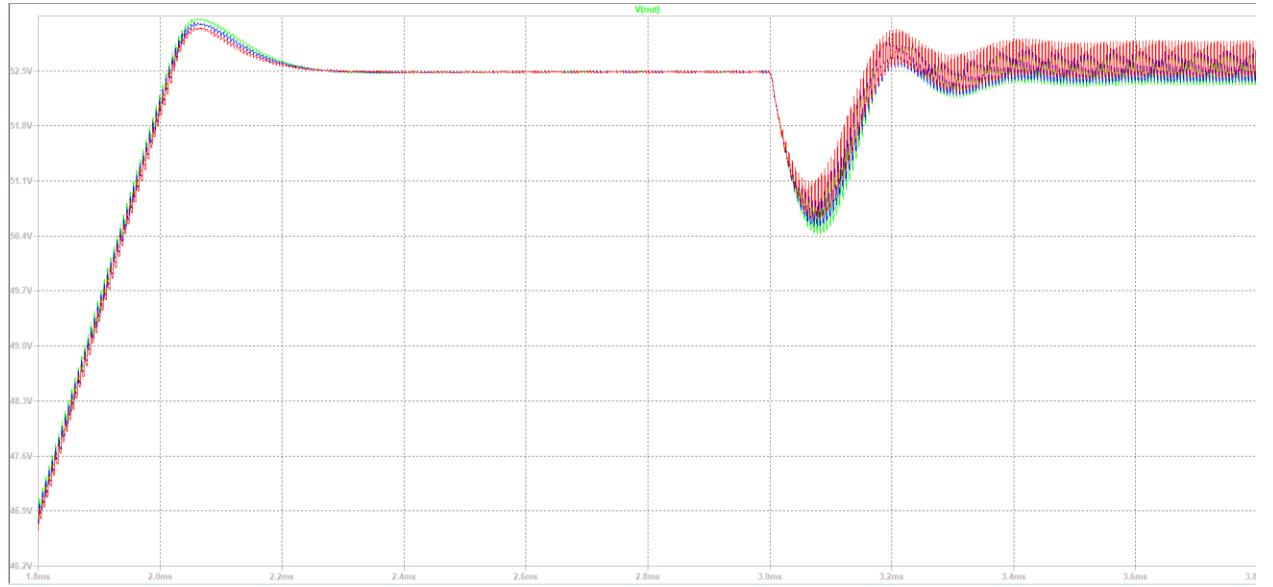


Figure 28: Overshoot and Undershoot at the output for capacitor values from 10pF to 20pF

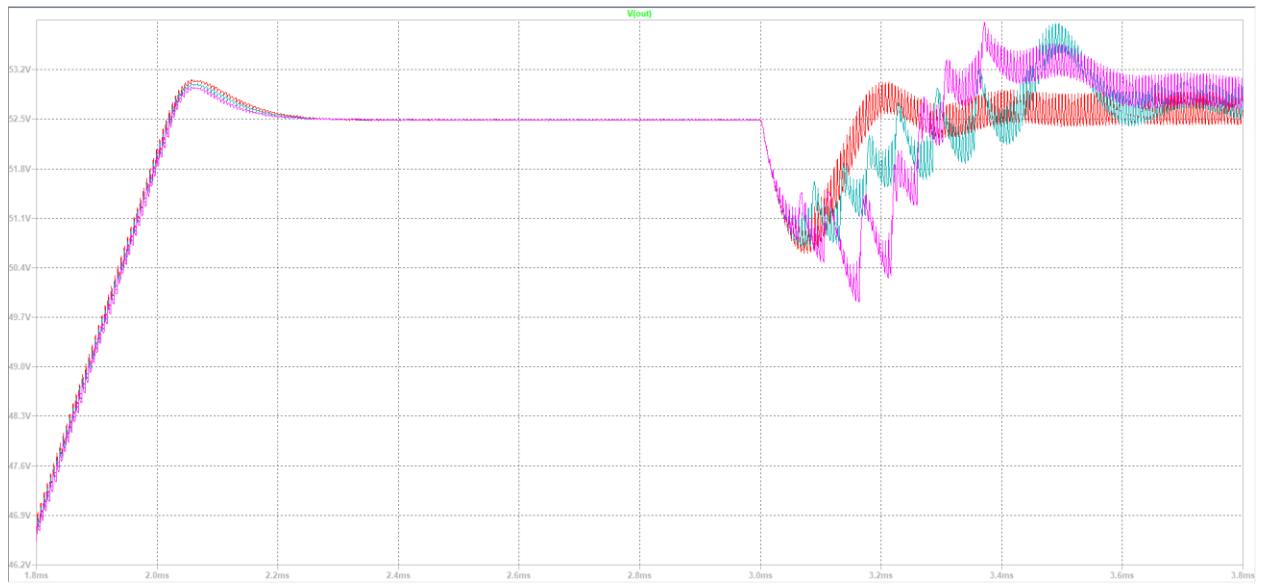


Figure 29: Overshoot and Undershoot at the output for capacitor values from 20pF to 30pF

As we can see from figure 28 and figure 29, increasing up to 20pF is increase output voltage swing performance, but after this point we lose stability of the system, and steady state swings. According to this result, 20pF is the most suitable choice.

After these simulation result, I start to work on demo board for experimental analysis of the IC.

5.4. Experimental Analysis

In this section, I work on demo board, and obtain experimental data. I start to check demo board design and how to modify it to my design requirements because I do not want to change many components on the board. First, check demo board design in figure 30 and figure 31.

To obtain 50V output, I change resistor RFB1 and RFB2. In previous chapter, I used $492\text{K}\Omega$ and $12.1\text{K}\Omega$ or $49.2\text{K}\Omega$ and $1.21\text{K}\Omega$ (These choices are made according to data sheet. Formula is $V_{out}=1.2V * (1+RFB1/RFB2)$). However, $472\text{K}\Omega$ is not in the stock, so I need to change values according to formula. Therefore, closest pair was $470\text{K}\Omega$ and $11\text{K}\Omega$. Unfortunately, this pair gives 52.5V output. Result of this, output power increase to 346.5W. Also, R22 and R25 are changed. They are related with $V_{in OV}$, which is an important property of IC. This voltage division resistors decide at which level IC shut itself down to prevent circuit from over voltage. They are changed to $61\text{K}\Omega$ and $1.21\text{K}\Omega$ respectively. Thanks to this combination, over voltage level is set to 66 V. R30 and R31 resistors are, also, changed to set minimum input voltage. When we check the schematic (front), we see that these resistors' voltage division connected to the run pin, so they decided to opening voltage of the IC. They are changed to $22\text{K}\Omega$ and $3\text{K}\Omega$ respectively. Thanks to that, IC can open at the level of 10 V. After these modifications, demo board can be used for our output requirements.

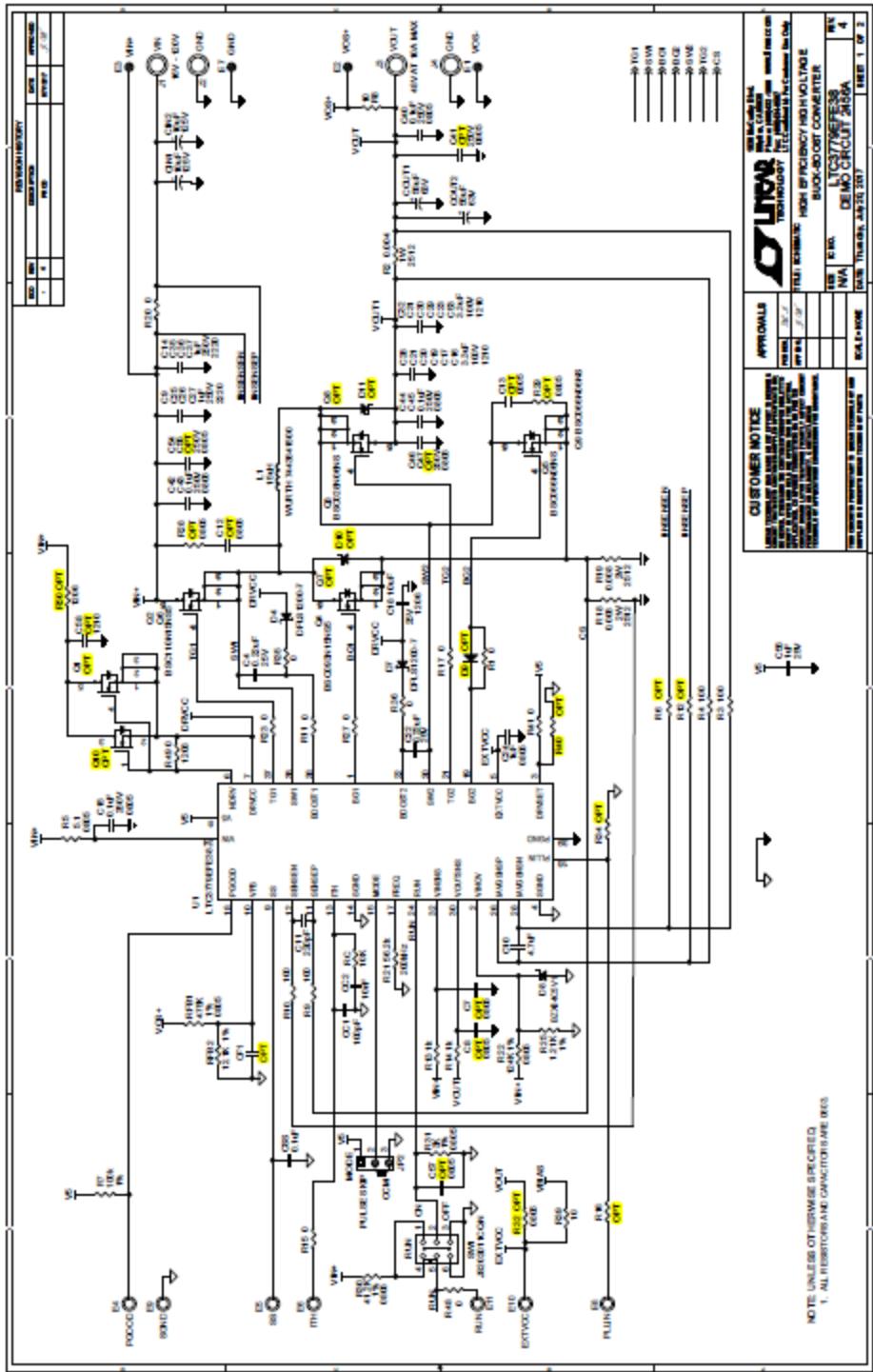


Figure 30: Demo board schematic diagram top

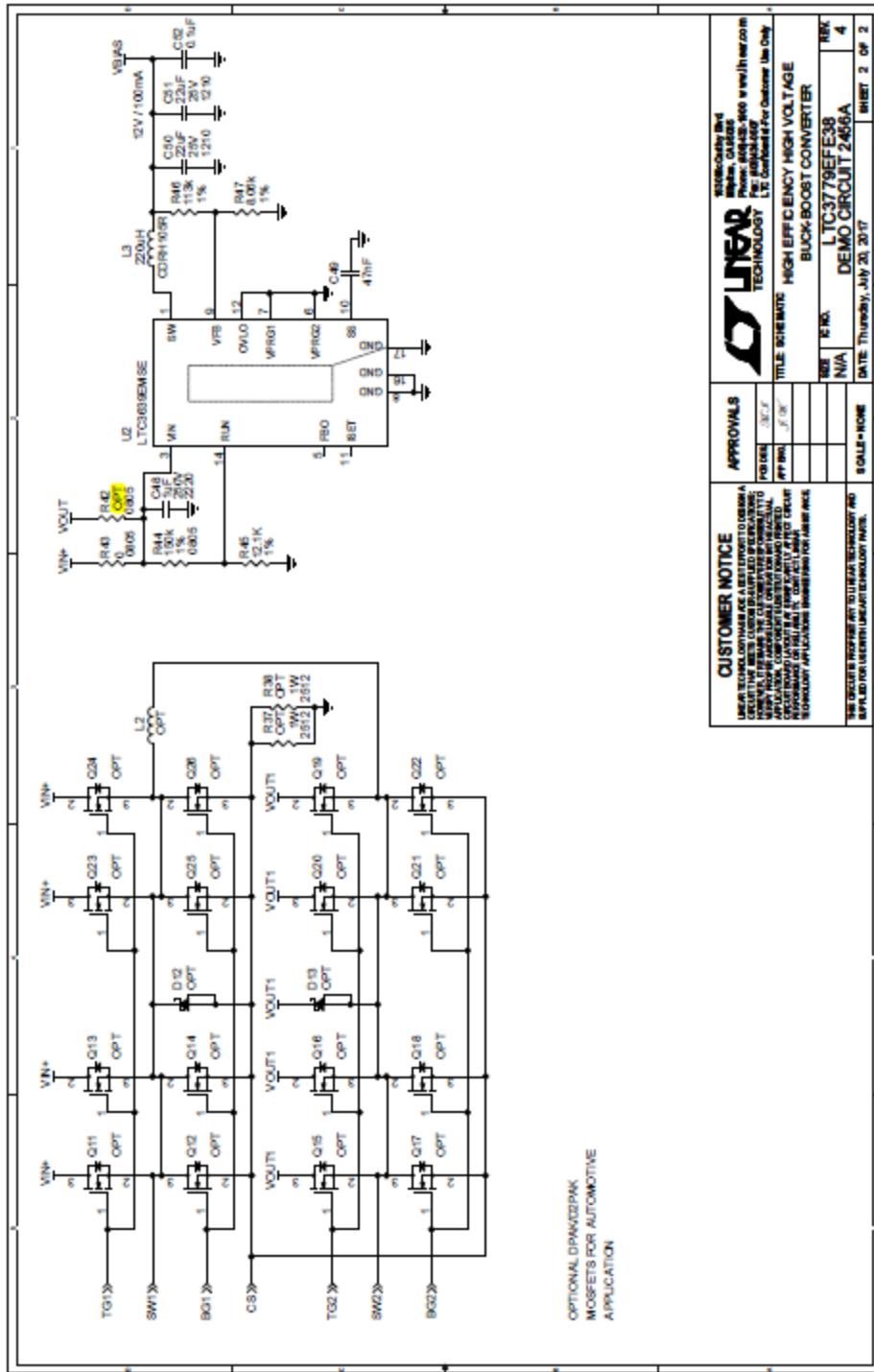


Figure 31: Demo board schematic diagram bottom

To make test systematically, we prepare a test document just like engineers do in here. Thanks to that, keeping test result is simple and practical. Test document have 8 column which represent test number, test, process, mode, load, expected results, measured results and additionally modified results (the last column adds to compare modification). The table of the test document is the following pages (x-x).

The eighth column's difference is switching MOSFETs are changed to what is planning to use. After this change, we can observe how suitable these MOSFETs which are CSD18563Q5A. These MOSFETs are chosen according to rule of thumb, and already verified in many designs.

As we can see from figure 31, EXTVCC pin is powered by 12V, so to see the effect of this pin, we change the power to 6.5V. This value is selected because in real design, they consider using this value from another converter.

Test Number	Test	Process	Mode	Yük	Beklenen sonuç	Ölçüm sonucu	Ölçüm sonuçları-2 (New Mos)
1	Mode Control	Measuring Input voltage	Floating	0	<10 mA	1 mA	
2	Mode Control	Measuring Input current	Floating	0	< 0.1 V	0	
3	System initial check	Measuring input current	Forced Continuous	0	< 100 mA	34 mA	50mA/70mA/10mA/130mA/200mA
4	Run	Measuring Voltage on the run pin	Forced Continuous	0	>1.2 V	1.6 V	
5	Input Voltage	Measuring Input voltage	Forced Continuous	0	17-36V	24	
6	Output Voltage	Measuring output voltage	Forced Continuous	0	52-54 V	52.9 V	52.9 V
7	Gate Waveform	Measuring Waveform on the Gate Q5	Forced Continuous	0	4.5-6.65 V	20 Vpp	
8	Gate Waveform	Measuring Waveform on the Gate Q9	Forced Continuous	0	4.5-6.65 V	20 Vpp	
9	Ovvoltage Protection (66.7V)	Output Voltage	Forced Continuous	0	0	0	
10	Feedback voltage	RFB2 Bacağı	Forced Continuous	0	1.2	xxx	
11	Output Voltage	Measuring output voltage for 17 V = Vin	Forced Continuous	1A	52-54 V	52.9 V	52.9 V
12	Gate Waveform	Measuring Waveform on the Gate Q5 for 17 V = Vin	Forced Continuous	1A	5-15 V	11.25 V	
13	Gate Waveform	Measuring Waveform on the Gate Q9 for 17 V = Vin	Forced Continuous	1A	5-15 V	11.25 V	

14	Efficiency	Measuring Efficiency for 17 V = Vin (EXTVCC=12V)	Forced Continuous	1A	>95,5	90.19	
15	Efficiency	Measuring Efficiency for 17 V = Vin (EXTVCC=6.5V)	Forced Continuous	1A	>95,5	90.15	89.18
16	Output Voltage	Measuring output voltage for 24 V= Vin	Forced Continuous	1A	52-54 V	52,9 V	52.9 V
17	Gate Waveform	Measuring Waveform on the Gate Q5 for 24 V= Vin	Forced Continuous	1A	5-15 V	10.5 V	
18	Gate Waveform	Measuring Waveform on the Gate Q9 for 24 V= Vin	Forced Continuous	1A	5-15 V	10.5 V	
19	Efficiency	Measuring Efficiency for 24 V = Vin	Forced Continuous	1A	>95,5	90.33	89.14
21	Output Voltage	Measuring output voltage for 36 V= Vin	Forced Continuous	1A	52-54 V	52,9 V	52.9 V
22	Gate Waveform	Measuring Waveform on the Gate Q5 for 36 V= Vin	Forced Continuous	1A	5-15V	10.5 V	
23	Gate Waveform	Measuring Waveform on the Gate Q9 for 36 V= Vin	Forced Continuous	1A	5-15V	10.5 V	
24	Efficiency	Measuring Efficiency for 36 V= Vin	Forced Continuous	1A	>95,5	92.16	90.63
26	Efficiency	Measuring Efficiency for 17 V = Vin	Forced Continuous	2A	>95,5	93.18	93.28
28	Output Voltage	Measuring output voltage for 17 V = Vin	Forced Continuous	2A	52-54 V	52,9 V	52.8 V
29	Efficiency	Measuring Efficiency for 24 V= Vin	Forced Continuous	2A	>95,5	94.4	94.11
31	Output Voltage	Measuring output voltage for 24 V= Vin	Forced Continuous	2A	52-54 V	52,9 V	52.9 V
32	Efficiency	Measuring Efficiency for 36 V= Vin	Forced Continuous	2A	>95,5	95.05	94.74
34	Output Voltage	Measuring output voltage for 36 V= Vin	Forced Continuous	2A	52-54 V	52,9 V	52.9 V

35	Output Voltage	Measuring output voltage for 17 V = Vin	Forced Continuous	3A	52-54 V	52,9 V	52.9 V
36	Gate Waveform	Measuring Waveform on the Gate Q5 for 17 V = Vin	Forced Continuous	3A	5-15V	9,88 V	
37	Gate Waveform	Measuring Waveform on the Gate Q9 for 17 V = Vin	Forced Continuous	3A	5-15V	9,88 V	
38	Efficiency	Measuring Efficiency for 17 V = Vin	Forced Continuous	3A	>95,5	93.93	94.86
40	Output Voltage	Measuring output voltage for 24 V= Vin	Forced Continuous	3A	52-54 V	52,9 V	52.9 V
41	Gate Waveform	Measuring Waveform on the Gate Q5 for 24 V= Vin	Forced Continuous	3A	5-15V	10.4 V	
42	Gate Waveform	Measuring Waveform on the Gate Q9 for 24 V= Vin	Forced Continuous	3A	5-15V	10.4 V	
43	Efficiency	Measuring Efficiency for 24 V= Vin	Forced Continuous	3A	>95,5	95.28	95.53
45	Output Voltage	Measuring output voltage for 36 V= Vin	Forced Continuous	3A	52-54 V	52,9 V	52.9 V
46	Gate Waveform	Measuring Waveform on the Gate Q5 for 36 V= Vin	Forced Continuous	3A	5-15V	10.4 V	
47	Gate Waveform	Measuring Waveform on the Gate Q9 for 36 V= Vin	Forced Continuous	3A	5-15V	10.4 V	
48	Efficiency	Measuring Efficiency for 36 V= Vin	Forced Continuous	3A	>95,5	96.26	95.81
50	Efficiency	Measuring Efficiency for 17 V = Vin	Forced Continuous	4A	>95,5	93.88	94.99
52	Output Voltage	Measuring output voltage for 17 V = Vin	Forced Continuous	4A	52-54 V	52,9 V	52.8 V
53	Efficiency	Measuring Efficiency for 24 V= Vin	Forced Continuous	4A	>95,5	95.73	96.11
55	Output Voltage	Measuring output voltage for 24 V= Vin	Forced Continuous	4A	52-54 V	52,9 V	52.9 V

56	Efficiency	Measuring Efficiency for 36 V= Vin	Forced Continuous	4A	>95,5	96.73	96.89
58	Output Voltage	Measuring output voltage for 36 V= Vin	Forced Continuous	4A	52-54 V	52,9 V	52.9 V
59	Output Voltage	Measuring output voltage for 17 V = Vin	Forced Continuous	6.6A	52-54 V	52,8 V	52.9 V
60	Gate Waveform	Measuring Waveform on the Gate Q5 for 17 V = Vin	Forced Continuous	6.6A	5-15V	10.62 5 V	
61	Gate Waveform	Measuring Waveform on the Gate Q9 for 17 V = Vin	Forced Continuous	6.6A	5-15V	10.62 5 V	
62	Efficiency	Measuring Efficiency for 17 V = Vin(EXTVCC = 12 V)	Forced Continuous	6.6A	>95,5	94.77	
63	Efficiency	Measuring Efficiency for 17 V = Vin (EXTVCC=6.5V)	Forced Continuous	6.6A	>95,5	95.5	93.96
64	Output Voltage	Measuring output voltage for 24 V= Vin	Forced Continuous	6.6A	52-54 V	52,9 V	52.9 V
65	Voltage on R2	Measuring Voltage on the R2 for 24 V= Vin	Forced Continuous	6.6A	4,2-4,8 mV	27 Mv	
66	Gate Waveform	Measuring Waveform on the Gate Q5 for 24 V= Vin	Forced Continuous	6.6A	4,2-6,2 V	11 V	
67	Gate Waveform	Measuring Waveform on the Gate Q9 for 24 V= Vin	Forced Continuous	6.6A	4,2-6,2 V	11 V	
68	Efficiency	Measuring Efficiency for 24 V= Vin(EXTVCC = 12 V)	Forced Continuous	6.6A	>95,5	96.12	
69	Efficiency	Measuring Efficiency for 24 V= Vin (EXTVCC= 6.5 V)	Forced Continuous	6.6A	>95,5	96.9	96.33
70	Output Voltage	Measuring output voltage for 36 V= Vin	Forced Continuous	6.6A	52-54 V	52,9 V	52.9 V
71	Gate Waveform	Measuring Waveform on the Gate Q5 for 36 V= Vin	Forced Continuous	6.6A	4,2-6,2 V	10.12 5 V	
72	Gate Waveform	Measuring Waveform on the Gate Q9 for 36 V= Vin	Forced Continuous	6.6A	4,2-6,2 V	10.12 5 V	

73	Efficiency	Measuring Efficiency for 36 V= Vin (EXTVCC = 12 V)	Forced Continuous	6.6A	>95,5	97.26	
74	Efficiency	Measuring Efficiency for 36 V= Vin (EXTVCC = 6.5 V)	Forced Continuous	6.6A	>95,5	97.65	94.44
75	Component Pictures	Thermal Camera	Forced Continuous	6.6A			
Test Number	Test	Process	Mode	Yük	Beklenen sonuç	Ölçüm sonucu	Ölçüm sonuçları-2 (New Mos)
1	Efficiency	Measuring Efficiency for 10.5 V = Vin	Forced Continuous	2A	>95,5	87.9	91.5
3	Output Voltage	Measuring output voltage for 10.5 V = Vin	Forced Continuous	2A	52-54 V	52.8	52.9
4	Efficiency	Measuring Efficiency for 15 V= Vin	Forced Continuous	2A	>95,5	93.93	92.97
6	Output Voltage	Measuring output voltage for 15 V= Vin	Forced Continuous	2A	52-54 V	52.9	52.9
7	Efficiency	Measuring Efficiency for 10.5 V = Vin (EXTVCC = 12 V)	Forced Continuous	4A	>95,5	91.95	
8	Efficiency	Measuring Efficiency for 10.5 V = Vin (EXTVCC=6.5V)	Forced Continuous	4A	>95,5	92.06	89.98
9	Output Voltage	Measuring output voltage for 10.5 V = Vin	Forced Continuous	4A	52-54 V	52.8	52.9
10	Efficiency	Measuring Efficiency for 15 V= Vin (EXTVCC = 12 V)	Forced Continuous	4A	>95,5	95.11	
11	Efficiency	Measuring Efficiency for 15 V= Vin (ExtVCC= 6.5V)	Forced Continuous	4A	>95,5	95.35	94.41
12	Output Voltage	Measuring output voltage for 15 V= Vin	Forced Continuous	4A	52-54 V	52.9	52.9

During tests, I took thermal pictures of the card to see thermal issues and performance. The thermal pictures are at the appendix.

After this part, I check output waveform from oscilloscope in the conditions which are steady state, undershoot, and, and I obtain following figures.

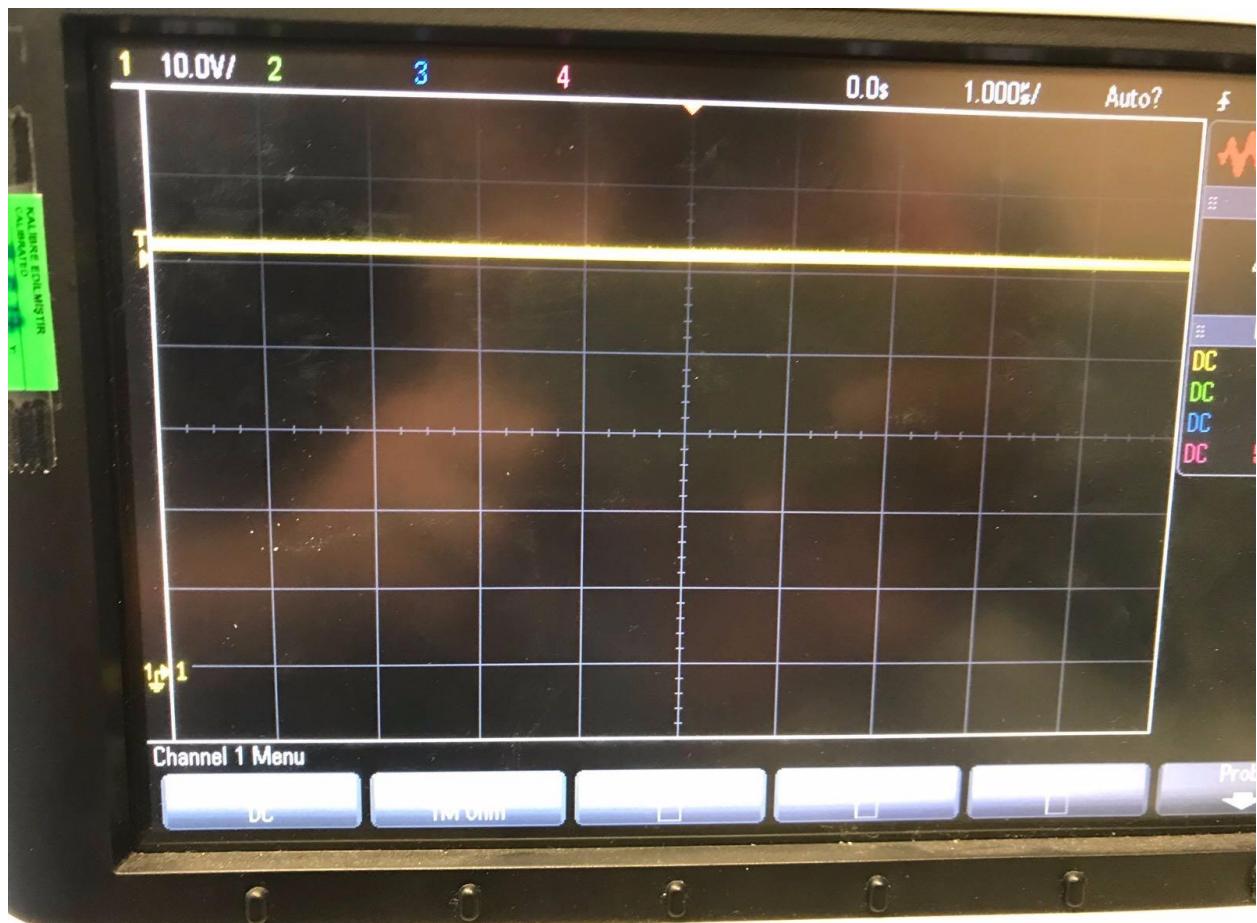


Figure 32: output waveform at 24V input

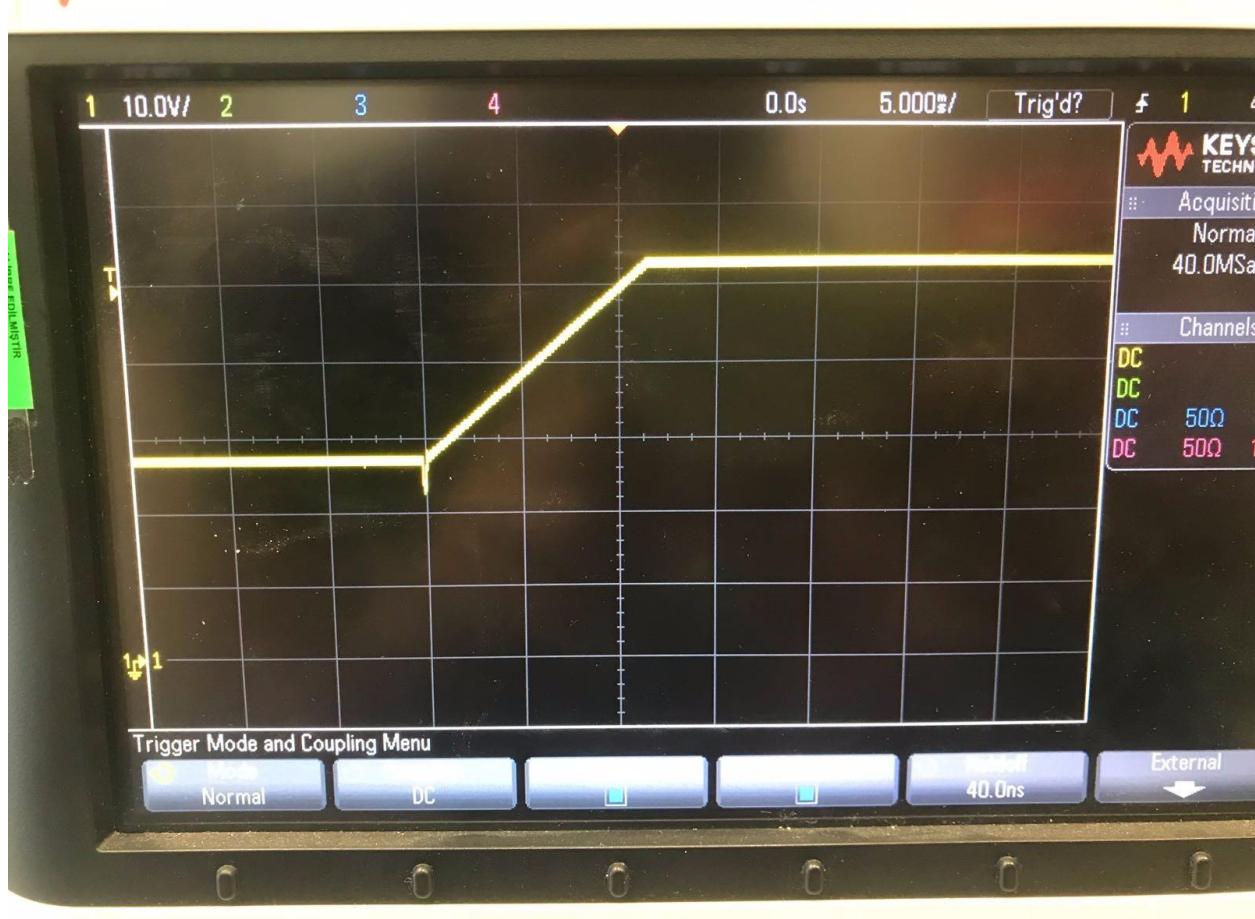


Figure 33: Output waveform up to steady state

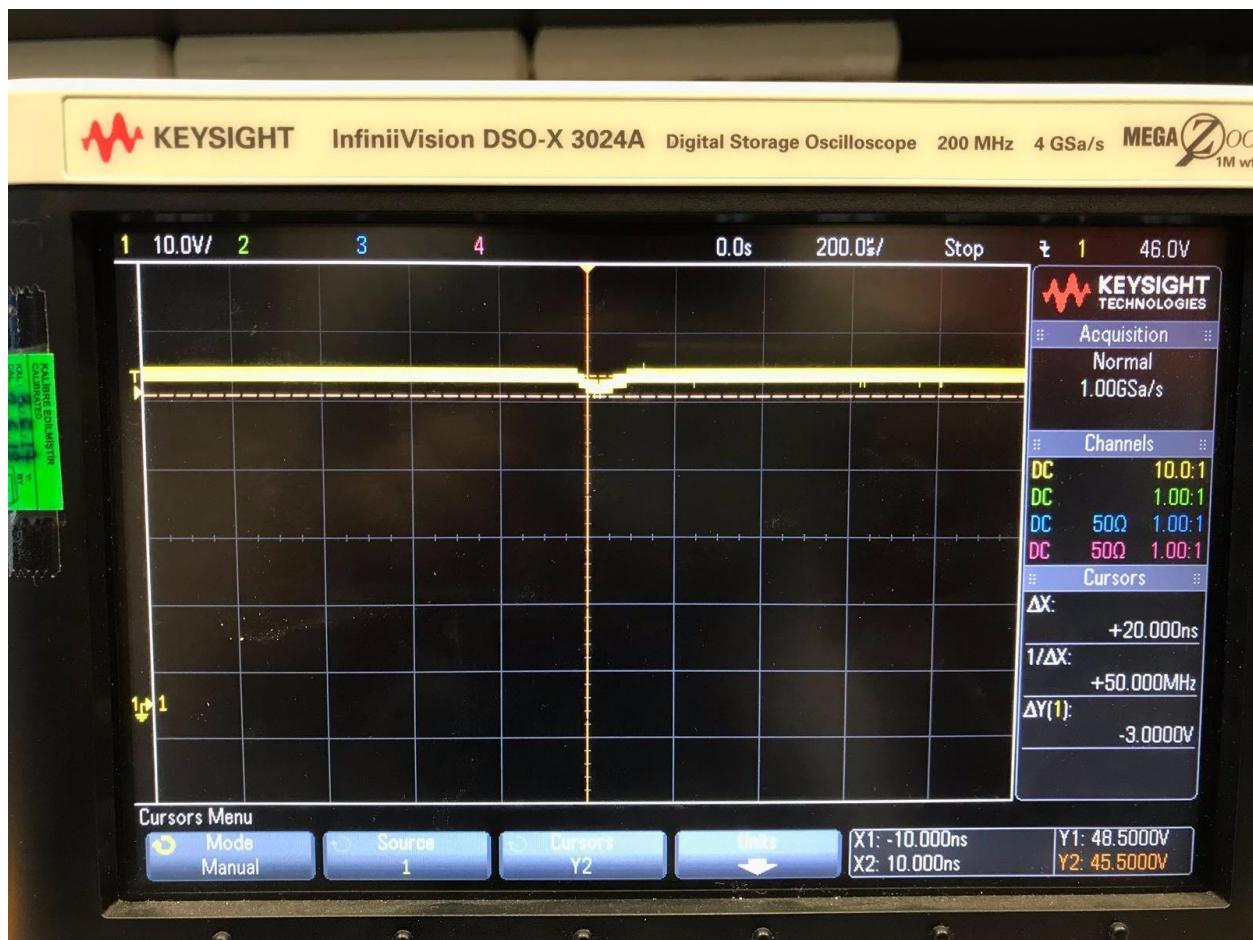


Figure 34: 6.6A load undershoot with 24V input

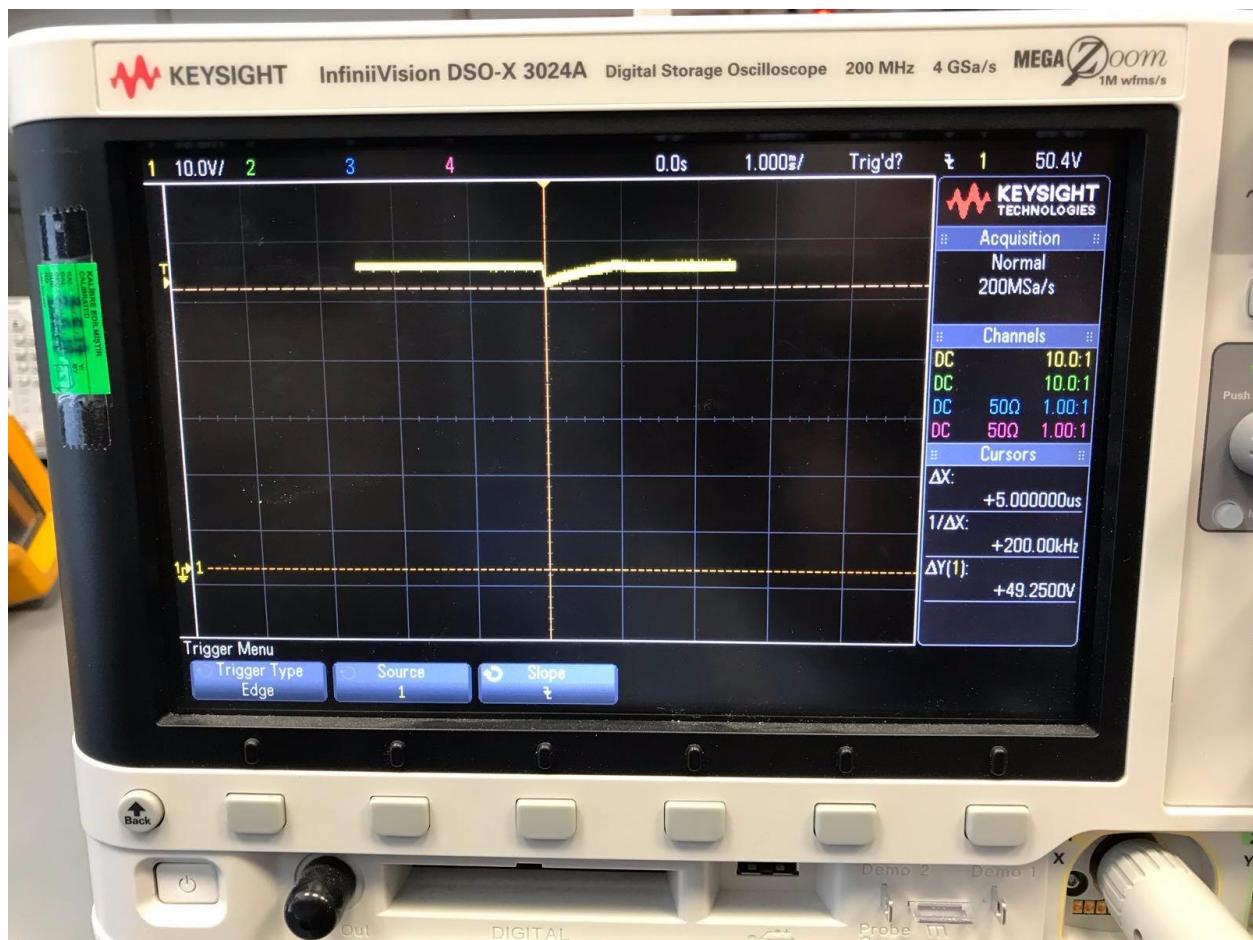


Figure 35: 6.6A load undershoot with 17V input

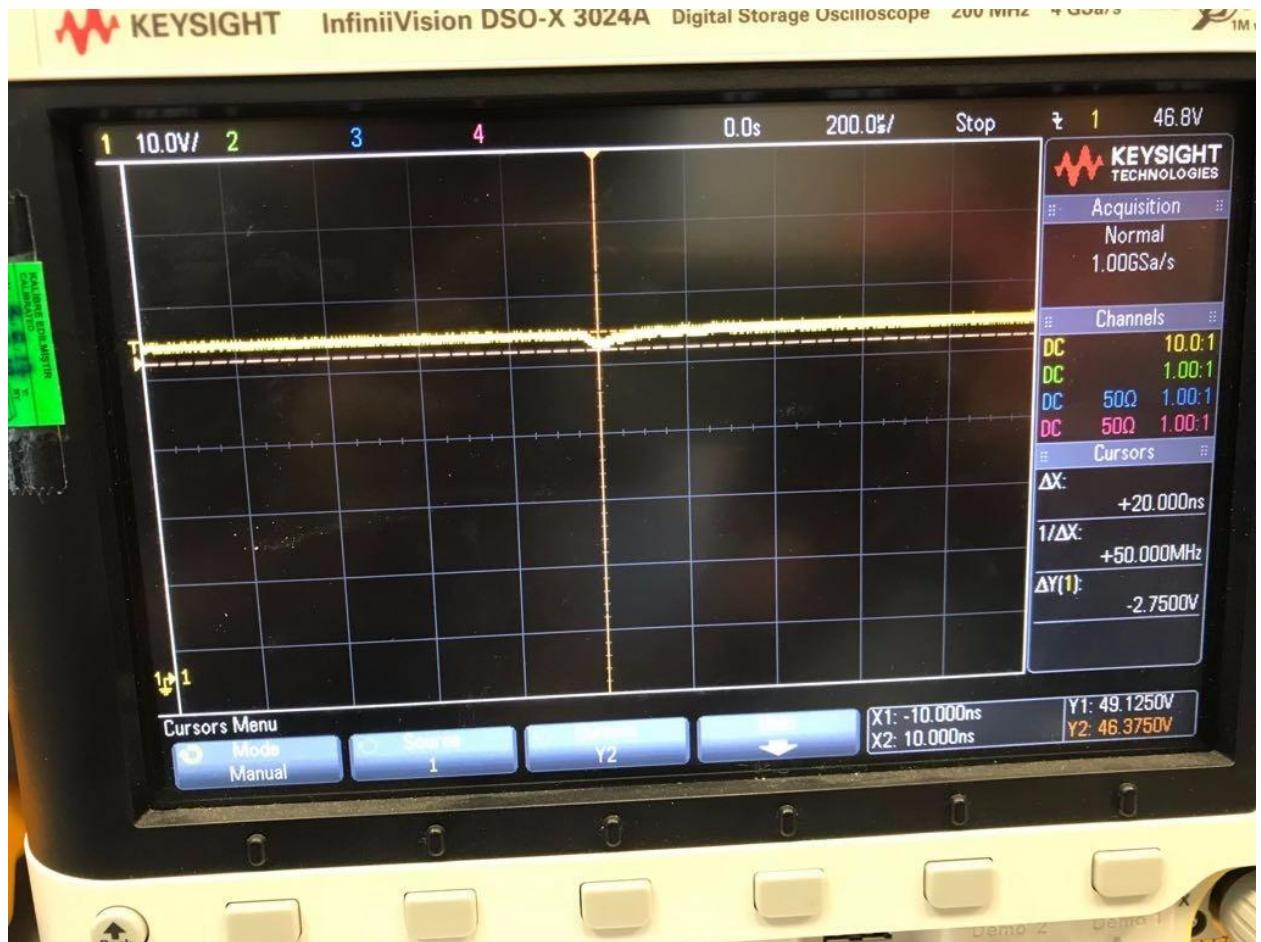


Figure 36: 6.6A load undershoot with 24V input with 220pF capacitor

When we compare figure 34 and figure 36, we can see the effect of the capacitor on the undershoot performance. It gives us 0.25 V decrease which is a good result.

Additional to these tests, we make spectral test to see the output noise frequencies of the design. Related pictures of this test are at the appendix.

Also, Demo board have additional larger package MOSFET slots to reduce pressure on the switching MOSFETs, especially for motor drive purposes, we try to use these parts. Thanks to that, we increase the package and heat loss on the MOSFETs, and we try to use heat sink (pictures of this are in the appendix). Although the idea seems good, in practice, there is no significant change because this bigger MOSFETs specs are worse than small ones. Therefore, we lose what we gain from other side. However, when we use heat sink with CSD MOSFETs, we obtain important drop (around 10-degree Celsius) drop on the MOSFETs whose pictures can be seen in the appendix.

After these results, efficiency and performance of the converter is well. Especially, when input is higher than 17V efficiency of the IC and converter is around 90% or more. However, when input range is

lower than 17 V, efficiency is not that high and overall design has heat problems. All in all, the overall design gives what is required with high efficiency, and task has been achieved.

6. Vin = 10.5-36 V, O/P 22 V 145W Buck-Boost Dc-Dc converter

Another design of my SP is 22V/145W Buck-Boost converter. In this design, I use full specs of the given IC. This part has no practical analysis and tests because I left no time to test this design, but due to lower output requirement, according to simulations, I did not face the previous problems.

Requirements:

$$V_{in} = 10.5-36 \text{ V}$$

$$V_{out} = 22\text{V}/6.6\text{A}$$

$$f_s = 250-500 \text{ KHz}$$

$$\Delta V_{ripple} = V_{out}/100$$

As the previous case, I select to frequency 400KHz because I make both design at the same time by selecting same frequency makes my calculations easy.

6.1. Component Selection

As the previous case, I make my choices according to formulas from datasheets. However, in this case, I need to consider buck case, also. Therefore, I choose which is limitation factor for design.

a.) Inductor

$$L_{BUCK} > \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT}) \cdot 100}{f \cdot I_{OUT(MAX)} \cdot \%Ripple \cdot V_{IN(MAX)}} \text{ H} \quad (9)$$

Equation (9) is gives the minimum value of the Inductor. In this equation, I choose Ripple is 40% same as the boost case. After calculation, result is $L > 7.74 \mu\text{H}$. After this result, I pick $L = X \mu\text{H}$ because it was the closest value of my calculation and small value means small size.

As the previous design current rating and serial resistance are, also, important factor for choosing correct Inductor.

b.) Capacitor

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8 \cdot f \cdot C_{OUT}} \right) \quad (10)$$

Equation (10) is the buck mode ripple equation. However, there are two parameter and one equation for buck case, so I choose capacitors for boost case by using equations (2) and (3). After solving them, results are $C=89 \mu F$ and $ESR=33m\Omega$.

c.) Power MOSFET

While choosing these components, I consider $R_{ds(on)}$ value which is related with current loss. For boost region, main load is on the MOSFET A, C and D and MOSFET, so we consider their values.

$$P_{B,BUCK} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \cdot I_{OUT(MAX)}^2 \cdot P_\tau \cdot R_{DS(ON)} \quad (11)$$

When we look at the datasheet, there is only B transistor has Buck oriented equation, so others should be selected according to equations (4), (5) and (6). When we solve the equations, we obtain following results;

$$R_{ds(on), A} < 1.35 m\Omega, \text{ (same as previous design)}$$

$$R_{ds(on), B} < 15.56 m\Omega$$

$$R_{ds(on), D} < 1.92 m\Omega$$

Different from previous case, $R_{ds(on), D}$ is drop significantly from $9.94 m\Omega$ to $1.92 m\Omega$. This shows that main load will be on this transistor during operation. According to results, I can choose same transistor for A, B, and C, but I need to change D.

d.) Sense Resistor

$$R_{SENSE(MAX,BUCK)} = \frac{2 \cdot V_{SENSE(MAX,BUCK,MINDC)}}{(2 \cdot I_{OUT(MAX,BUCK)}) - \Delta I_{L(MIN,BUCK)}} \Omega \quad (12)$$

$$\Delta I_{L,BUCK} = \frac{V_{OUT}}{f \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \quad (13)$$

According to equation (12) and (13), $R_{sense} = 7 m\Omega$. However, when we calculate for boost region by using equation (7) and (8), we obtain $4.257 m\Omega$. Therefore, I choose $4.2 m\Omega$ for sense resistor.

The main components are selected by these methods from library of the LTspice after this part my design shapes like figure 37.

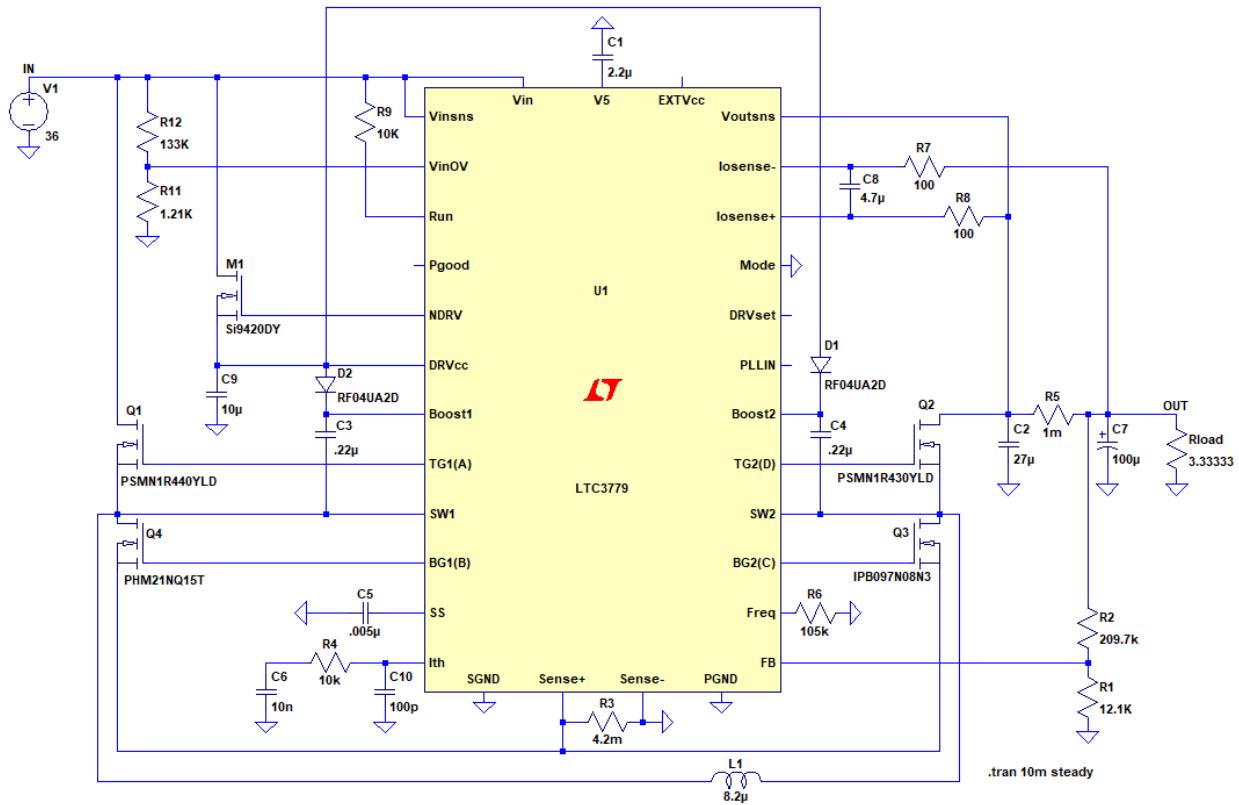


Figure 37: Overall design

6.1.1 Simulation and Modifications

I start with output analysis of the design, and I obtain following waveforms;

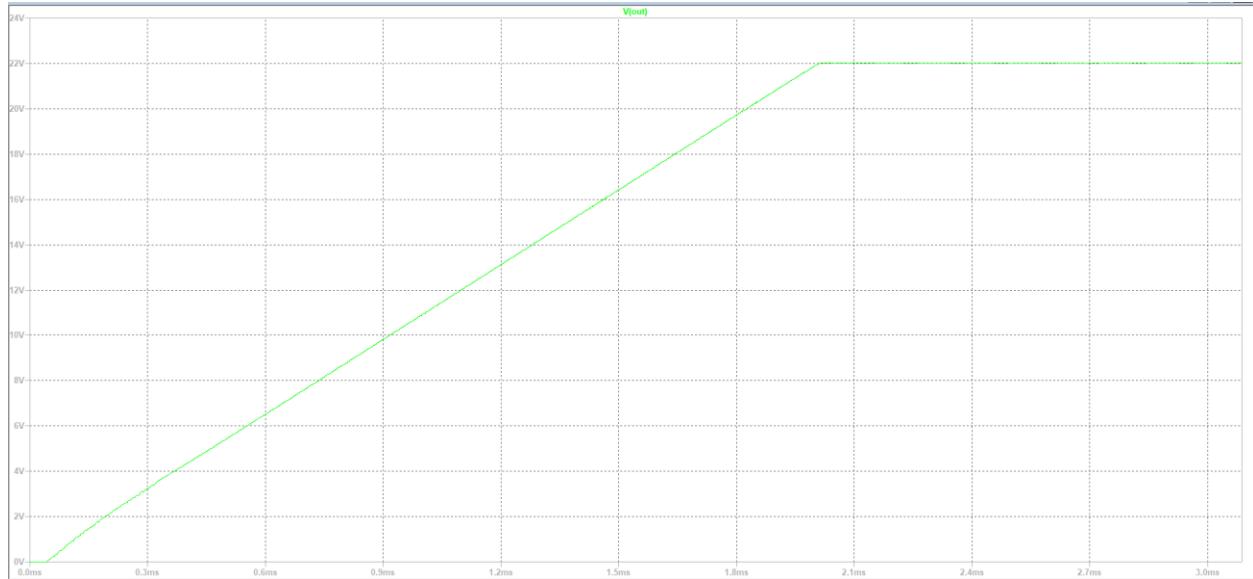


Figure 38: Output wave form of figure 37

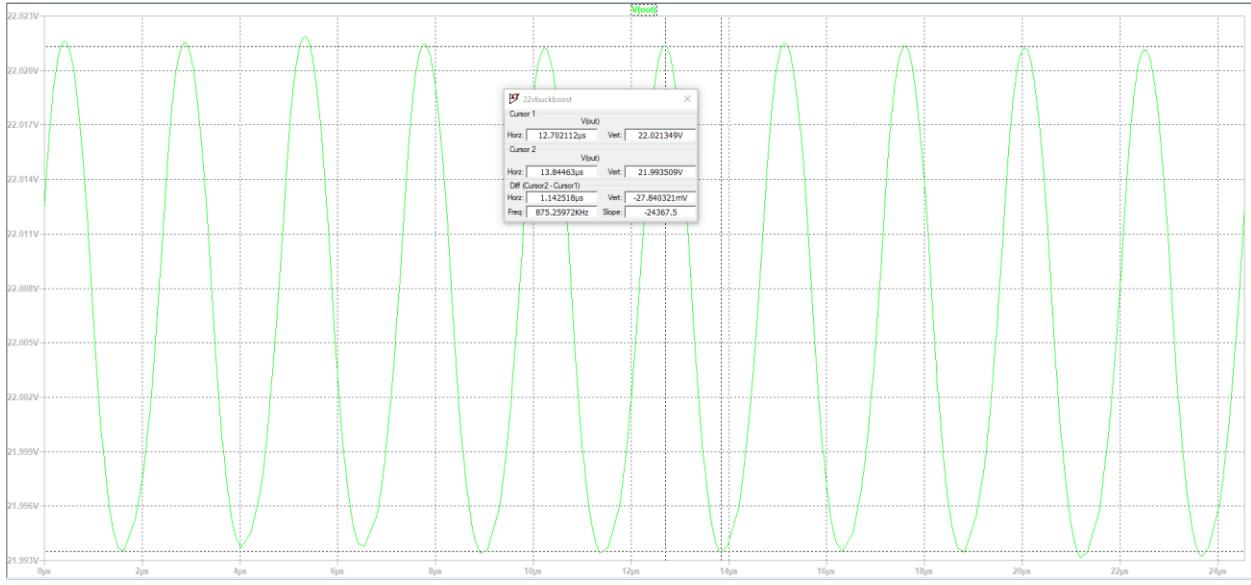


Figure 39: Steady state simulation of figure 37

According to figure 38 and figure 39, output is good, but voltage ripple for 36V input is higher than 1% of the output voltage, so I need to fix this problem. Firstly, to reduce this, I try to connect one more parallel capacitor to reduce the ESR value half of it. However, the solution does not work. I need to decrease ESR value more, so I select higher capacitance value with much lower ESR value. I pick two $470\mu\text{F}$ capacitors with $34\text{m}\Omega$. After this selection, 23mV output ripple is obtained, but it was not enough. My second solution is about modification of the ITH pin of the IC. This pin is located to reduce ripple and there is no analytic calculation of the components that connect this pin, so according to example design and demo board structure, I try to find better choices. I can decrease 0.5mV more, but it still is not enough. Unfortunately, as a last change, I increase the inductor value. I do not want to increase this value because of the size requirement, but by increasing we decrease ripple significantly thank to decrease in the resistance at the same time. To observe effect of inductance, I use sweep property of LTspice and obtain figure 40.

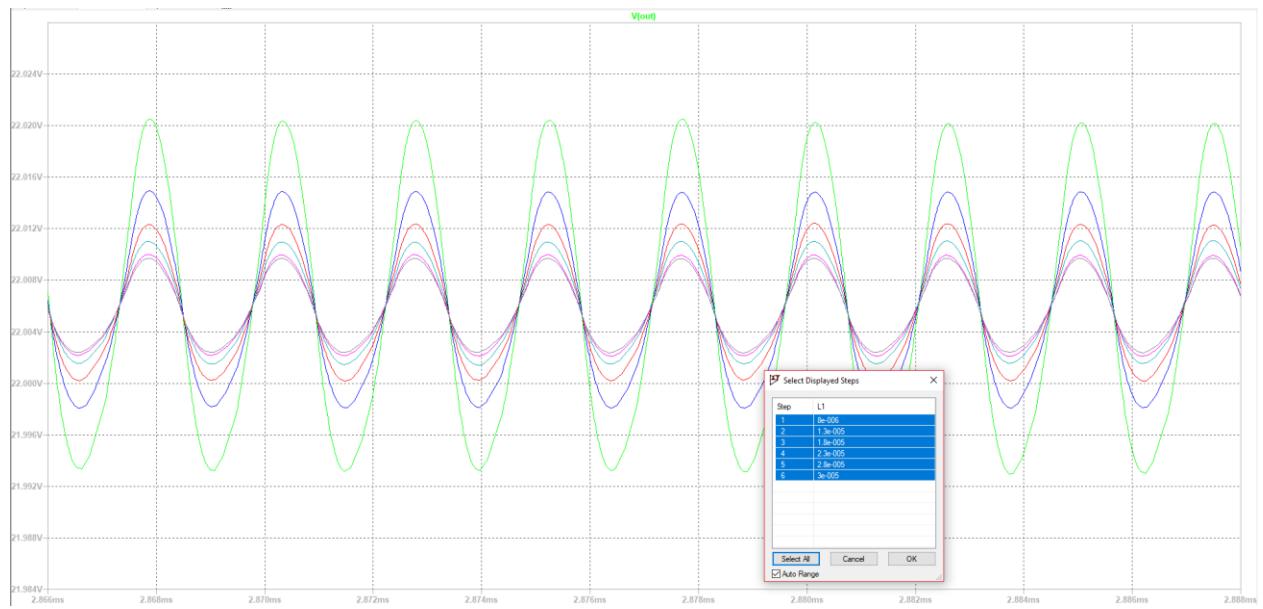


Figure 40: output voltage ripple at steady state with sweeping inductance value from $8\mu\text{H}$ to $30\mu\text{H}$ with $5\mu\text{H}$ steps.

As we can see from figure 40 easily, increasing inductance value improve ripple performance. However, when value getting higher, improvement getting slower, so I pick $15\mu\text{H}$ inductor. Thanks to that, I decrease voltage ripple 14mV which is lower than 22mV , so it is acceptable.

After that, I check efficiency of the design.

--- Efficiency Report ---
Efficiency: 92.6%

**Input: 157W @ 36V
 Output: 145W @ 22V**

Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	378mA	1248mA	0mW
C3	524mA	28314mA	0mW
C4	0mA	0mA	0mW
C5	0mA	0mA	0mW
C6	0mA	0mA	0mW
C7	135mA	197mA	1mW
C8	0mA	0mA	0mW
C9	477mA	27013mA	0mW
C10	0mA	0mA	0mW
D1	0mA	0mA	0mW
D2	466mA	26958mA	64mW
L1	6594mA	7284mA	336mW
M1	55mA	63mA	1517mW
Q1	6097mA	63277mA	6259mW
Q2	6594mA	7495mA	66mW
Q3	3mA	1259mA	0mW
Q4	4782mA	56051mA	2900mW
R1	0mA	0mA	119µW
R2	0mA	0mA	2mW
R3	4806mA	56526mA	97mW
R4	0mA	0mA	0µW
R5	6584mA	6794mA	43mW
R6	0mA	0mA	42µW
R7	0mA	0mA	0µW
R8	0mA	0mA	0µW
R9	0mA	0mA	0µW
R11	0mA	0mA	87µW
R12	0mA	0mA	10mW
U1	305mA	2241mA	280mW

Figure 41: Efficiency report of the figure 37 design

When we analyses efficiency results, overall efficiency looks good. However, when numbers are detailed analyze, power dissipation is localized few components, so this is problem as the previous part. For solution, I start to change power MOSFETs according to rule of thumb. According to result Q1 and Q4 has heat problem, so I change them with better MOSFETs to decrease dissipations on them. I increase the Rds(on) value of the Q1 to reduce gate charge. For Q4, I pick MOSFET to reduce gate charge same as the Q1. Finally, I increase efficiency of the design as figure 42.

--- Efficiency Report ---
Efficiency: 98.0%

Input: 148W @ 36V
Output: 145W @ 22V

Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	376mA	5670mA	0mW
C3	250mA	38501mA	0mW
C4	0mA	3mA	0mW
C5	0mA	0mA	0mW
C6	0mA	0mA	0mW
C7	133mA	189mA	1mW
C8	0mA	0mA	0mW
C9	230mA	37529mA	0mW
C10	0mA	0mA	0mW
D1	0mA	3mA	0mW
D2	232mA	37516mA	13mW
L1	6599mA	8020mA	338mW
M1	13mA	13mA	354mW
Q1	5268mA	48948mA	799mW
Q2	6599mA	12241mA	66mW
Q3	11mA	4345mA	1mW
Q4	4109mA	39792mA	1213mW
R1	0mA	0mA	119µW
R2	0mA	0mA	2mW
R3	4105mA	39644mA	71mW
R4	0mA	0mA	0µW
R5	6588mA	6793mA	43mW
R6	0mA	0mA	42µW
R7	0mA	0mA	0µW
R8	0mA	0mA	0µW
R9	0mA	0mA	0µW
R11	0mA	0mA	87µW
R12	0mA	0mA	10mW
U1	107mA	1373mA	84mW

Figure 42: Efficiency report of the modified design

After this process overall design looks like figure 43.

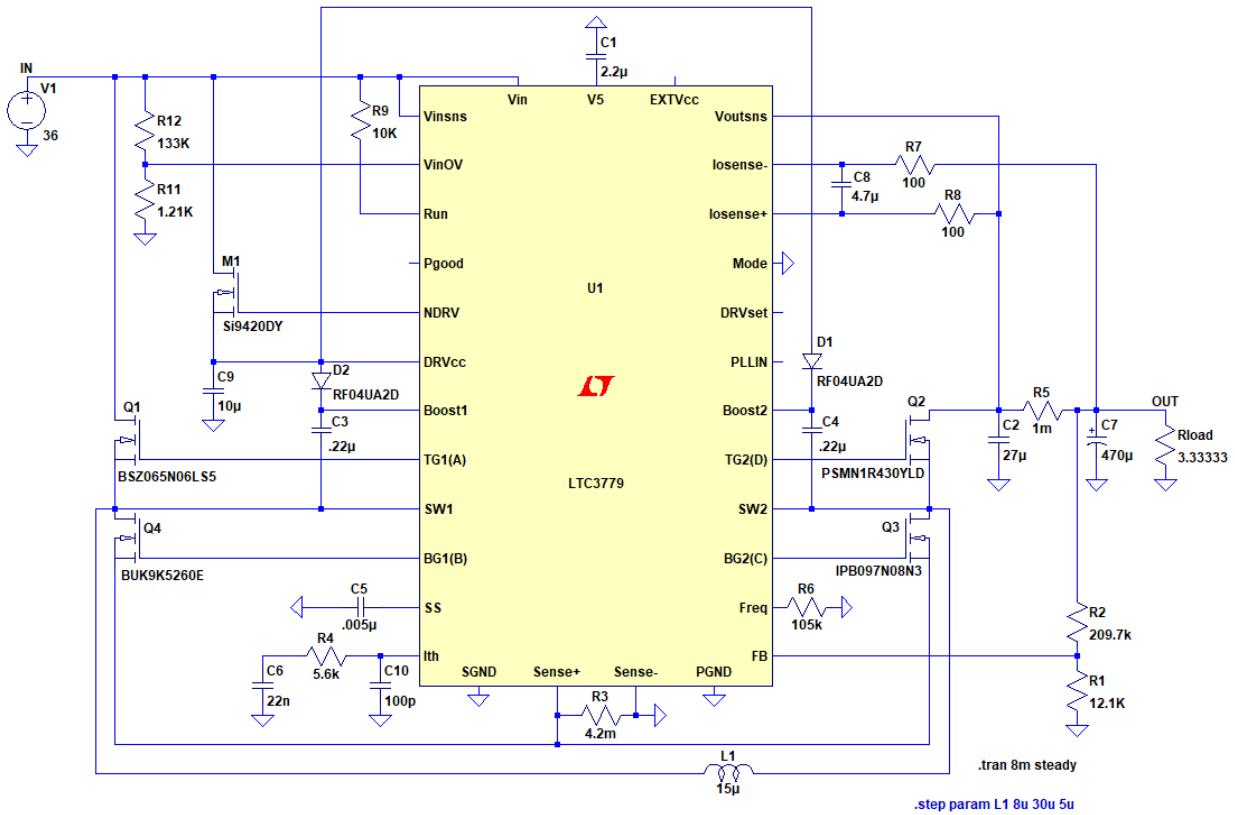


Figure 43: Modified overall design

At this point my SP period is done. Therefore, I could not work on further analysis of this design such as overshoot etc.

7.Conclusion

All in all, I have completed my summer practice (EE400) in ASELSAN. It was good experience for me. I had chance to work on a small part of a project. This gives me a chance to see power electronic area of electrical-electronic engineering, and observation of working environment in ASELSAN. Also, I learnt new concepts such as converter topologies, regulators etc. Moreover, I had chance to use some technical equipment that I have never used before like thermal camera, spectrum analyzer, loads etc. Beside of these, I had chance to be participate working environment for a month, and it was very good and enjoyable for me.

I completed my first SP in 1st Air Force Sustainment Center Headquarter. When we compare my two SPs, second one is more active and efficient. The main reason of this is work planning difference. To clarify, first place works are planned, so they know how much they should work, so during holiday sessions, they reduce to loads. Therefore, summer practice sessions have low dense work load. However, my second SP location is working on design, so their works are at the level of their capabilities. Due to this, SP sessions have full efficient. In other words, there are always a work to participate. To sum up, I strongly suggest ASELSAN/TEKNOKENT to SP.

8. APPENDICES

Appendix A Data Sheets

<http://www.analog.com/media/en/technical-documentation/data-sheets/ltc3779.pdf>

<http://www.analog.com/media/en/dsp-documentation/evaluation-kit-manuals/DC2456AF.PDF>

Appendix B Thermal and Heat sink Pictures

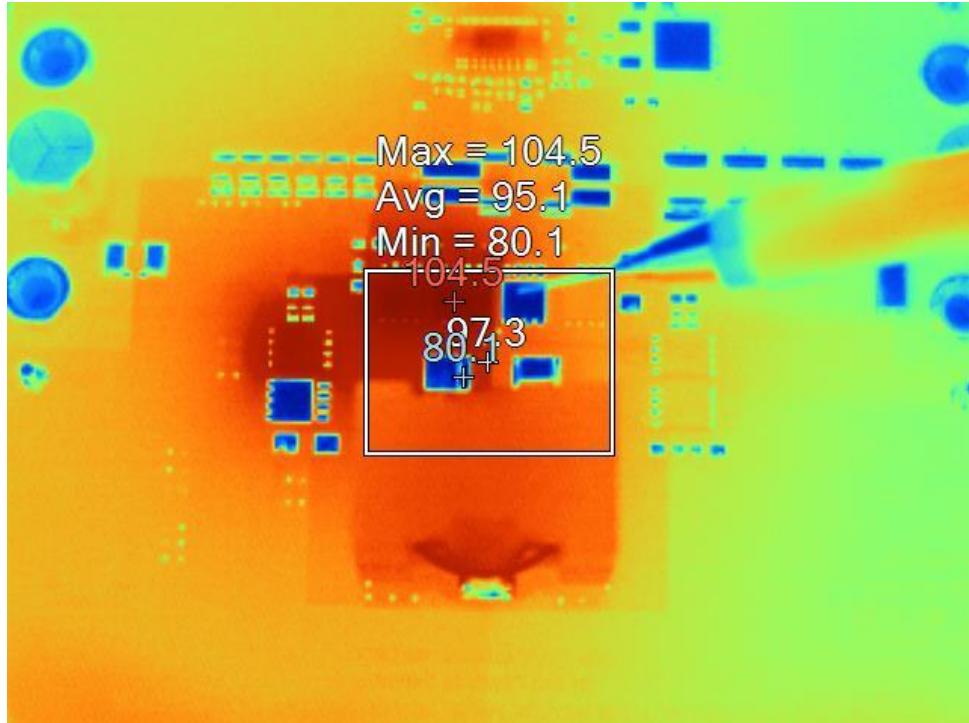


Figure 44: Thermal picture of the design with demo board transistors when input is 10.5V, and load is 2A

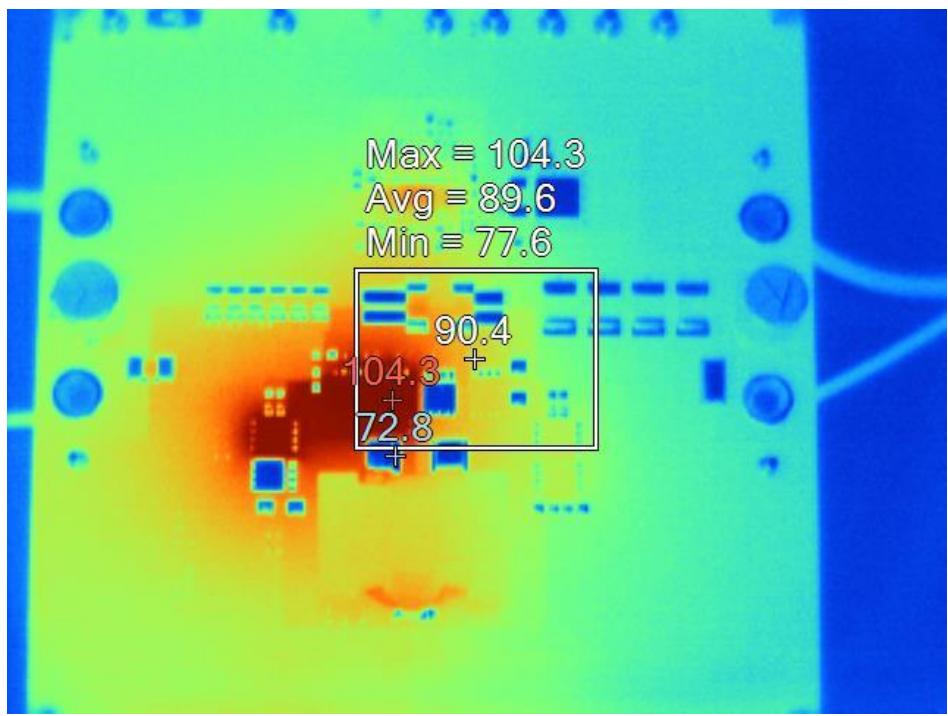


Figure 45: Thermal picture of the design with demo board transistors when input is 15V, and load is 2A

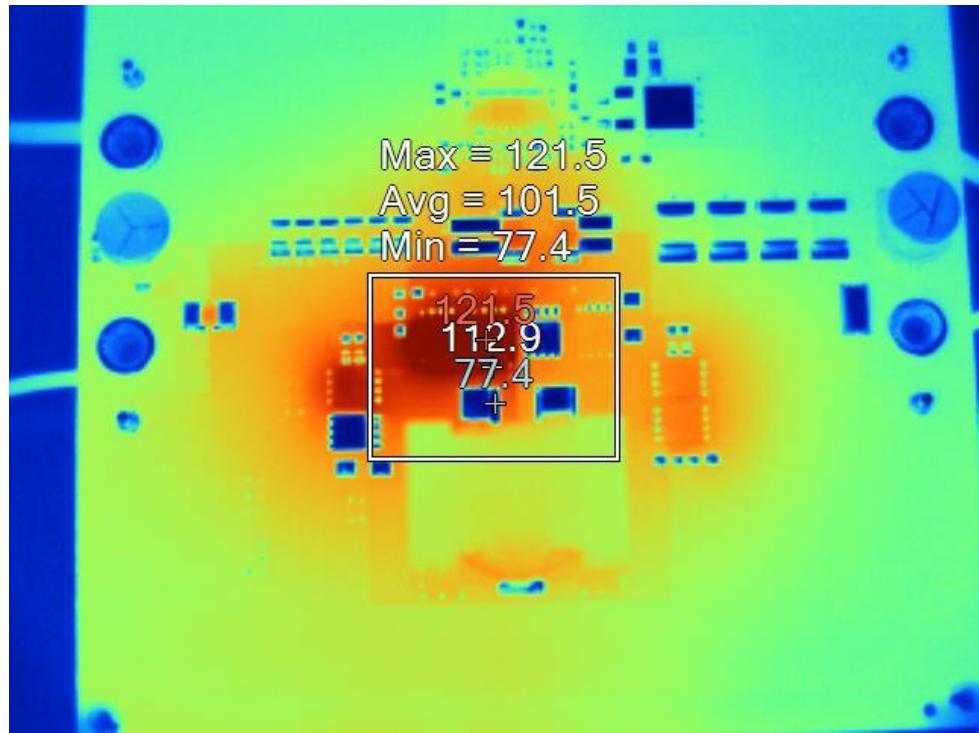


Figure 46: Thermal picture of the design with demo board transistors when input is 36V, and load is 6.6A

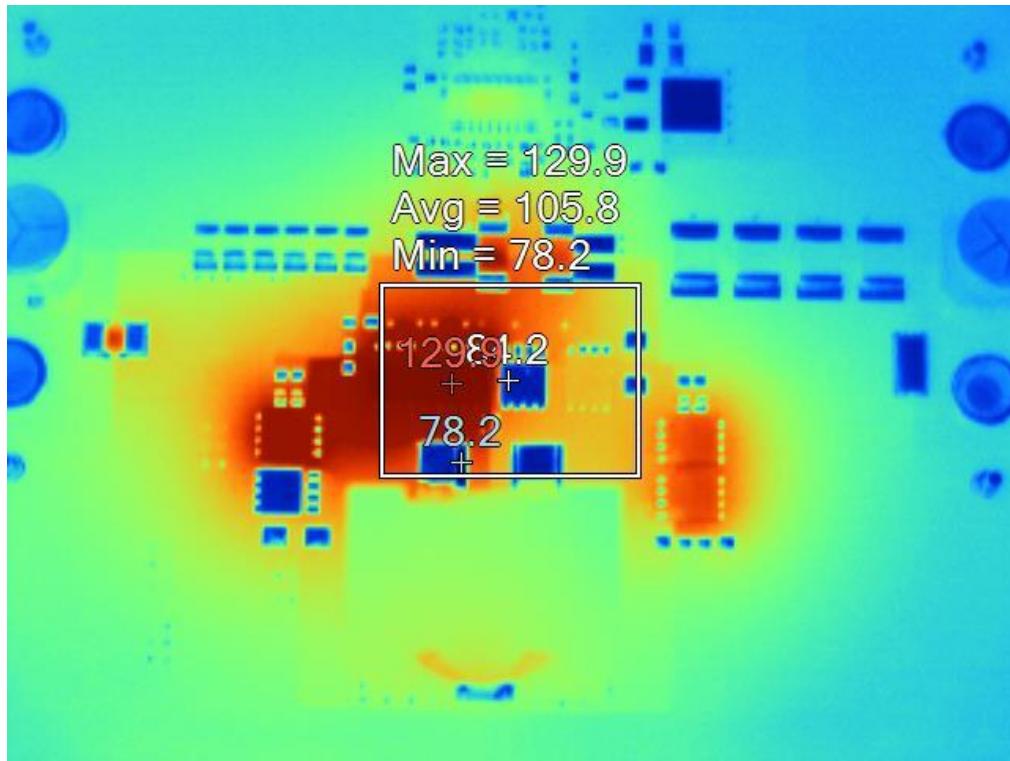


Figure 47: Thermal picture of the design with CSD MOSFETs and heat sink combination when input is 24V, and load is 6.6A

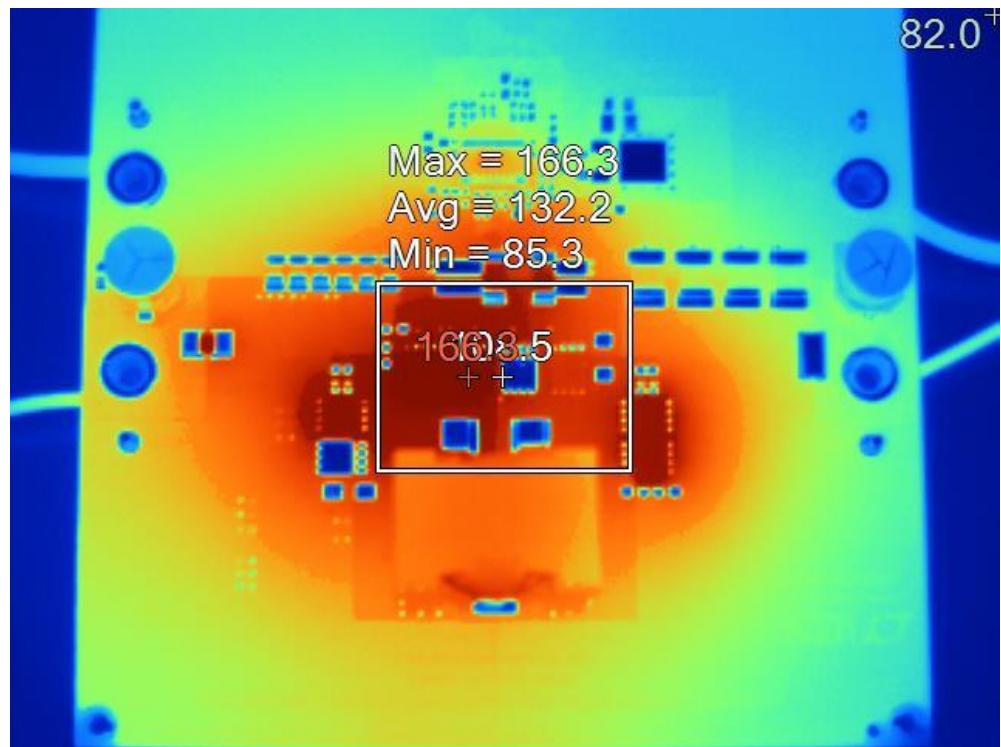


Figure 48: Thermal picture of the design with CSD MOSFETs and heat sink combinations when input is 10.5V, and load is 4A

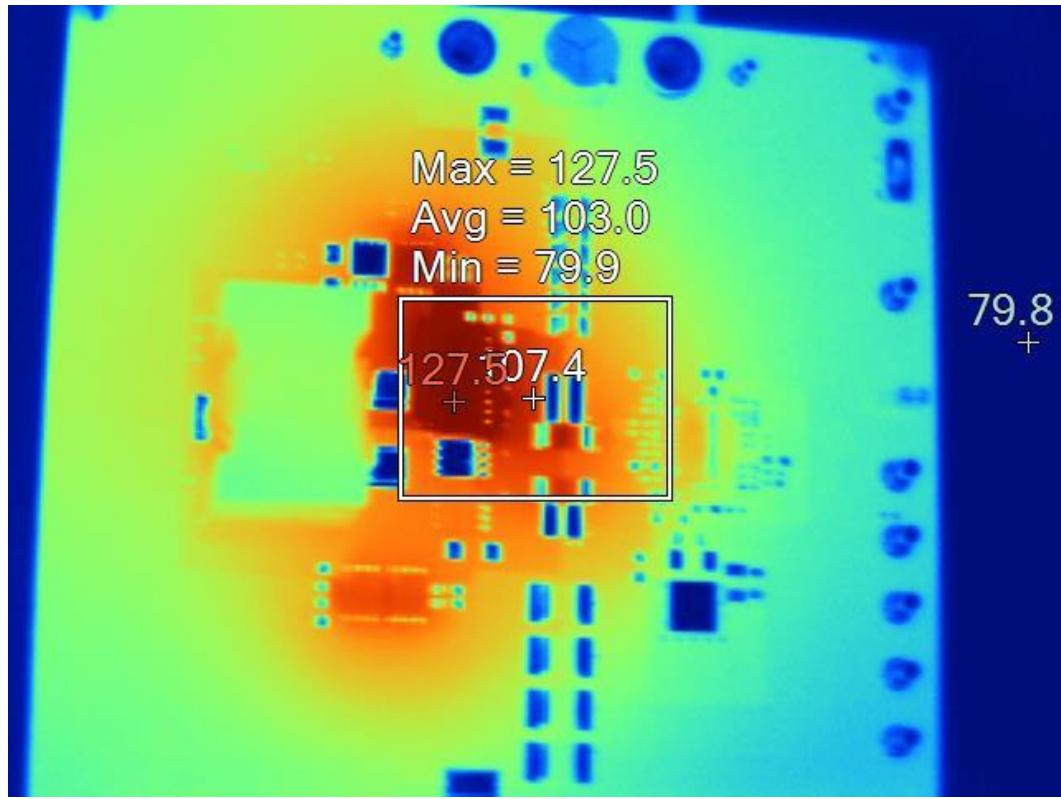


Figure 49: Thermal picture of the design with CSD MOSFETs when input is 36V, and load is 6.6A

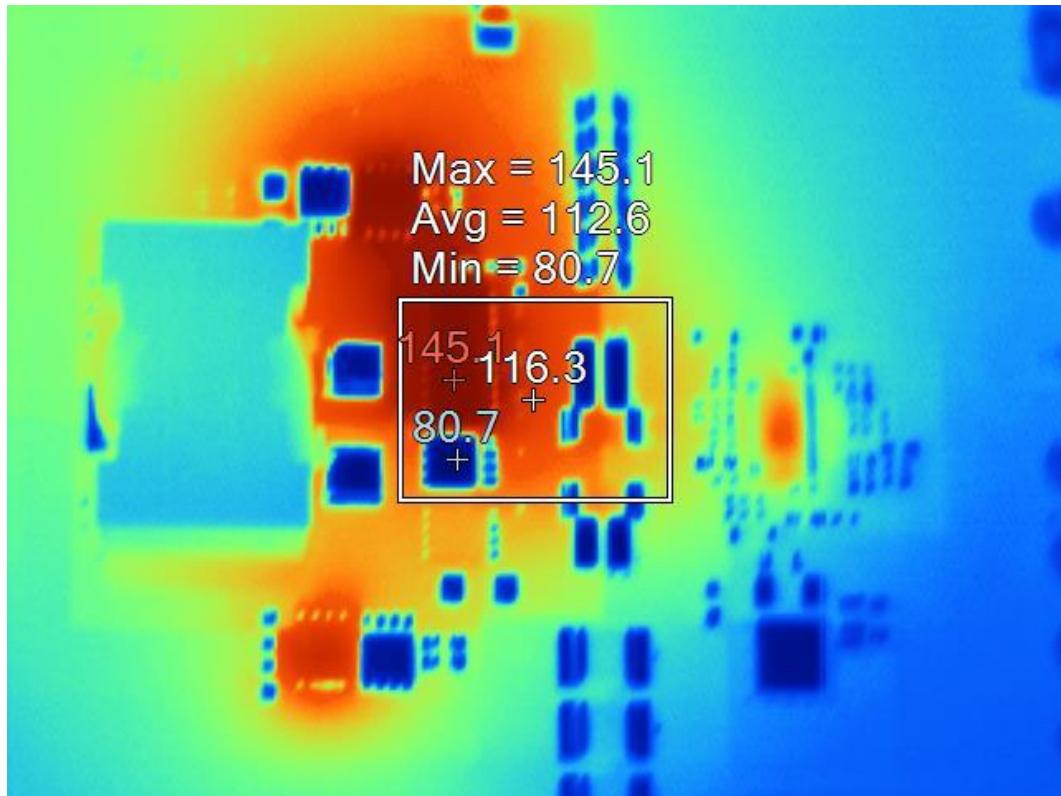


Figure 50: Thermal picture of the design with demo board transistors when input is 24V, and load is 6.6A

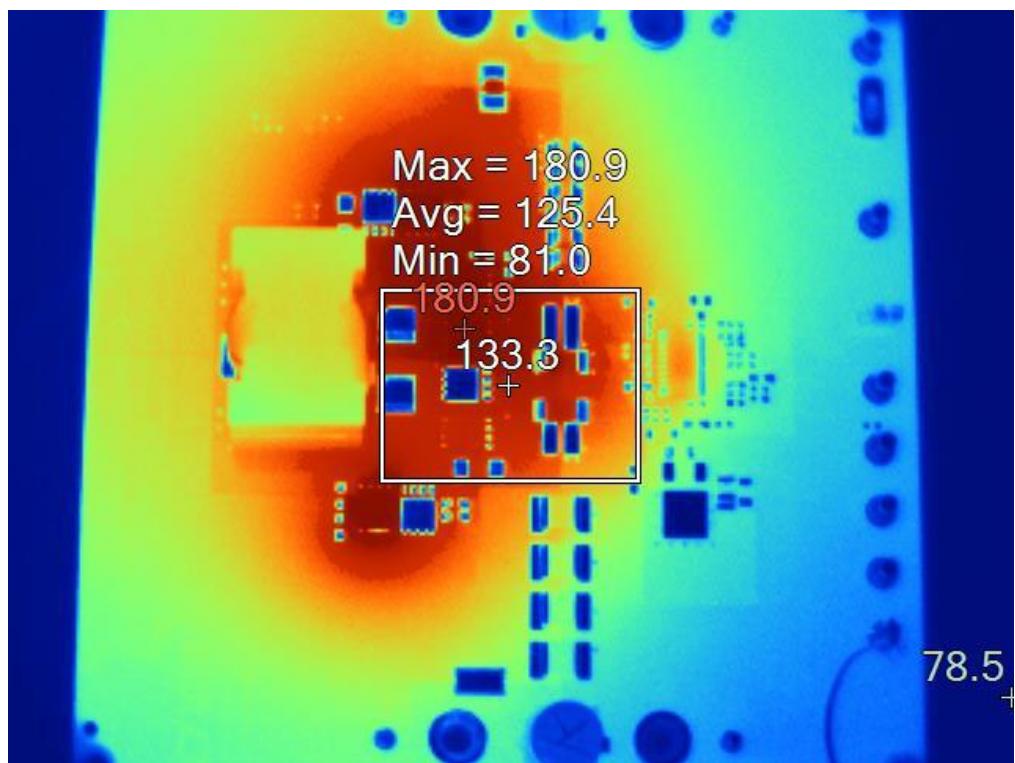


Figure 51: Thermal picture of the design with CSD MOSFETs and heat sink combinations when input is 17V, and load is 6.6A

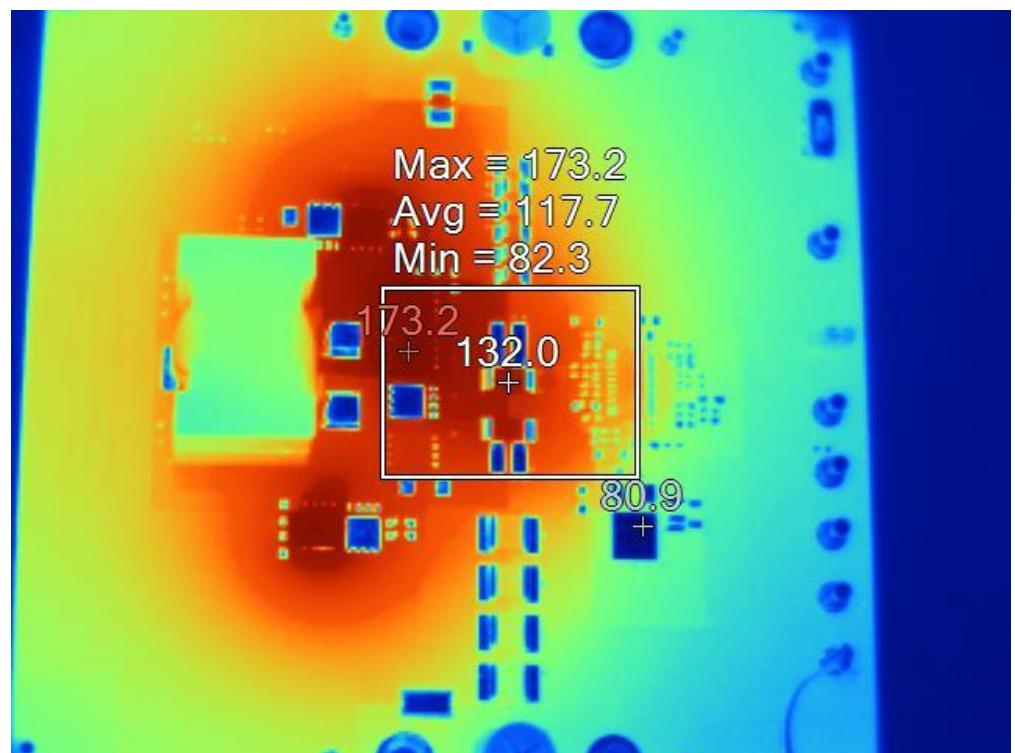


Figure 52: Thermal picture of the design with CSD MOSFETs when input is 15V, and load is 4A

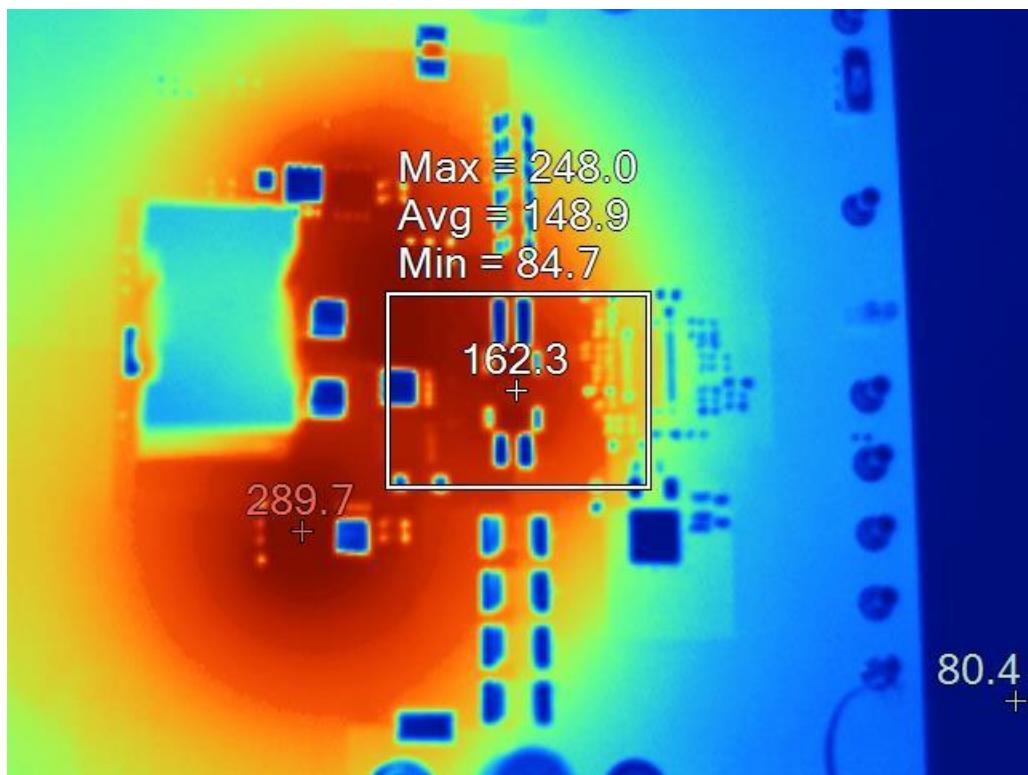


Figure 53: Thermal picture of the design with CSD MOSFETs when input is 10.5V, and load is 4A

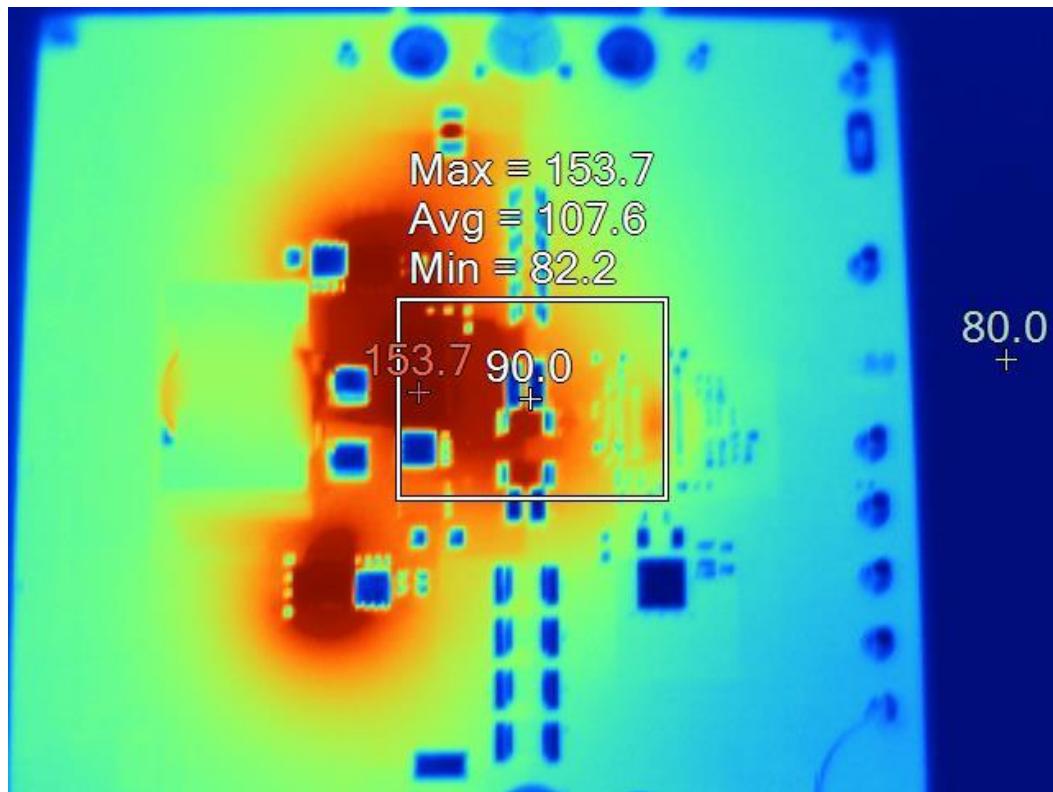


Figure 54: Thermal picture of the design with demo board transistors when input is 15V, and load is 4A

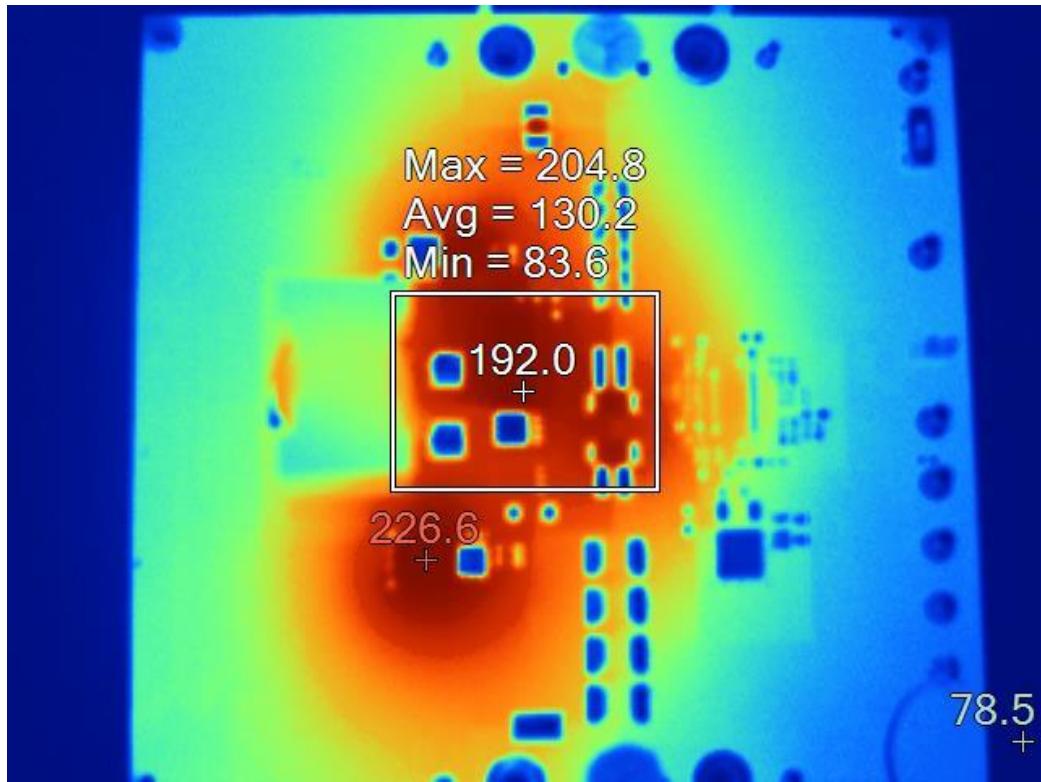


Figure 55: Thermal picture of the design with demo board transistors when input is 10.5V, and load is 4A

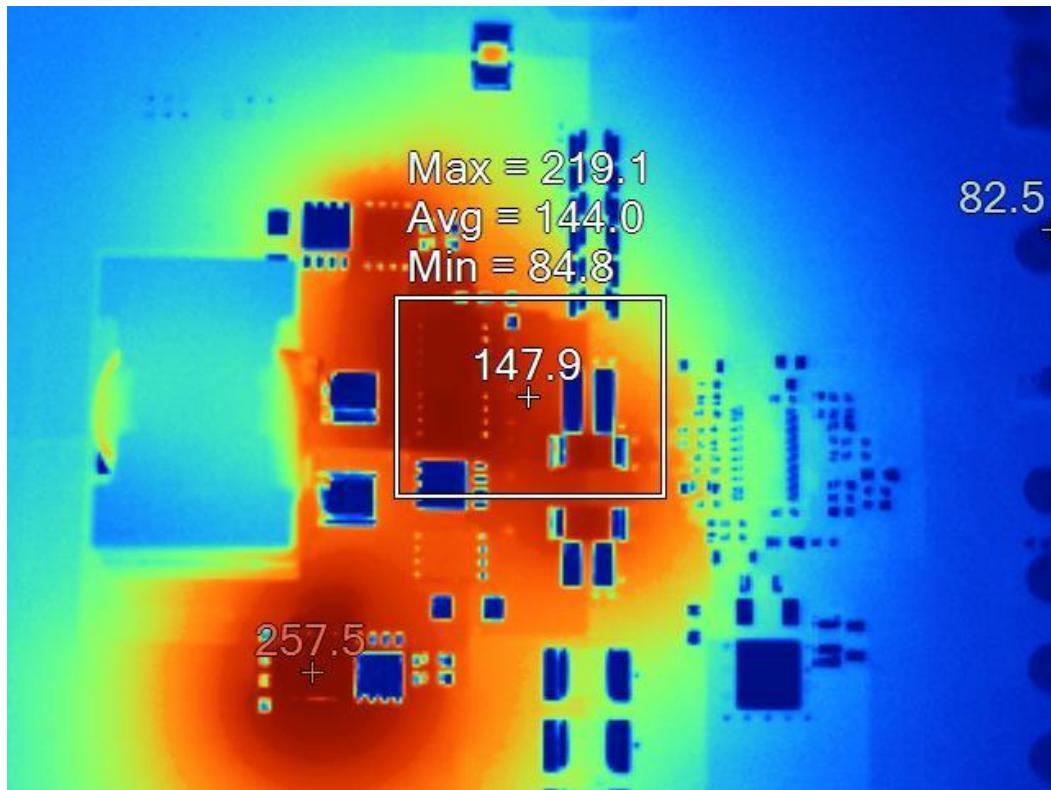


Figure 56: Thermal picture of the design with CSD MOSFETs when input is 17V, and load is 6.6A

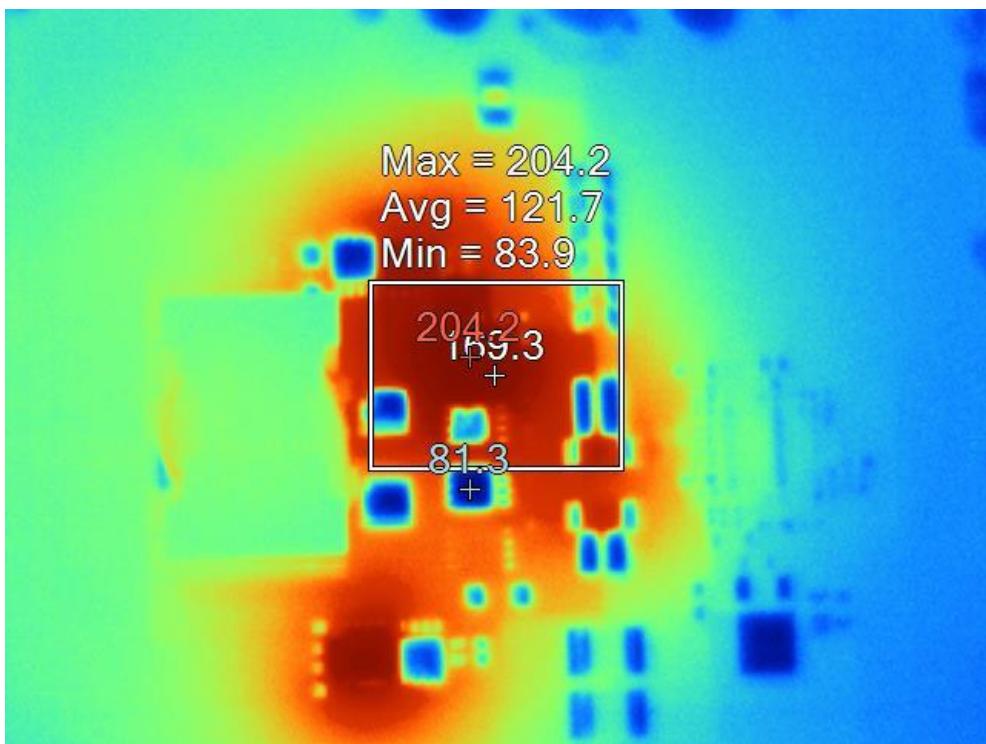


Figure 57: Thermal picture of the design with demo board transistors when input is 17V, and load is 6.6 A

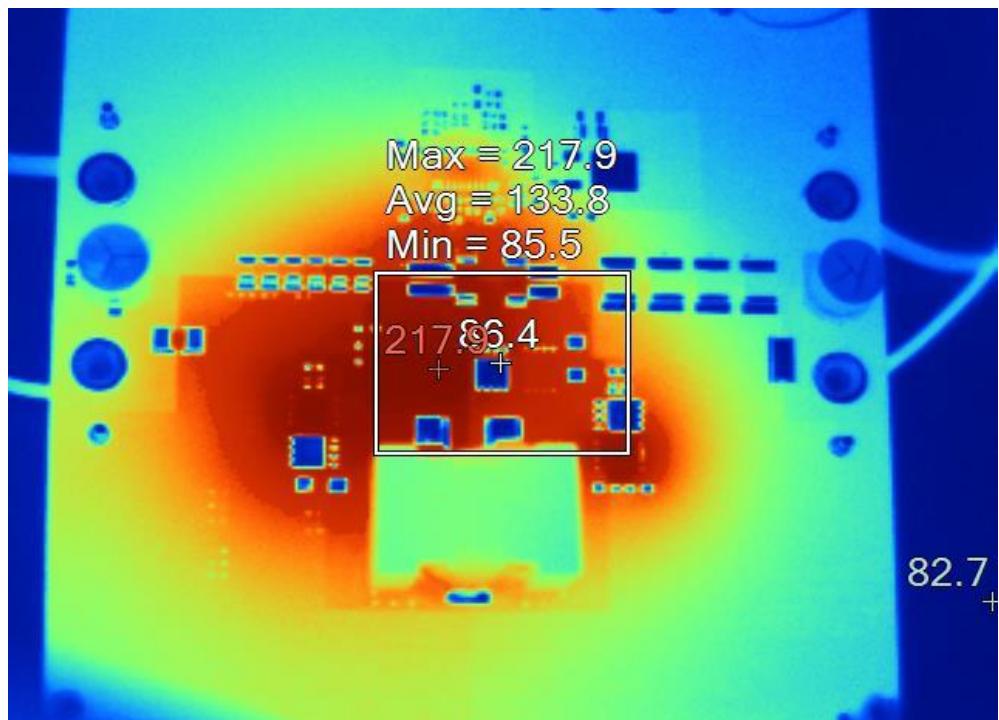


Figure 58: Thermal picture of the design with CSD MOSFETs at 400KHz switching frequency when input 24V, and load is 6.6A

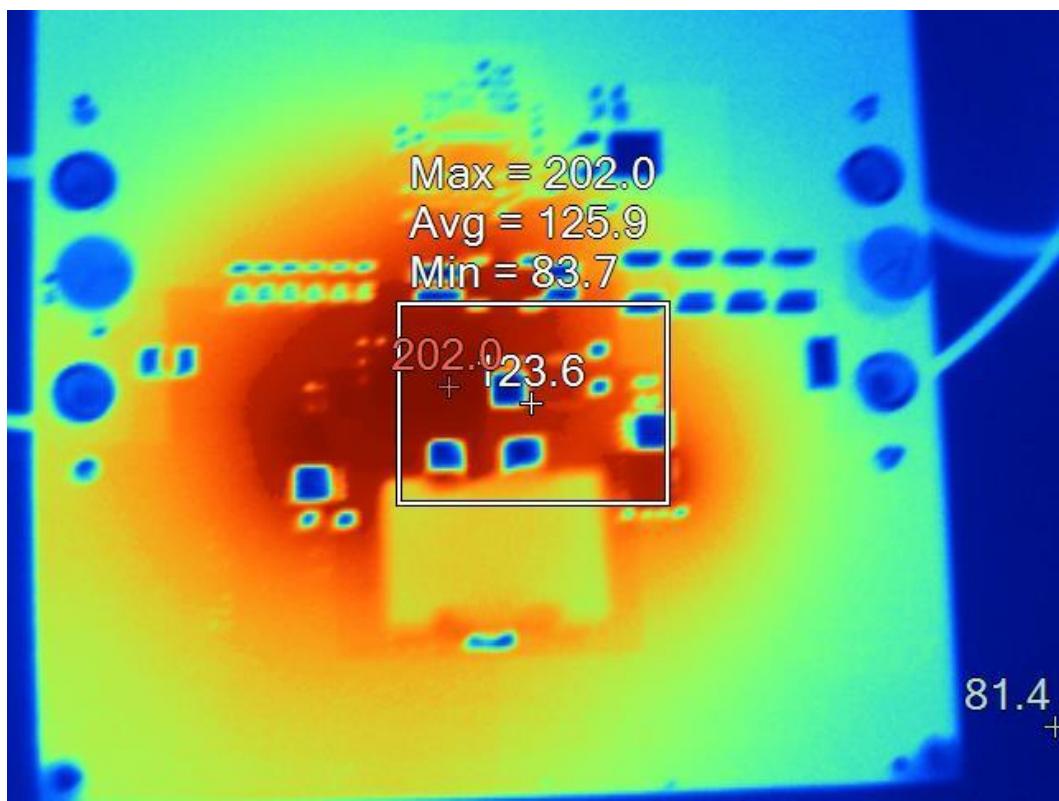


Figure 59: Thermal picture of the design with CSD MOSFETs at 400KHz switching frequency when input 36V, and load is 6.6A

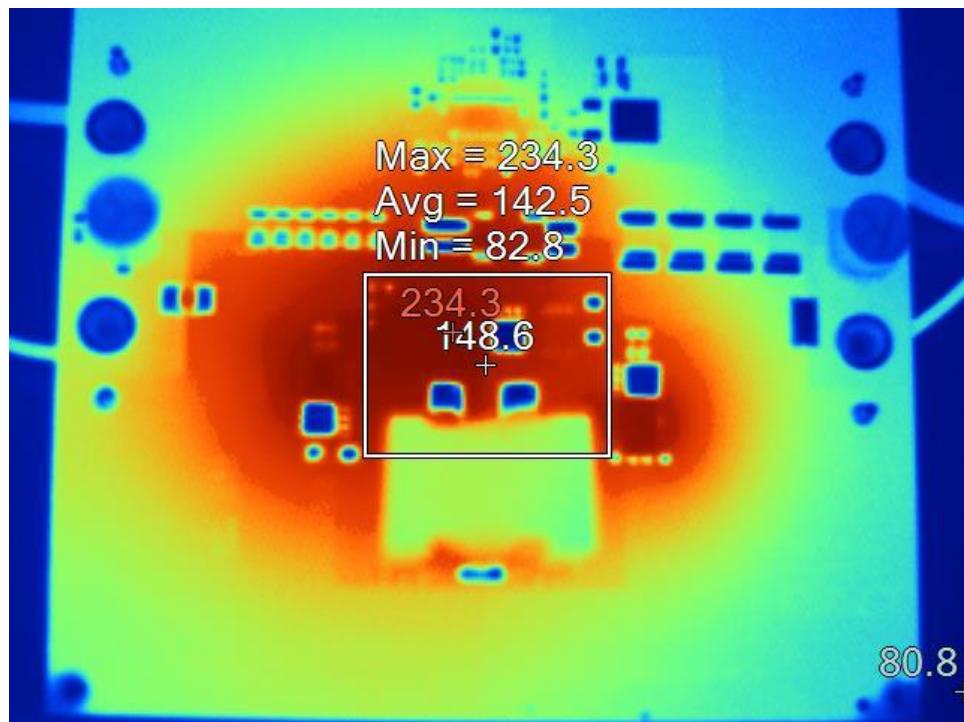


Figure 60: Thermal picture of the design with CSD MOSFETs at 400KHz switching frequency when input 17V, and load is 6.6A

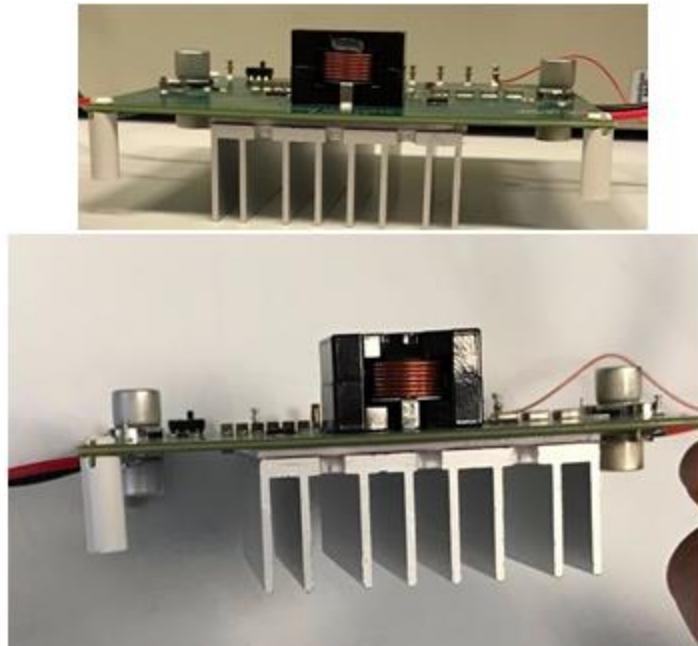


Figure 61: Demo board with heat sink

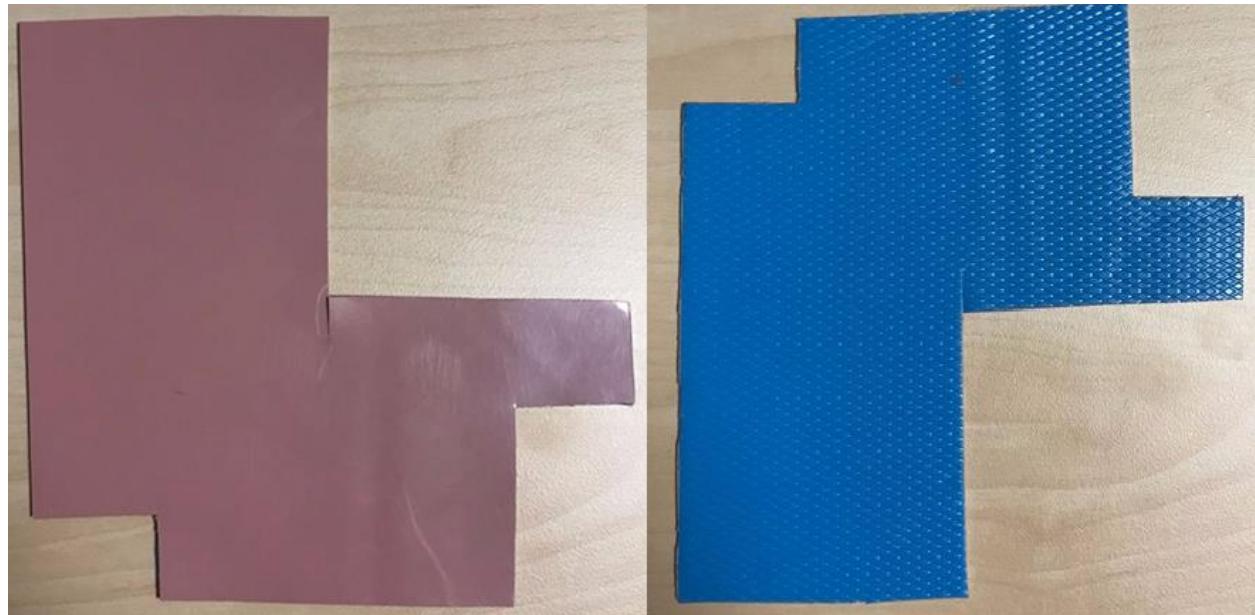


Figure 62: Thermal pad which is used between heat sink and the demo board (pink side towards to head sink)

Appendix C Spectral Analysis of the Vin = 10.5-36 V, O/P 50 V 330W/200W Boost Dc-Dc converter

Thanks to spectrum analyzer, we can observe frequency domain of the output signal. This gives us a chance to see noises of the output signal. I, also, make spectrum analysis of my design to see output noises are located at which frequencies.

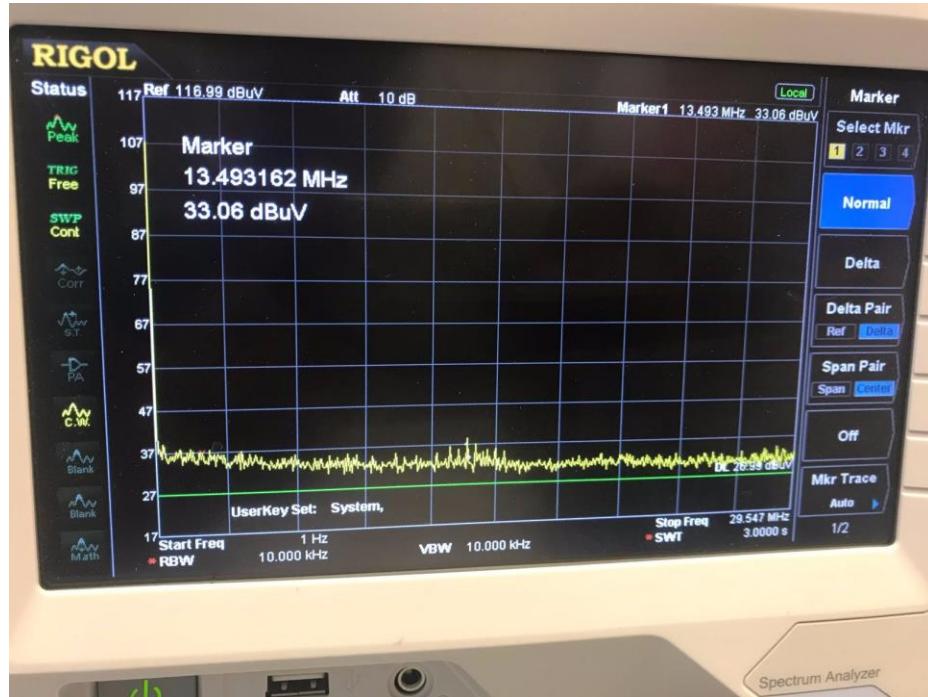


Figure 63: Output spectrum when input is 24V, and no load

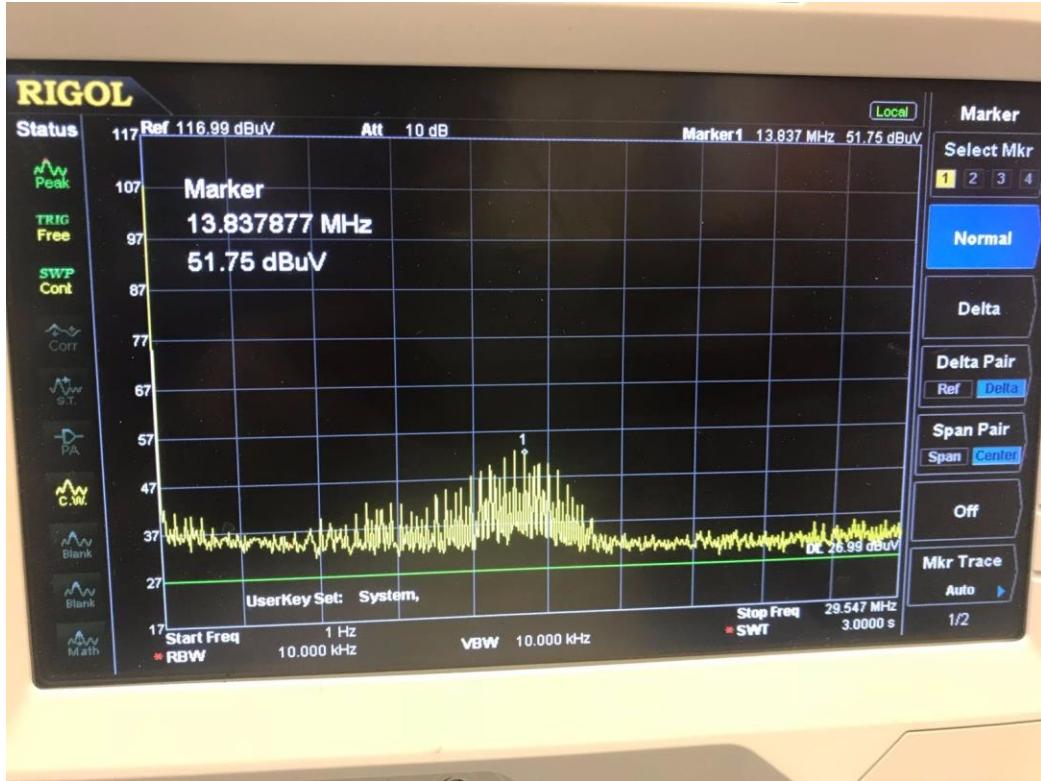


Figure 64: Output spectrum when input is 24V, and load is 6.6A

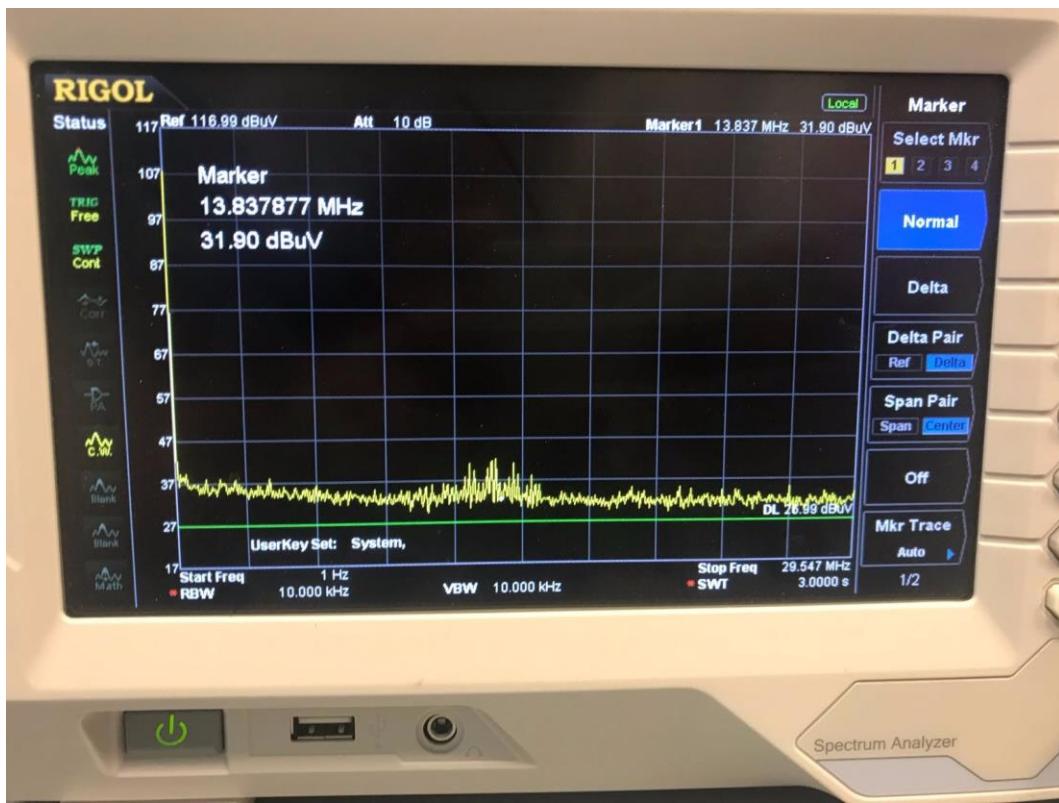


Figure 65: Output spectrum when input is 10.5V, and no load

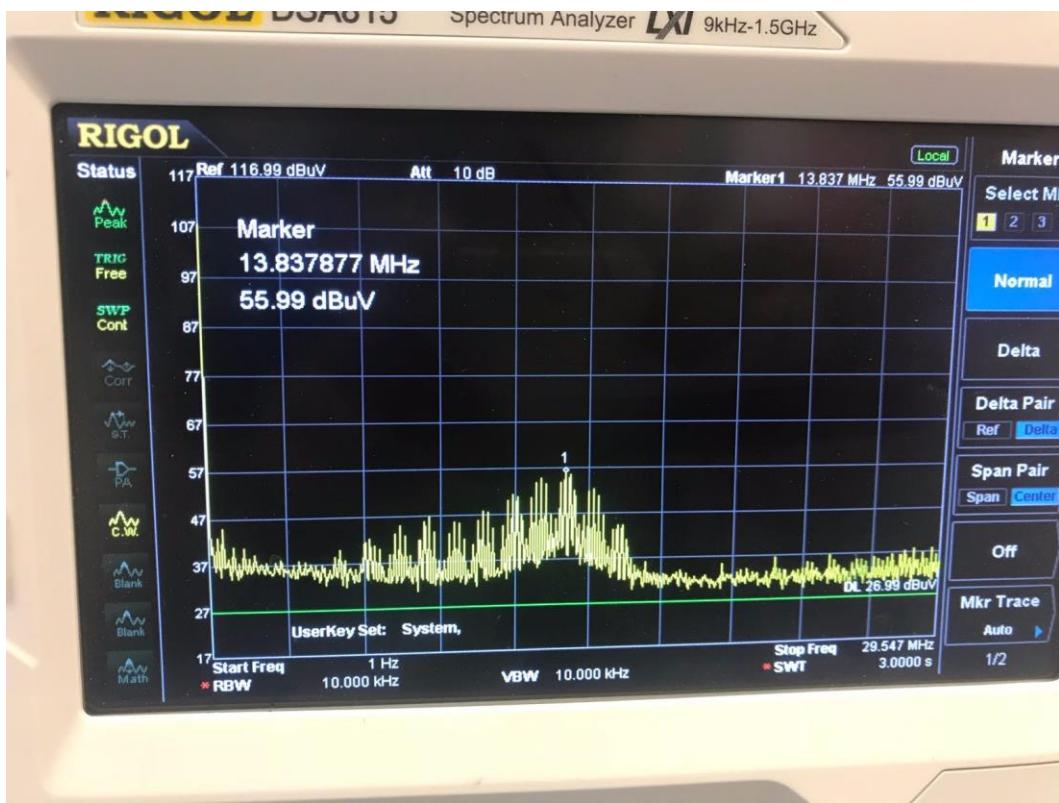


Figure 66: Output spectrum when input is 10.5V, and load is 4A

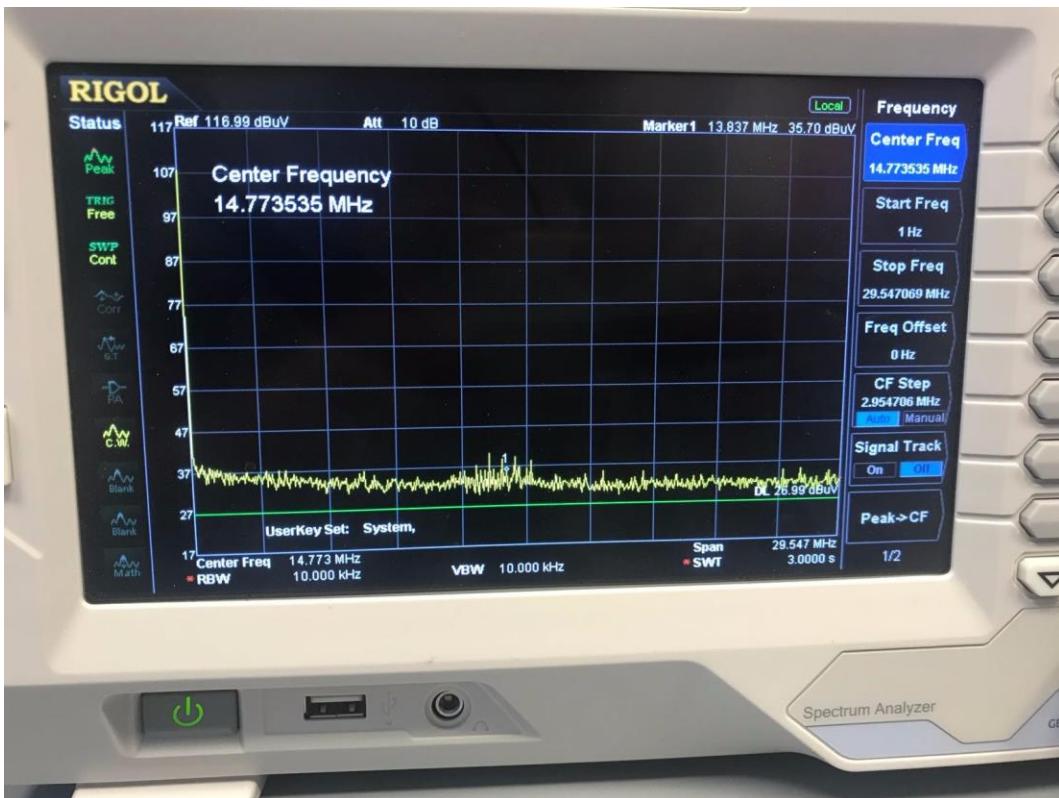


Figure 67: Output spectrum when input is 17V, and no load

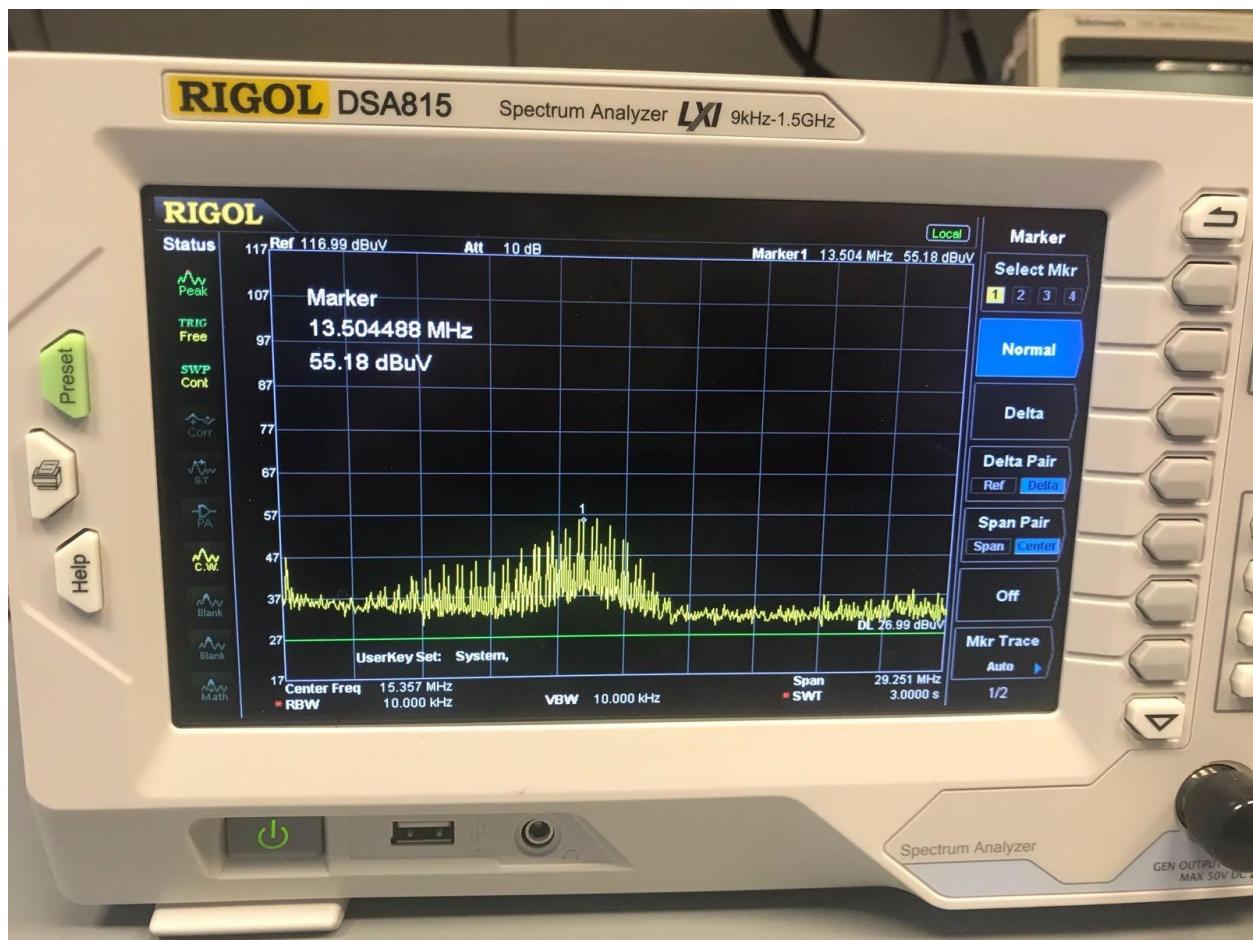


Figure 68: Output spectrum when input is 17V, and load 6.6A

9. REFERENCES

- [1] <https://www.aselsan.com.tr>
- [2] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power electronics: converters, applications, and design*. New York: J. Wiley, 1995.
- [3] Linear Technology. (March 1999). *Understanding Buck-Boost Power Stages in Switch Mode Power Supplies* [Brochure]. Milpitas: Author.
- [4] Linear Technology DC2456A data sheets <http://www.analog.com>
- [5] Linear Technology LTC3779 data sheets <http://www.analog.com>