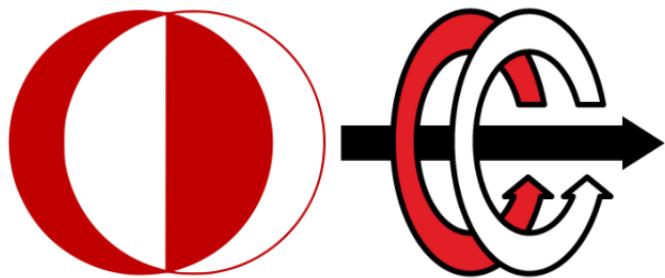


MIDDLE EAST TECHNICAL UNIVERSITY  
DEPARTMENT OF ELECTRICAL AND  
ELECTRONICS ENGINEERING



EE414 INTRODUCTION TO ANALOG INTEGRATED CIRCUITS  
TERM PROJECT

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Design of a Voltage and Temperature Independent  
Rail-to-Rail Input and Output Operational Amplifier  
Final Report

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**Students:**

*Halil Temurtas* : 2094522  
*Sarper Sertel* : 2094449

June 17, 2019

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# 1 Introduction

Operational amplifiers are one of the most widely used electronic components by the electronics communities. Although, a simple differential pair can be considered as an Op-Amp, a search for high performance Op-Amps has been continued since the discovery of operational amplifiers. In this project, our aim is to design a source voltage and temperature independent operational amplifier whose input and output common mode range is rail to rail.

In doing so, we considered our limited component budget and overall CMOS compatibility of the design. This report will focus on the key components of this kind of operational amplifiers. *Figure 1* represents the block diagram of the operational amplifier.

# 2 Operational Amplifier Design

In our design, we have considered the Op-Amp within four stages, namely,

1. **Biasing Stage:** The stage responsible from supplying temperature and supply voltage independent bias voltages and currents
2. **Input Stage:** The differential input stage responsible for rail-to-rail input operation
3. **First Stage:** The main amplification stage
4. **Second Stage:** Second amplification stage responsible for increasing bandwidth of the Op-Amp

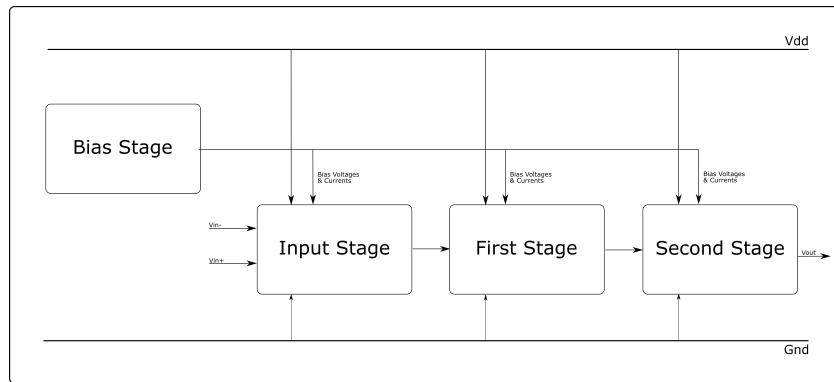


Figure 1: Block Diagram of the Rail-to-Rail Op-Amp



## 2.1 Biasing Stage

In Figure 2, temperature and supply independent bias structure is shown. The idea of this circuit is based on using threshold voltage of the MOSFETs at the bottom. On the left, reference voltage is created by using diode connected MOSFETs and mirrors. After this voltage transferred to bias generation stages.

At this stage, according to current, which is temperature independent, voltages are generated by  $V_{ds}$  values of the MOSFETs. At the last stage biasing current is generated ( $26\mu A$ ) by using reference voltage. So far, system is temperature independent, but supply dependency is not enough. Therefore, depletion type NMOS transistors are attached on top to isolation of the system from supply. Thanks to these approach, supply dependency is between 1 to 3 percent while temperature dependency is changing from 1 percent to 6.6 percent.

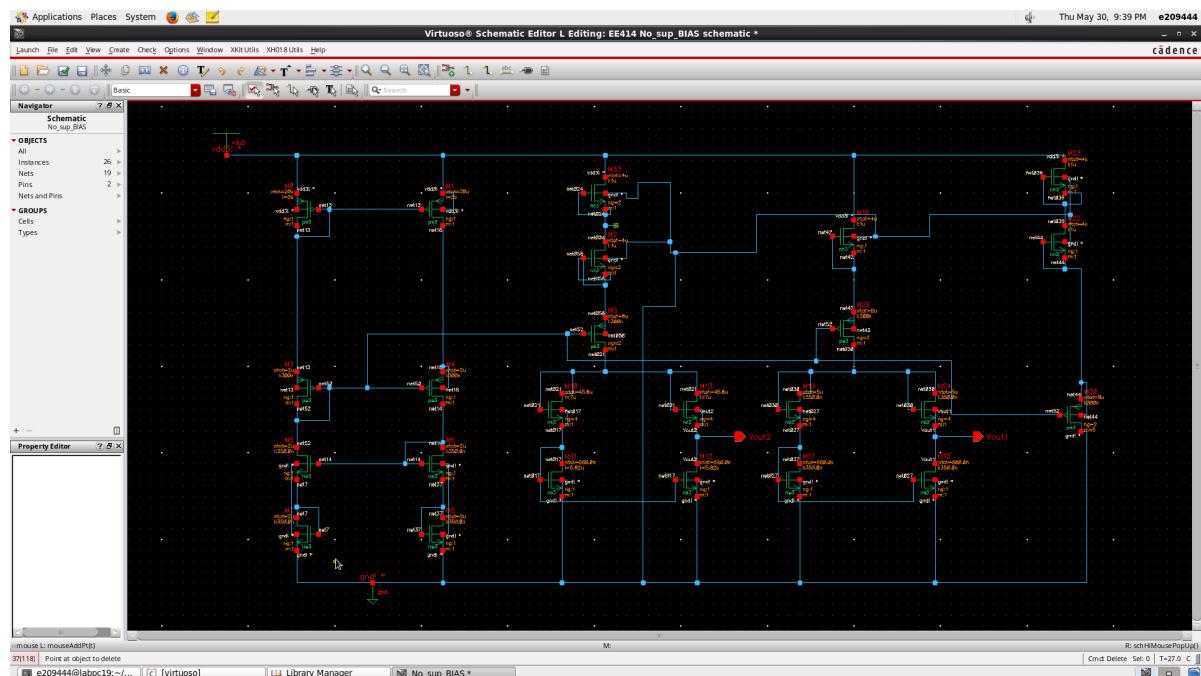


Figure 2: Bias Stage



Table 1: Bias Stage Transistors W/L Ratios

Transistors					W/L
M2	M16	M22	M23	M33	4/1
M0	M1	M3	M4		20/3
M5	M6	M7	M8		20/3.5
M9	M25	M30			80/3
M10	M13				45.6/7
M11	M12				0.56/5.82
M19	M24				50/3.5
M17	M18				6.8/3.5

## 2.2 Input Stage

To realise rail-to-rail input common mode range and avoid  $g_m$  variations at the same time, the input stage structure in the *Figure 3* is implemented.

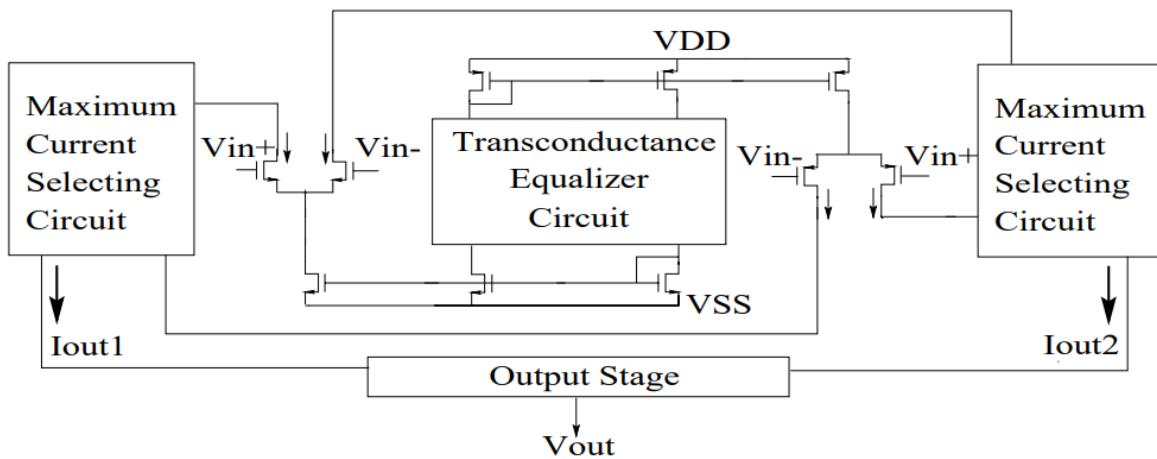


Figure 3: Input Stage[2]



## Input Differential Pair

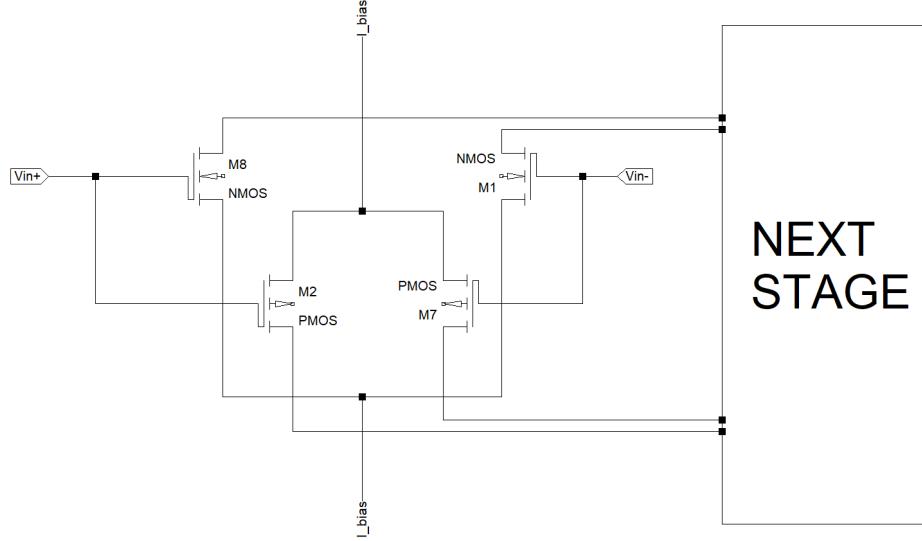


Figure 4: Input Stage[1]

This topology allows circuit to operate through PMOS differential pair low input voltage values and through NMOS differential pair at high input voltage values. However, this type of input structure also causes  $g_m$  variation due to activation and deactivation of transistors as shown in *Figure 5[1]*. This problem required us to utilize additional circuits in the implementation.

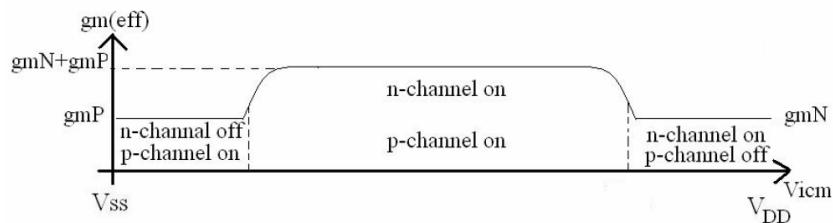


Figure 5:  $g_m$  variation with changing input[1]



## Max Selection Circuit

Basic idea behind this circuit is to compare and select the currents mirrored from PMOS complementary inputs and NMOS complementary inputs. To do so, currents from NMOS transistors are copied using  $M_{pp1}$  and  $M_{pp2}$  and transferred through  $M_{mnx}$ , similarly the current from PMOS transistors are copied using  $M_{m1}$  and  $M_{m2}$ . By the help of  $M_{m2-5}$ , maximum of this current then supplied to next stage, in our case to 1<sup>st</sup> Stage.

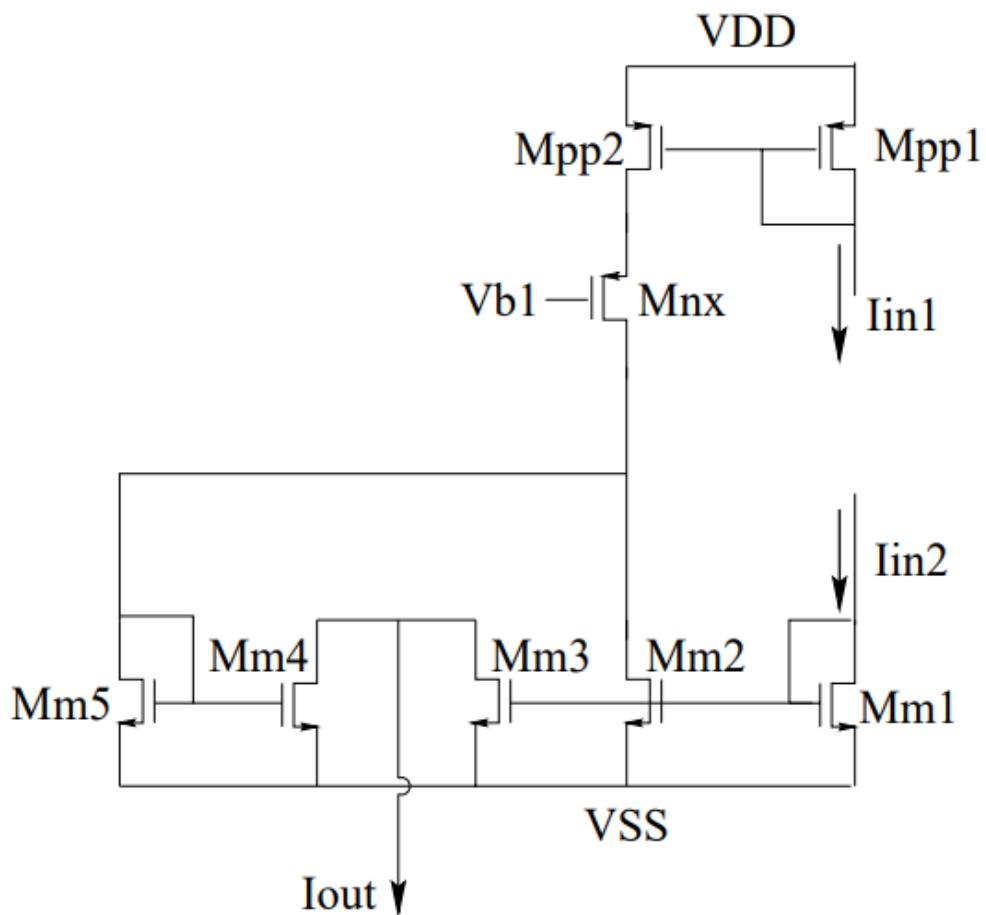


Figure 6: Max Selection Circuit



## Transconductance Equalizer Circuit

The last part of the input stage is the transconductance equalizer circuit, this circuit is implemented to increase the overall robustness of the input stage for the fabrication errors. In other words, the  $K_p-K_n$  mismatches due to fabrication processes is eliminated by this part.[2]

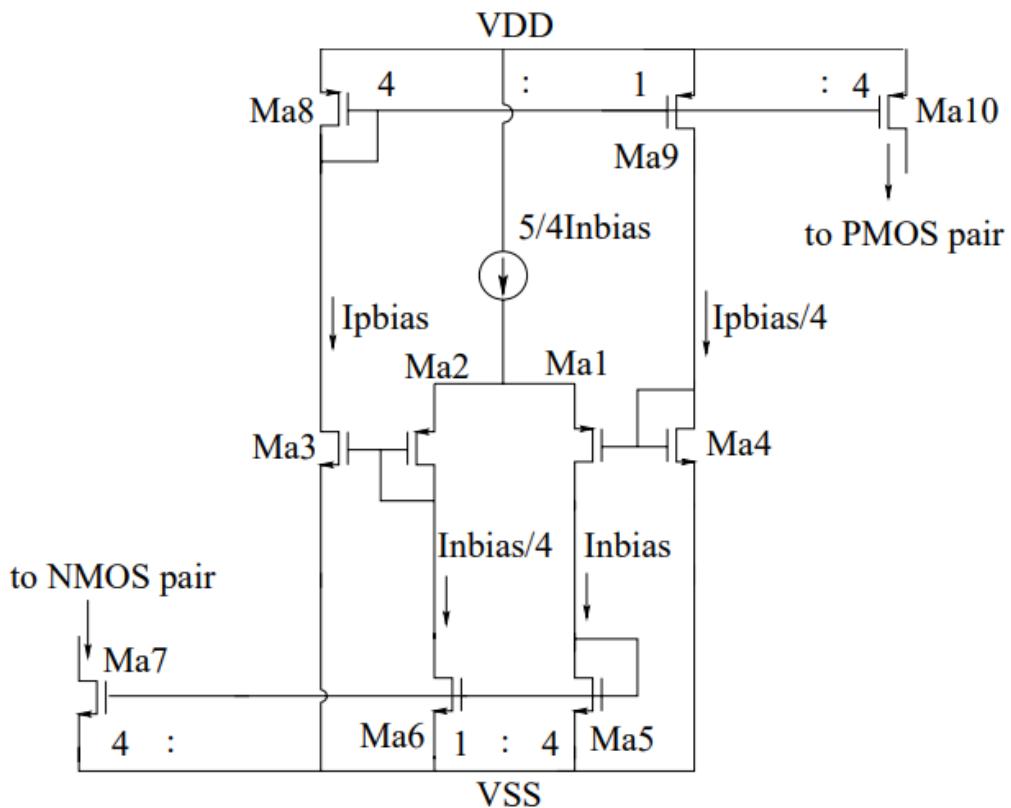


Figure 7: Equalizer Circuit



## Overall Input Stage

Overall input stage implemented in Cadence can be investigated in *Figure 8*. This circuit is then converted to a block to be used in the overall design.

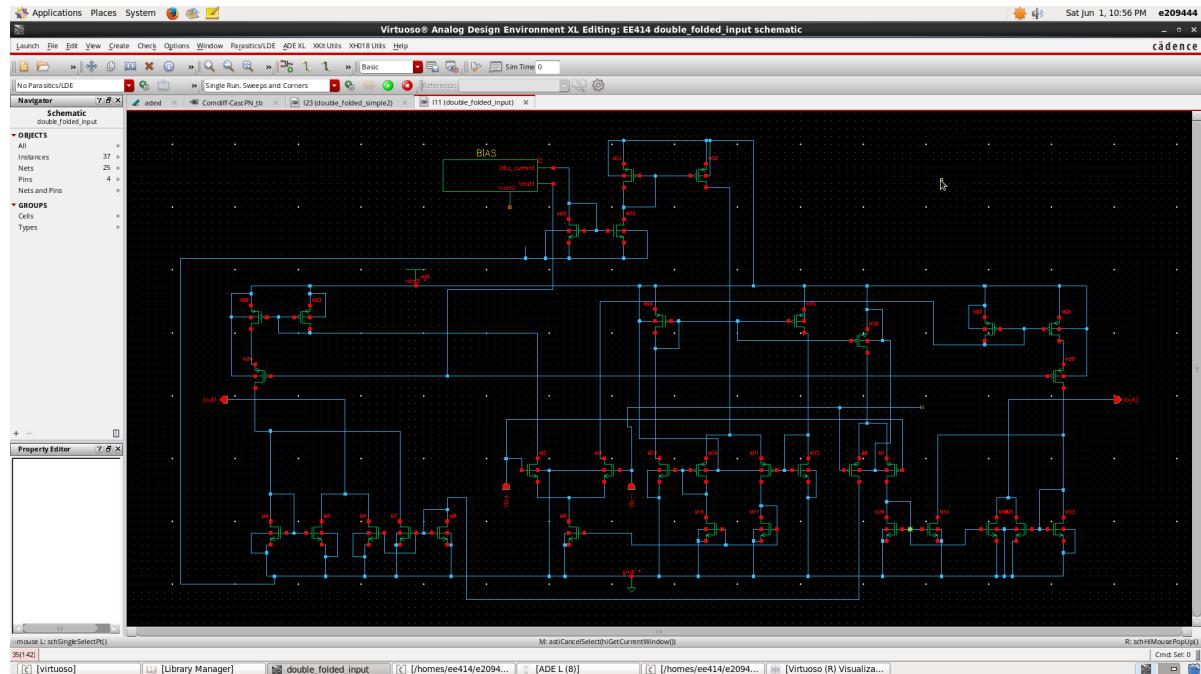


Figure 8: Overall Input Stage

Table 2: Input Stage Transistors W/L Ratios

Transistors		W/L
M33		45/1
M35		20/1
M31	M32	90/1
M4	M5    M6    M7    M9	36/1
M2	M3    M9	36/1
M19	M13    M16    M17	36/1
M10	M19    M21    M22    M30	36/1
M11	M14    M24    M25	36/1
M0	M1    M28	90/1
M30	M28    M29	90/1
M20	M23    M34	90/1



## 2.3 1<sup>st</sup> Stage

The 1<sup>st</sup> stage is the main amplification stage of the OP-AMP. As its name suggest an operational amplifier is basically an amplifier, thus, this stage plays a very crucial role in OP-AMP design. In our design, we haven utilized the folded cascode structure with input stage designed previously, can be seen in *Figure 9*, in order to improve our common mode input range while having high gain at one stage. However, although overall gain of this stage satisfied the given requirements, phase margin and bandwidth requirements required us to add an additional stage to the design.

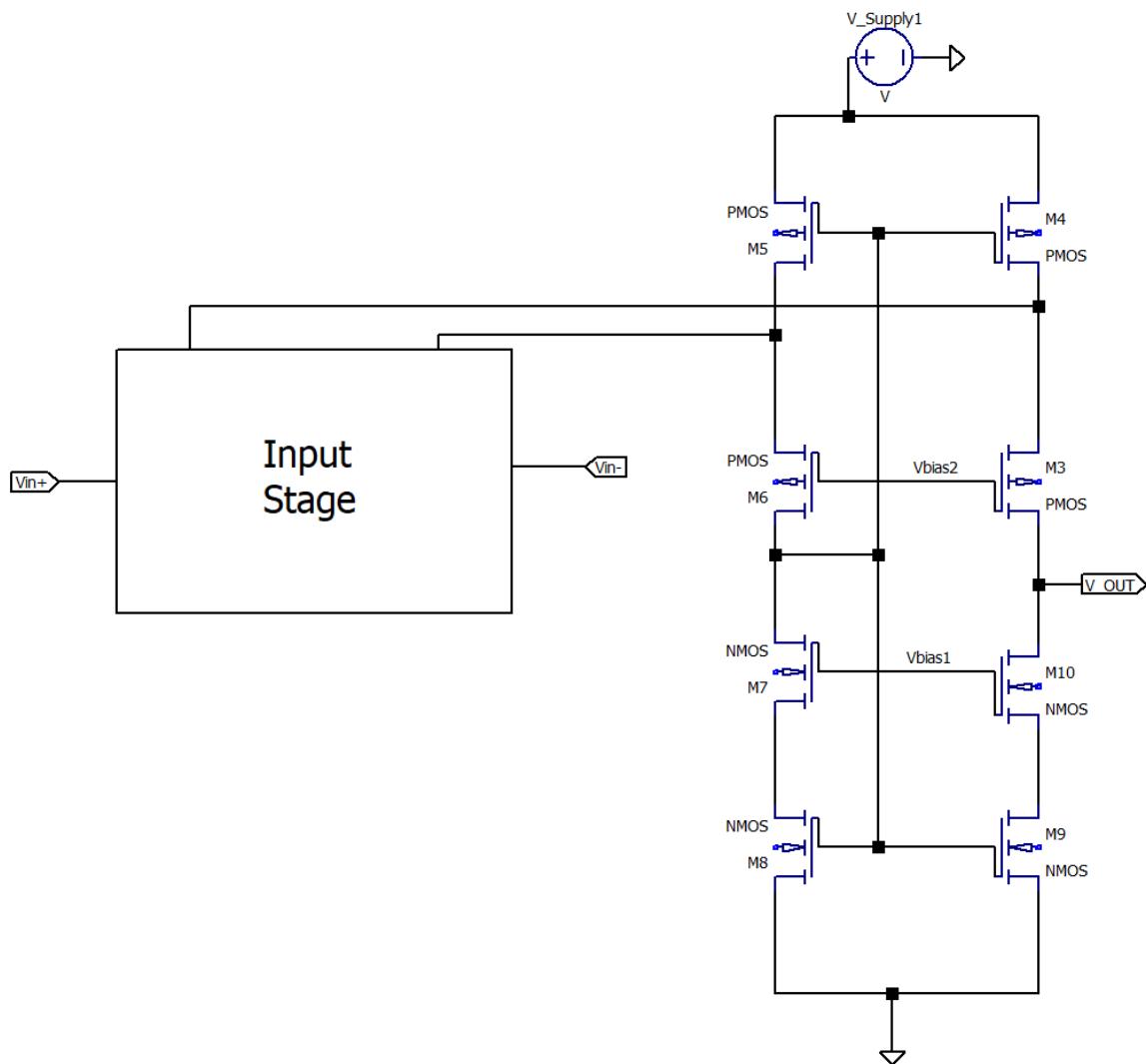


Figure 9: Folded Cascode with Input Stage [4]



## 2.4 2<sup>nd</sup> Stage

As a 2<sup>nd</sup> stage, active load differential amplifier, in *Figure 10*, is used. The purpose of this stage is mainly enhance gain/phase margin trade-off and bandwidth. of the OP-AMP. Since 1<sup>st</sup> stage is used to obtain 100dB gain, phase margin converges to zero. As a solution to enhance bandwidth another gain stage is added. To obtain better stability (phase margin in other words) miller capacitance is placed. Thanks to miller capacitance, dominant pole push up to 80Hz, so gain bode plot start to decrease earlier, and where the phase reach -180 degree, it has already drop below to the value of unity gain. Further analysis will cover in *Section 4*.

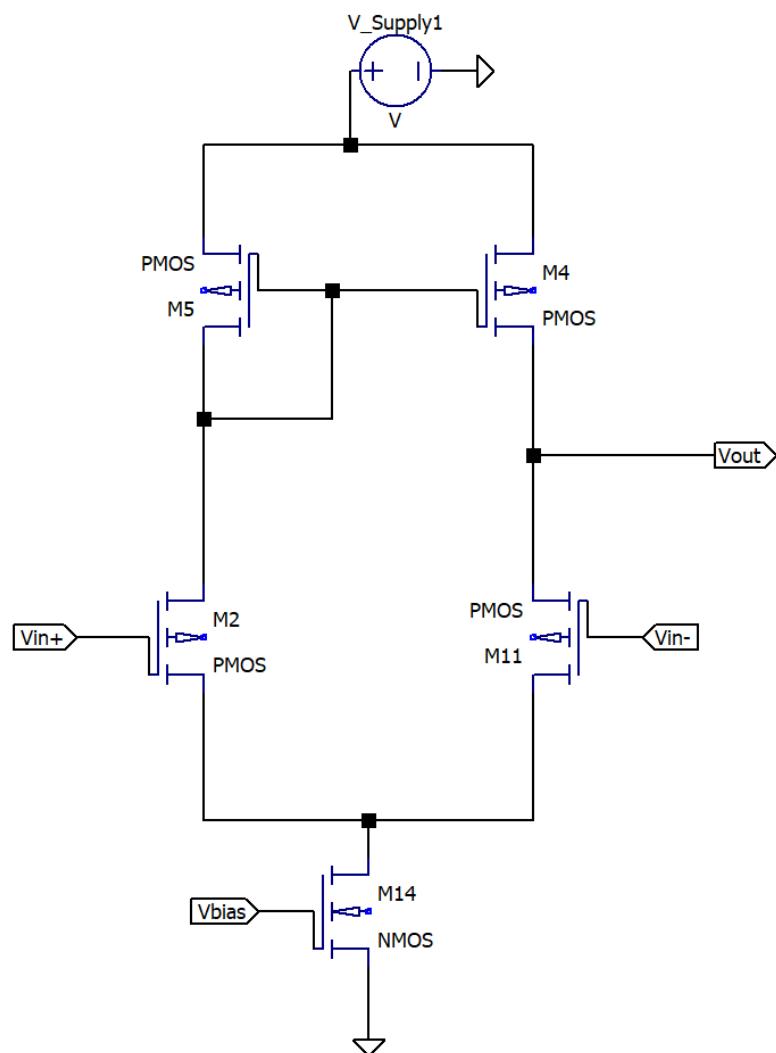


Figure 10: Active Load Differential Amplifier [??]



## 2.5 Finalized Design

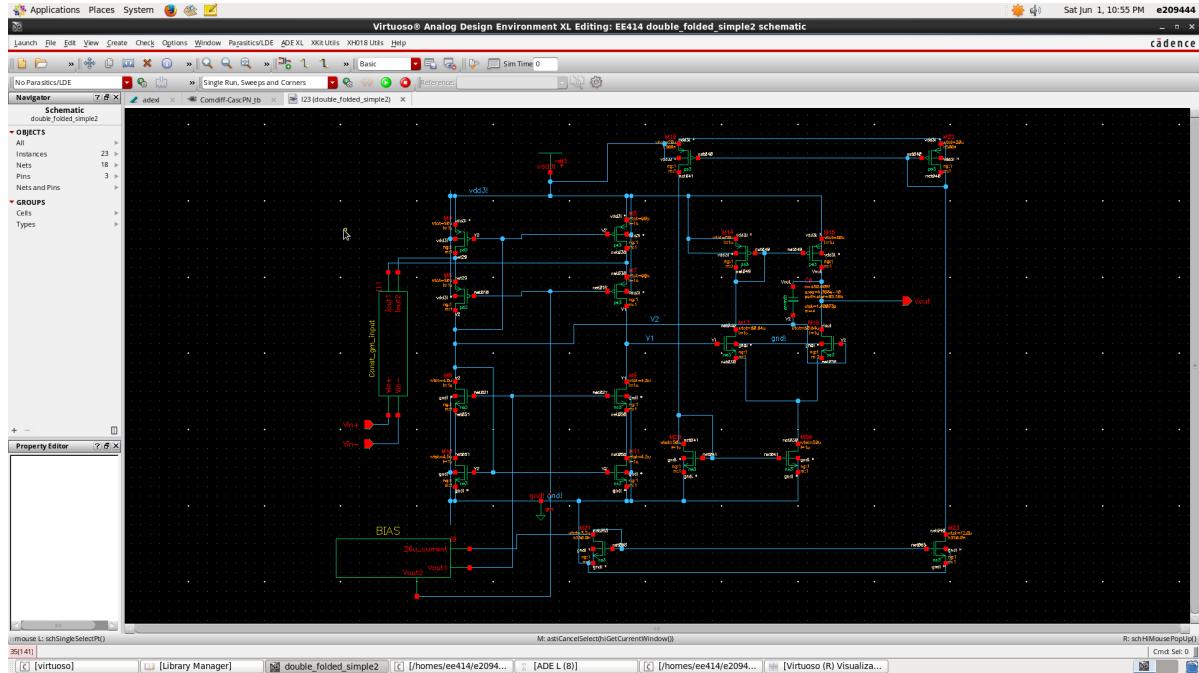


Figure 11: Finalized Design of the Operational Amplifier

## 3 Overall Specifications

Table 3: Design Specifications

Specification	Requirement	Actual Design
Supply Voltage	$3.3\text{ V} \pm 10\%$	$3.3\text{ V} \pm 10\%$
Maximum Power Dissipation	< 5 mW	1.6 mW
DC Gain	> 100 dB	106.33 dB
Phase Margin	> 60°	69.28°
Unity Gain-Bandwidth	> 100 MHz	<b>12.3</b> Mhz
Slew Rate	> $20\text{V}/\mu\text{sec}$	<b>8.41</b> $\text{V}/\mu\text{sec}$
PSRR	> 70 dB	105 dB
CMRR	> 70 dB	200 dB
Load Capacitance ( $C_L$ )	10 pF	10 pF
Input Common Mode Range	Rail-to-Rail	Almost Rail-to-Rail



## 4 Results for Verification Tests

Test bench of the OP-AMP design is shown *Figure 12*, thanks to 3 supply, frequency domain analysis and transient sinusoidal and pulse input analysis were done.

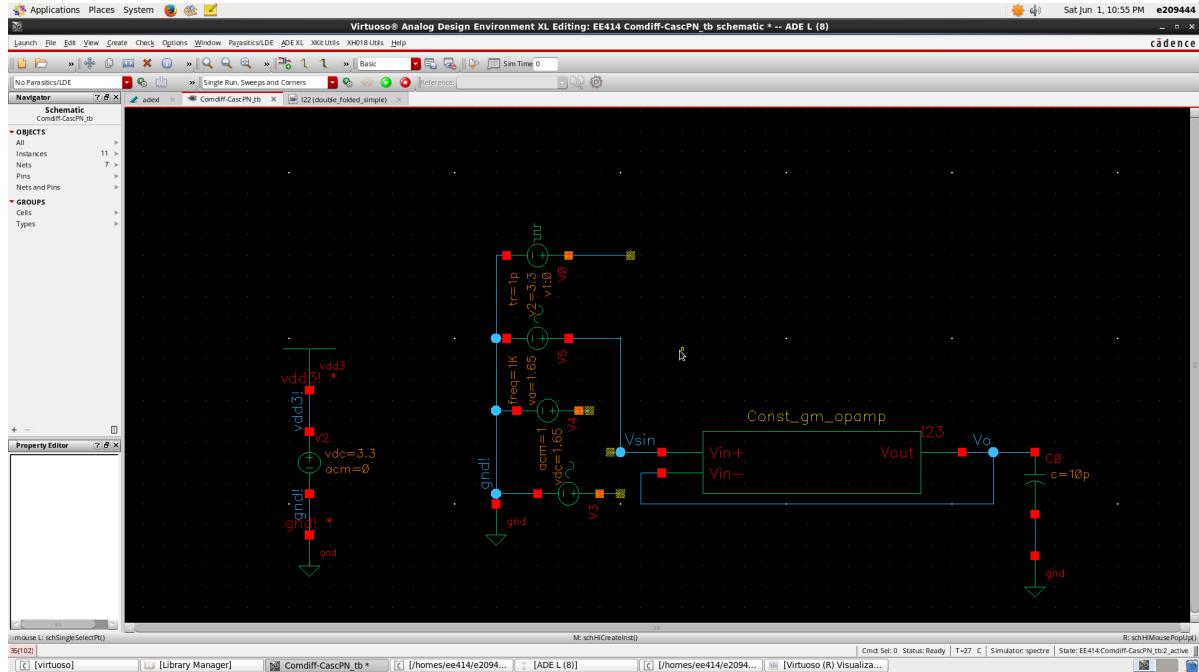


Figure 12: Test Bench Set-Up for Tested Op-Amp

### 4.1 Supply and Temperature Dependency of Bias Stage

In this section biasing sub-section of the OP-AMP is tested in variation of supply and temperature conditions. Required results are 5 percent changing for 10 percent change in supply, and 10 percent change for temperature is swepted 0 to 80 degree Celsius.

- According to *Figure 13* and *Figure 16*, 1V bias circuit's supply dependency is 1.4 percent while temperature dependency is 2 percent.
- According to *Figure 14* and *Figure 17*, 2V bias circuit's supply dependency is 2.3 percent while temperature dependency is 6.6 percent.
- According to *Figure 15* and *Figure 18*,  $26 \mu\text{A}$  bias circuit's supply dependency is 3% while temperature dependency is 1.13 percent.

These values are provide enough isolation from temperature and supply.



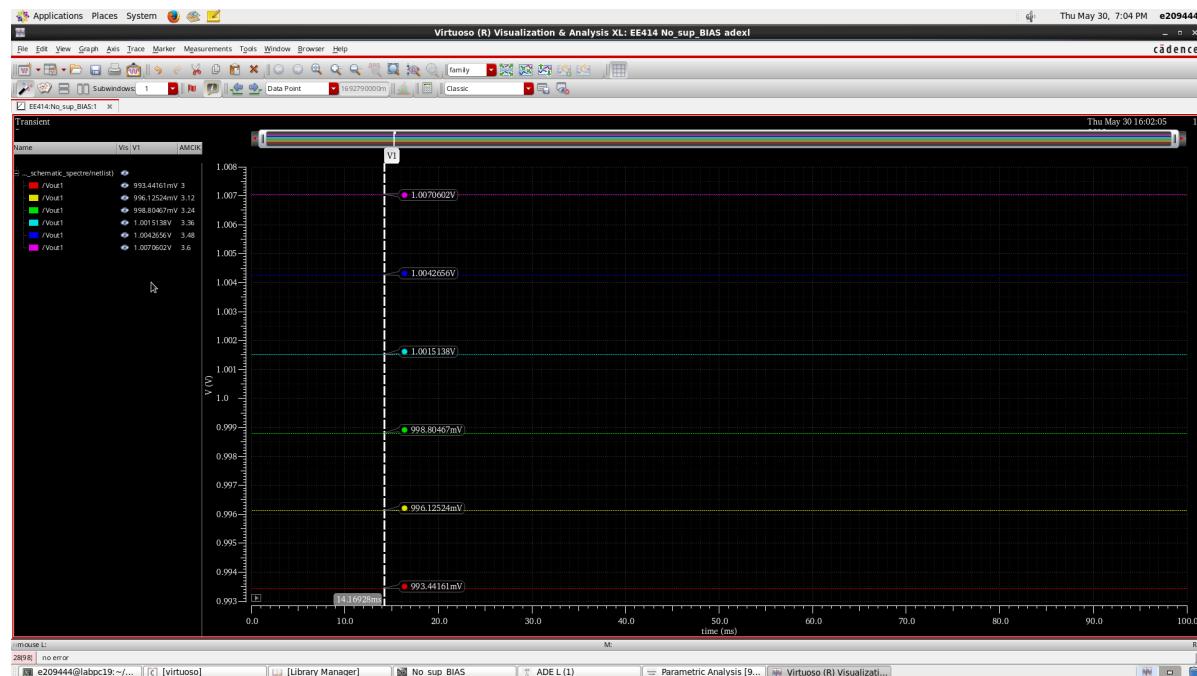


Figure 13: Supply Dependency Test of 1V Bias Voltage

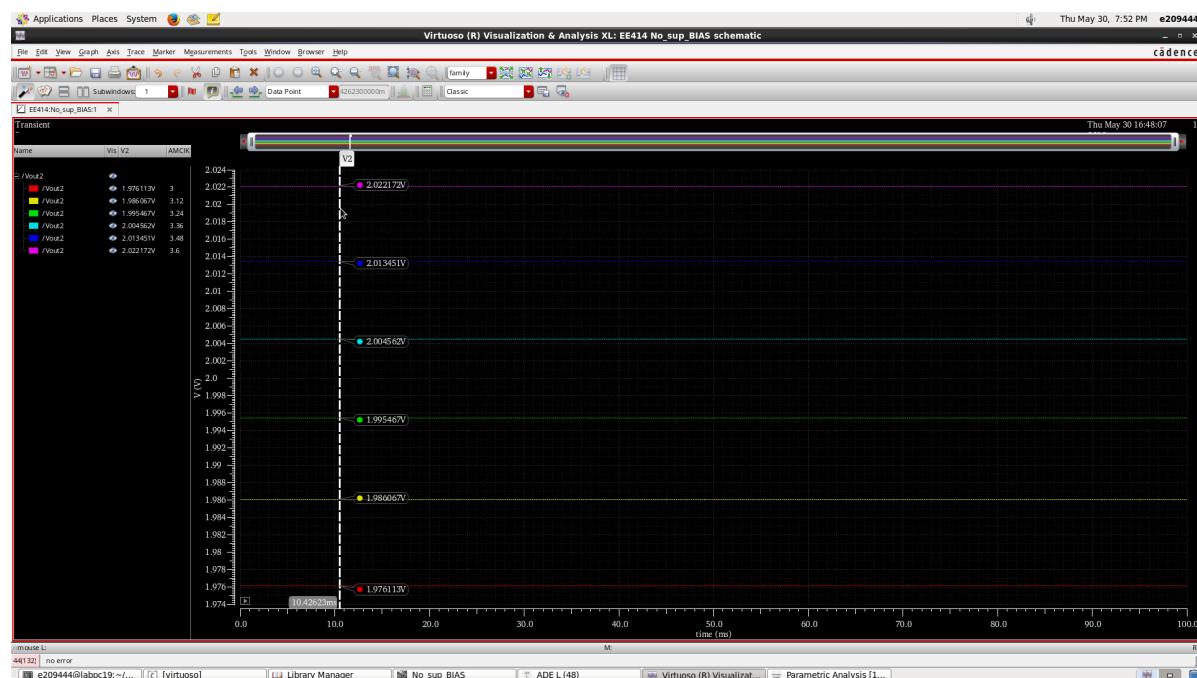


Figure 14: Supply Dependency Test of 2V Bias Voltage





Figure 15: Supply Dependency Test of  $26 \mu\text{A}$  Bias Current

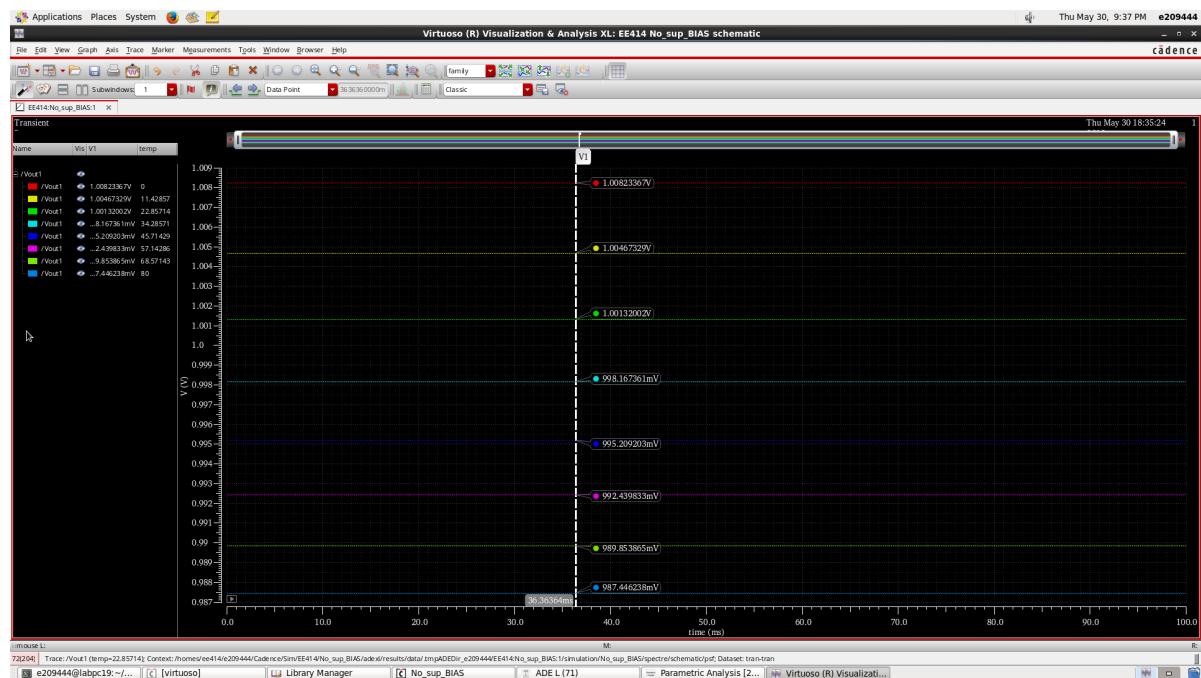


Figure 16: Temperature Dependency Test of 1V Bias Voltage



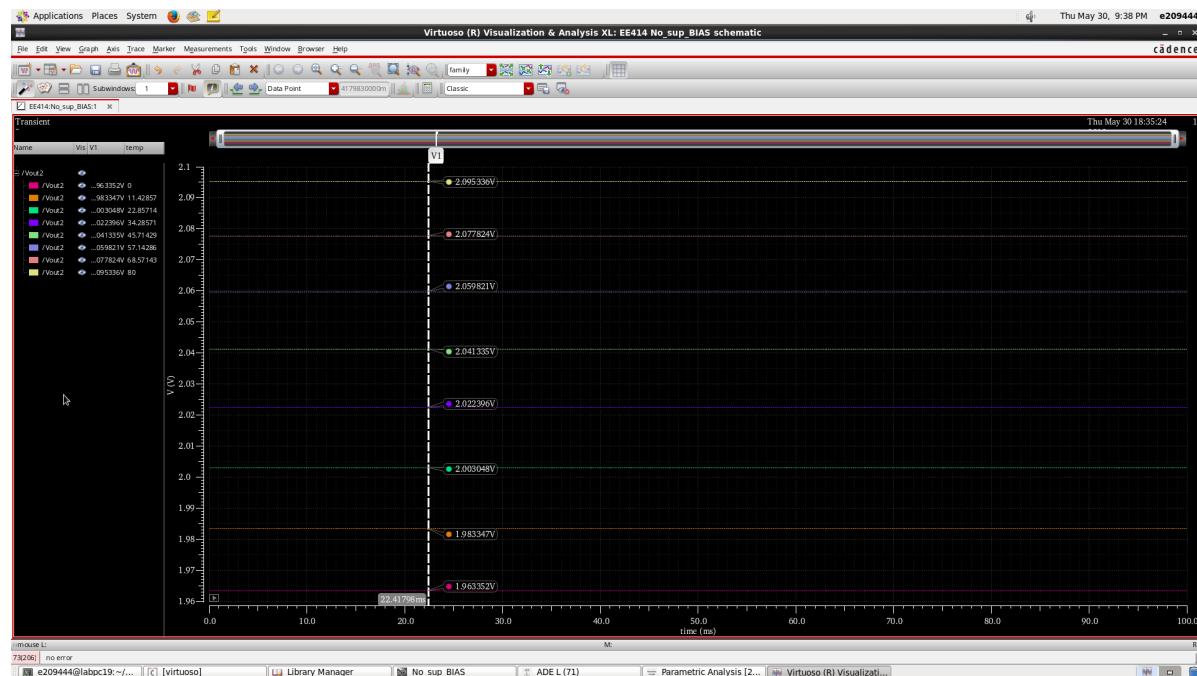


Figure 17: Temperature Dependency Test of 2V Bias Voltage



Figure 18: Temperature Dependency Test of  $26 \mu\text{A}$  Bias Current



## 4.2 Buffer Configuration Tests

In this section transient performance of the design is tested. In buffer configuration, system should follow the input at the output without distortion in ideal case. The test result at *Figure 19* proves that the circuit can operate at buffer configuration without any delay or clipping.

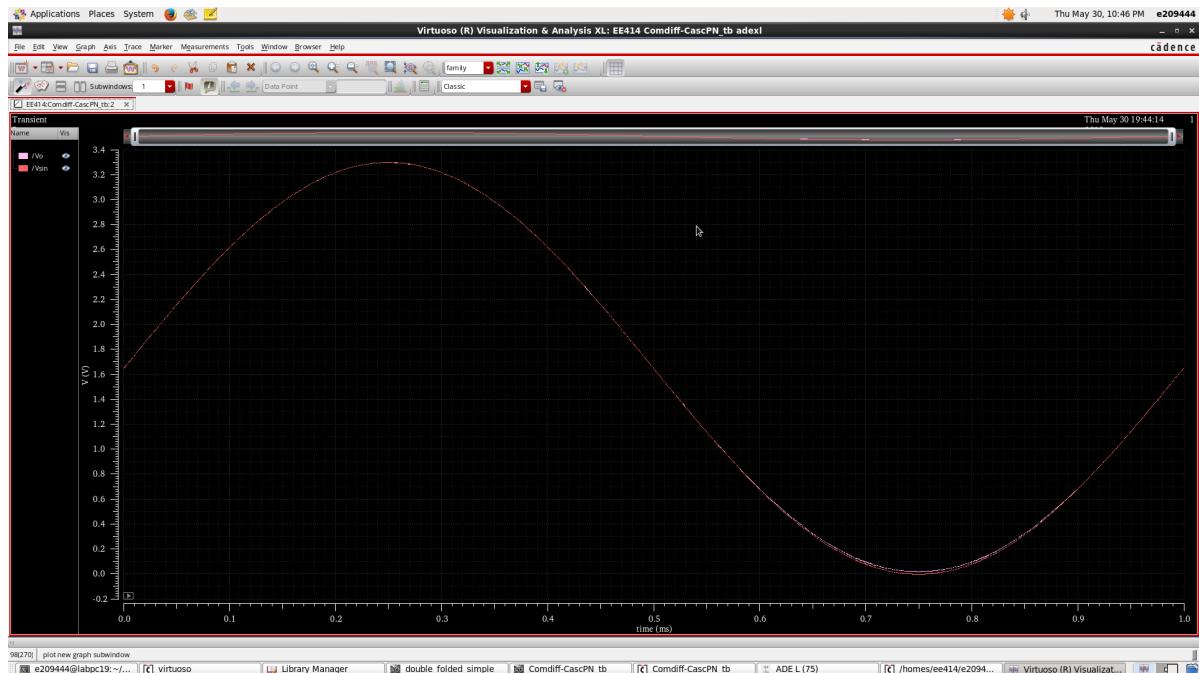


Figure 19: Buffer Configuration Test Result for the Op-Amp

To push the limitations of our amplifier, we have analyzed the Op-Amp at this configuration with different input signal frequencies. As can be seen in *Figure 20*, design can follow 1KHz signal without delay. Although almost no clipping at the top of the signal, lower section is clipped to the 15mV. Due to the  $V_{ds}$  values of the NMOS transistors and current supply from bottom, output voltage can not drop lower than this value.

Moreover, as seen in *Figure 21*, 200KHz sinusoidal signal tracking starts to fail and at the lower sections (below 0.6V) significant delay can be seen. Finally, as seen in *Figure 22*, 1MHz signal tracking does not seem good enough. At this stage, upper section has basic delay, but lower section lost their form to track input.



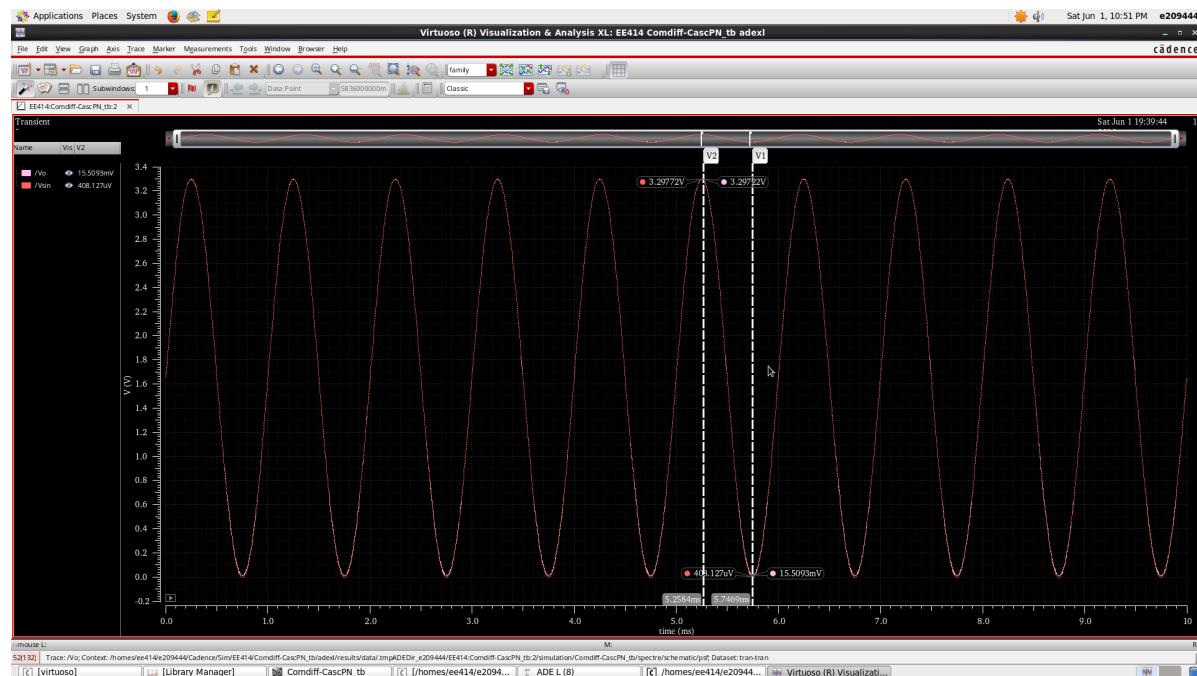


Figure 20: 1 KHz Sinus Input Track Test at Buffer Configuration

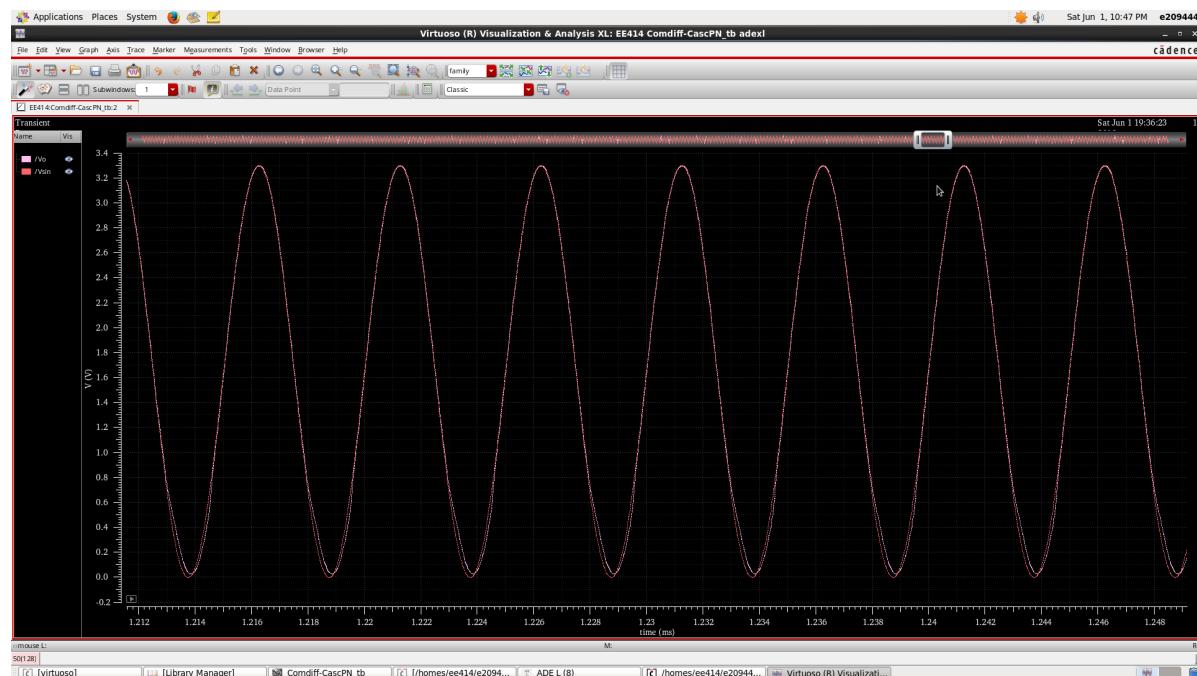


Figure 21: 200 KHz Sinus Input Track Test at Buffer Configuration



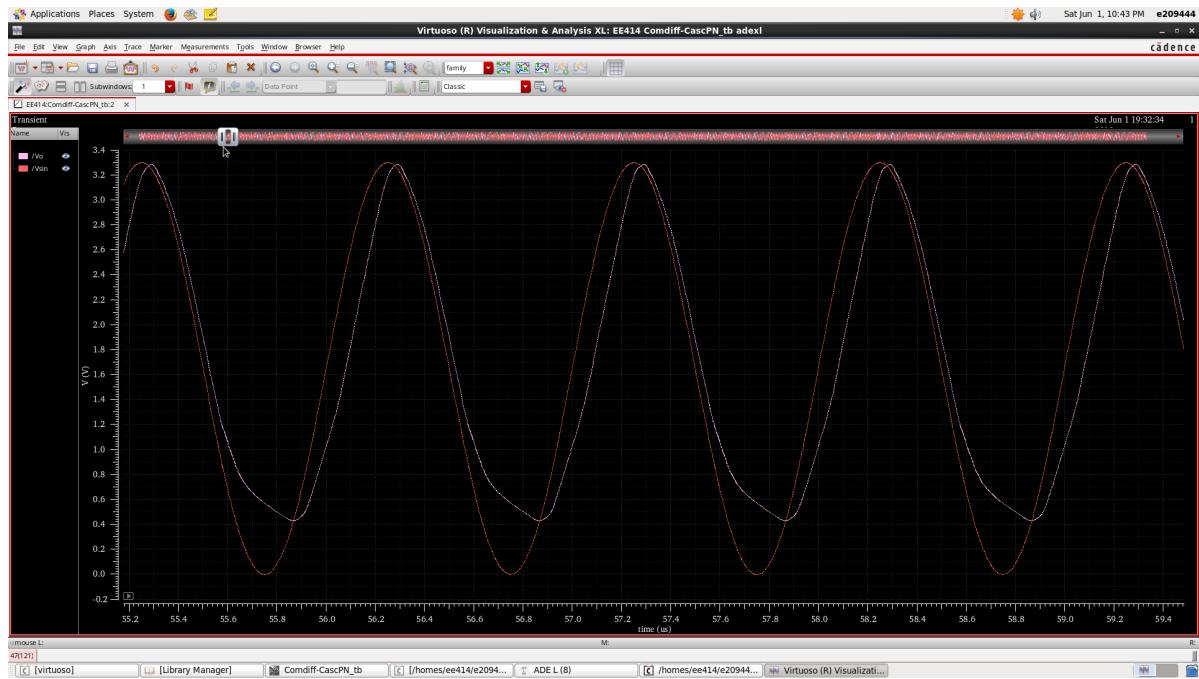


Figure 22: 1 MHz Sinus Input Track Test at Buffer Configuration

### 4.3 Amplification Tests

In this section small signal amplification performance of the design is tested. As seen in *Figure 23*, 10  $\mu$ V sinusoidal input signal was amplified without any distortion. Then, to test the limitations of our design, we have tested the circuit with other sinusoidal with higher frequencies. As seen in *Figure 24*, 70  $\mu$ V sinusoidal input signal was also amplified almost perfectly, *Figure 25* shows this amplification of this signal at full scale. *Figures 23 & 24* also verify our gain expectations. However, due to high gain of our Op-Amp high voltage signals such as 10mV peak-to-peak sinusoidal signals were saturated at the output.



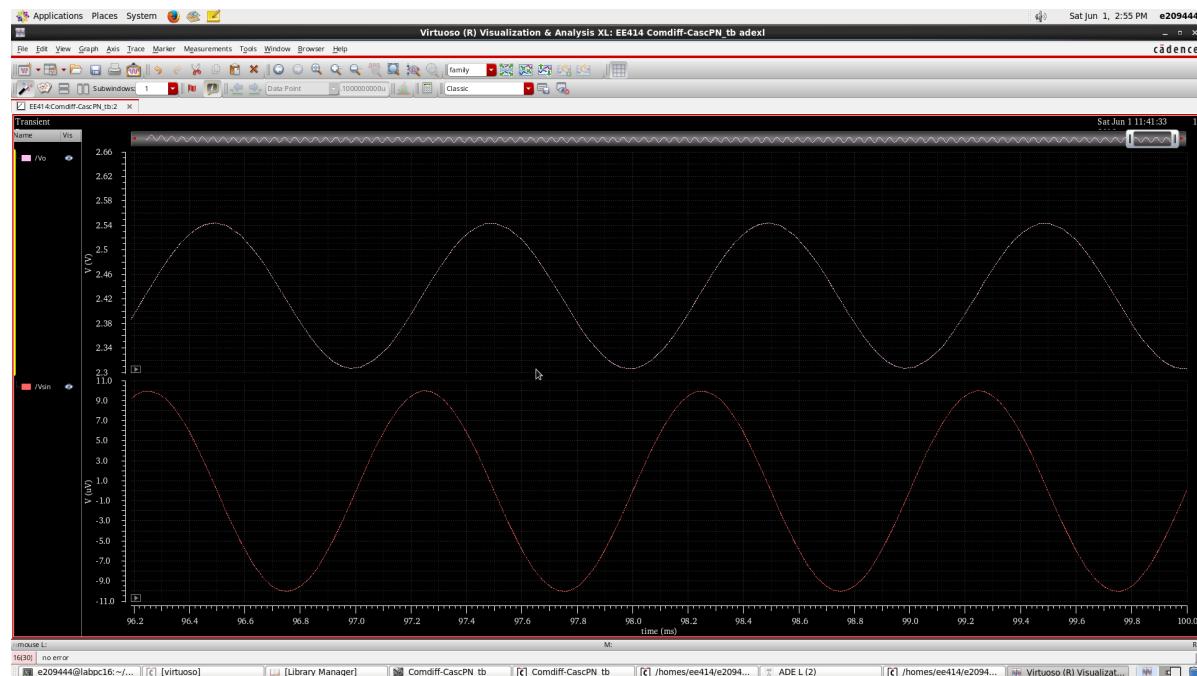


Figure 23: 10 $\mu$ V Input Amplification Test Result

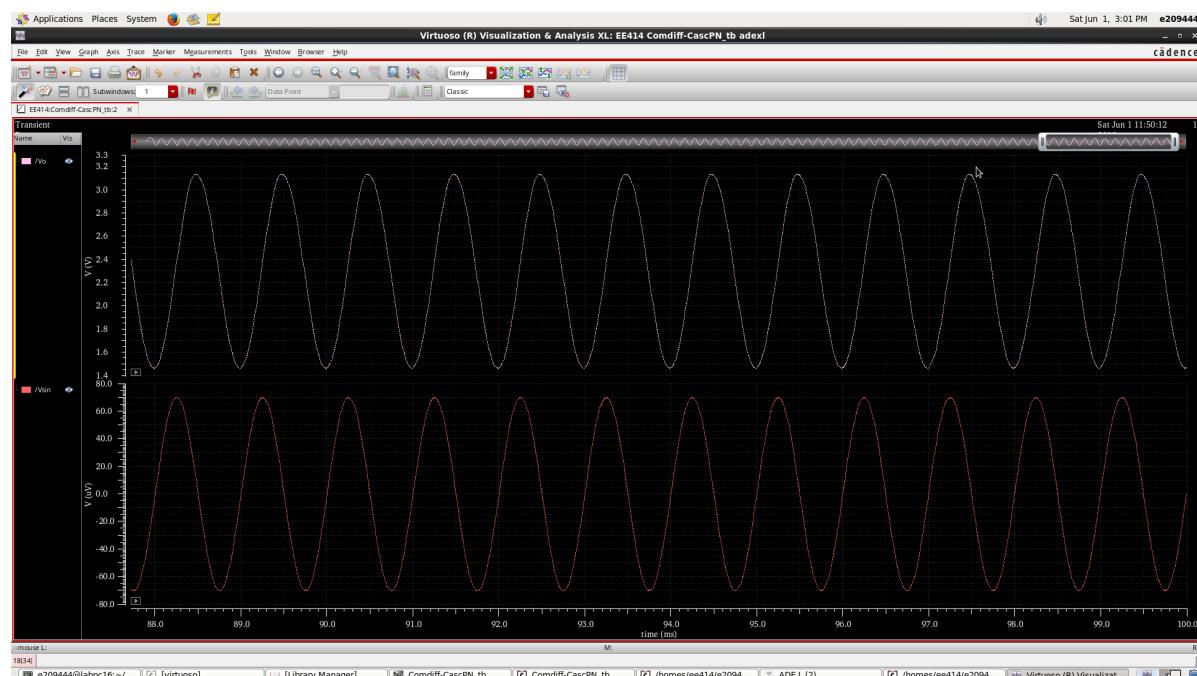


Figure 24: 70 $\mu$ V Input Amplification Test Result



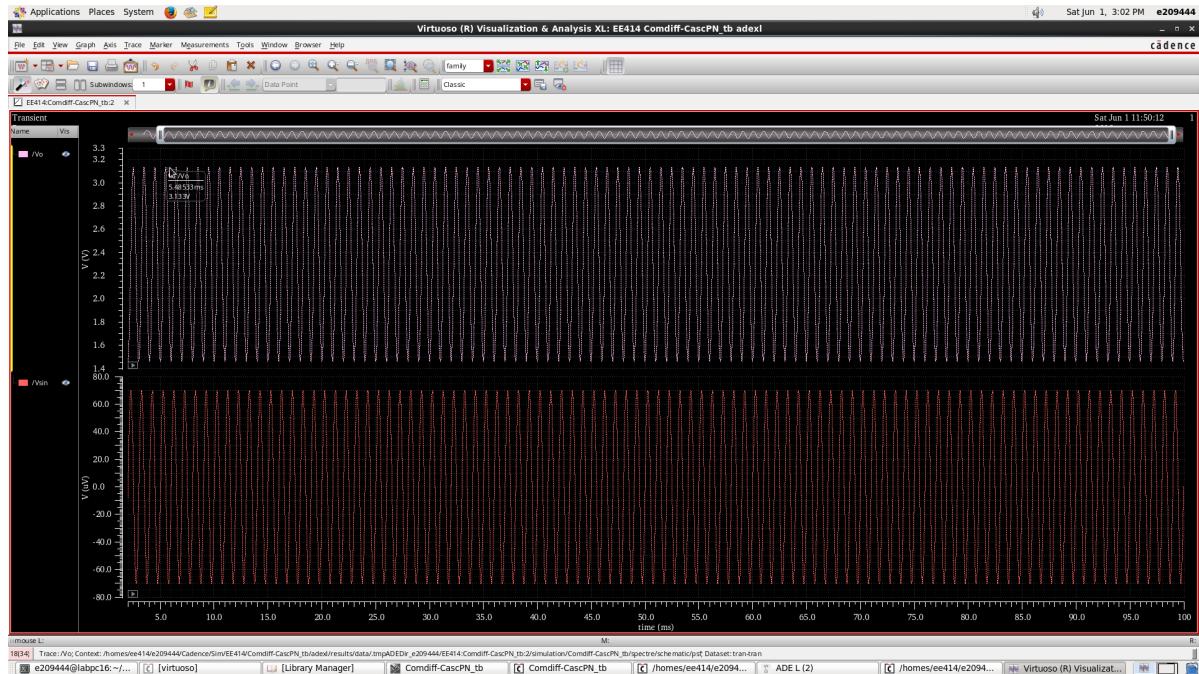


Figure 25:  $70\mu V$  Input Amplification Test Result at Full Scale

#### 4.4 Frequency Analysis Tests

In this section, frequency response of the design is tested. According to *Figure 26*, our design has  $69.23^\circ$  phase margin and 12.3 MHz unity gain band-width. Besides, DC gain of the design is 105dB. Then, to check input common mode range, input voltage is swepted from 0V to 3.3V, according to *Figure 27*, for different common mode voltages unity gain band-width varies from 12MHz to 14MHz, while phase margin varies between  $80^\circ$  to  $16^\circ$ . Moreover, as can be seen in *Figure 28*, for different input common mode voltages DC gain changes between from 105dB to 102dB, which is only 2.85% variation.





Figure 26: Band-with Test Results of the Op-Amp at Ideal Conditions



Figure 27: Input Common Mode Range Test Result



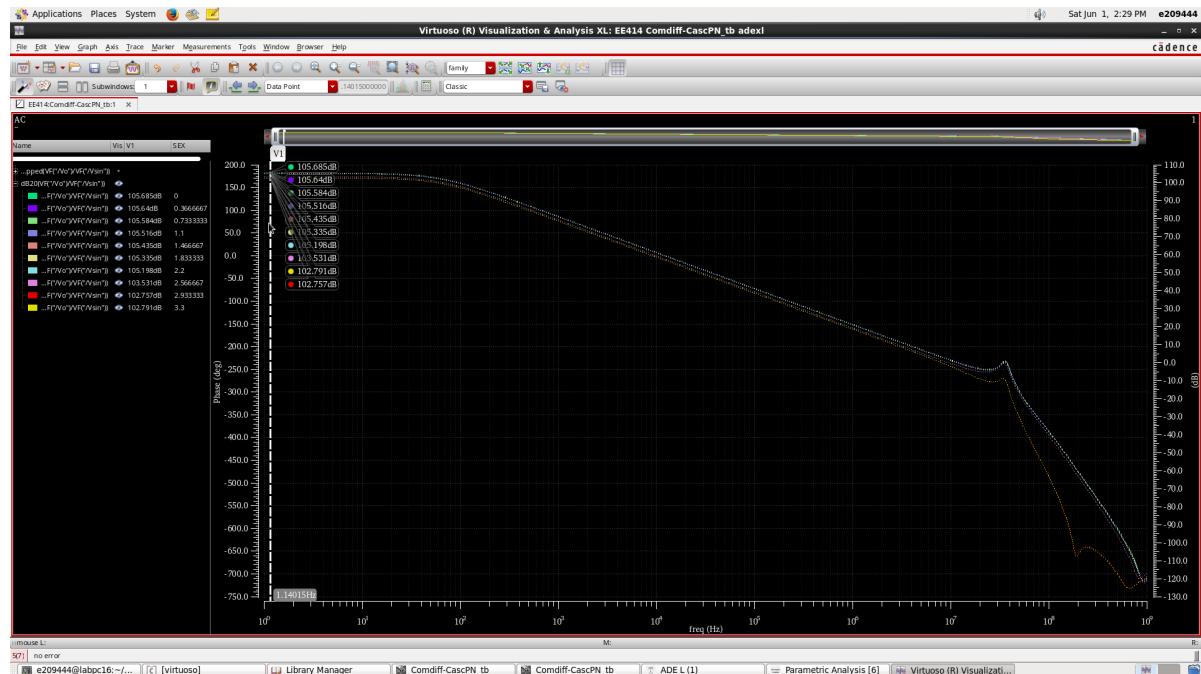


Figure 28: DC Gain Variation at Input Common Mode Range Test

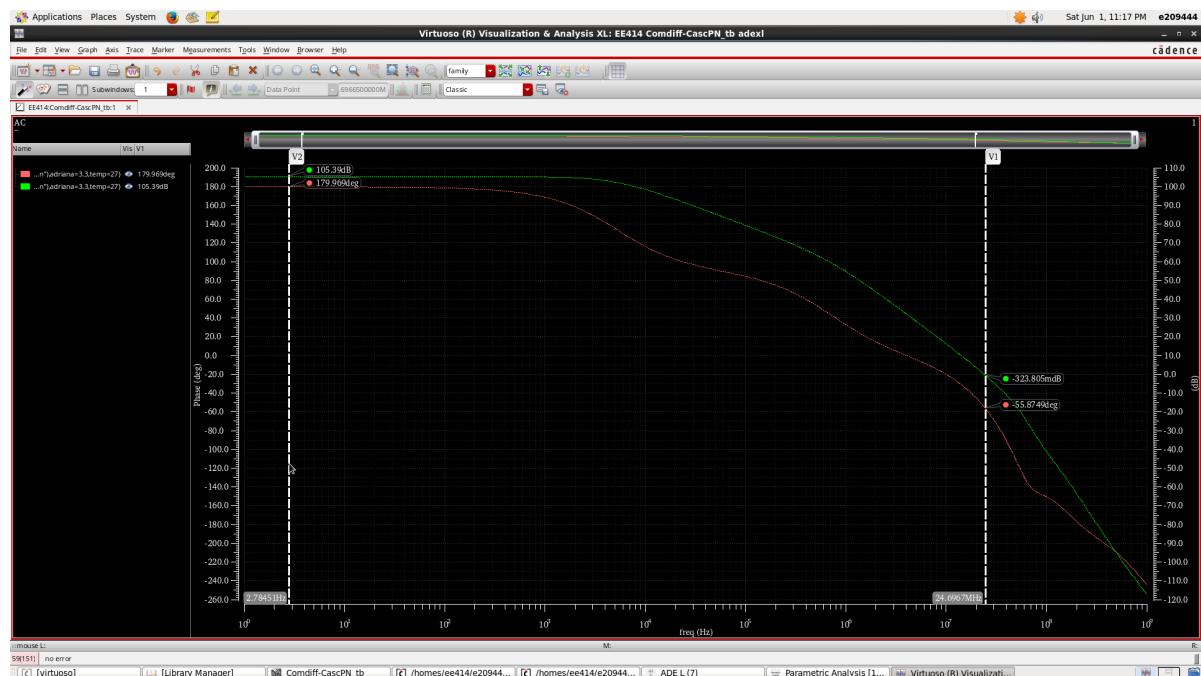


Figure 29: Frequency Response of the Op-Amp without Compensation Capacitor



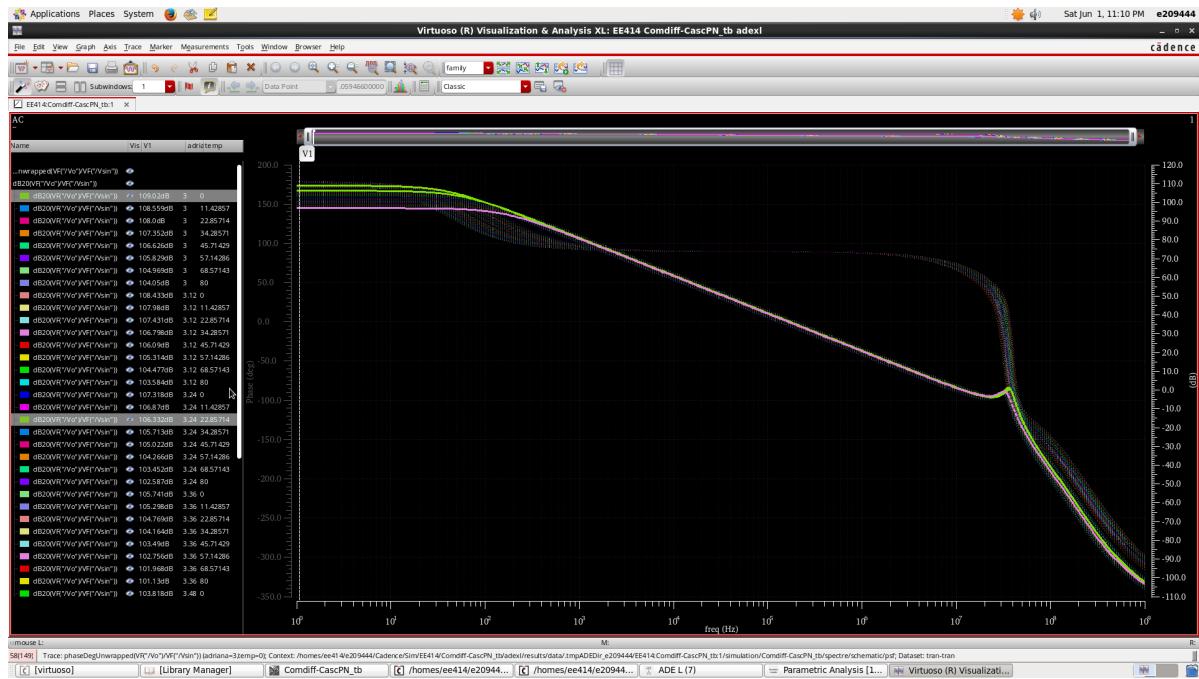


Figure 30: Temperature and Voltage Dependency of Frequency Response of the Op-Amp at Low Temperatures

*Figure 29* shows the frequency response of the overall design without compensation capacitor. In this configuration, unity-gain bandwidth extent up to 25MHz, however, phase margin is around -55 degree which means design is unstable. This shows the importance of the compensation for the design.

Finally, to test the overall dependency of the design, input voltage and temperature is sweeped at their full scale respectively. Results in the *Figures 31 & 31* proves that overall design performance quiet insensitive against changes variations in temperature and supply voltage thanks to biasing circuit isolation.



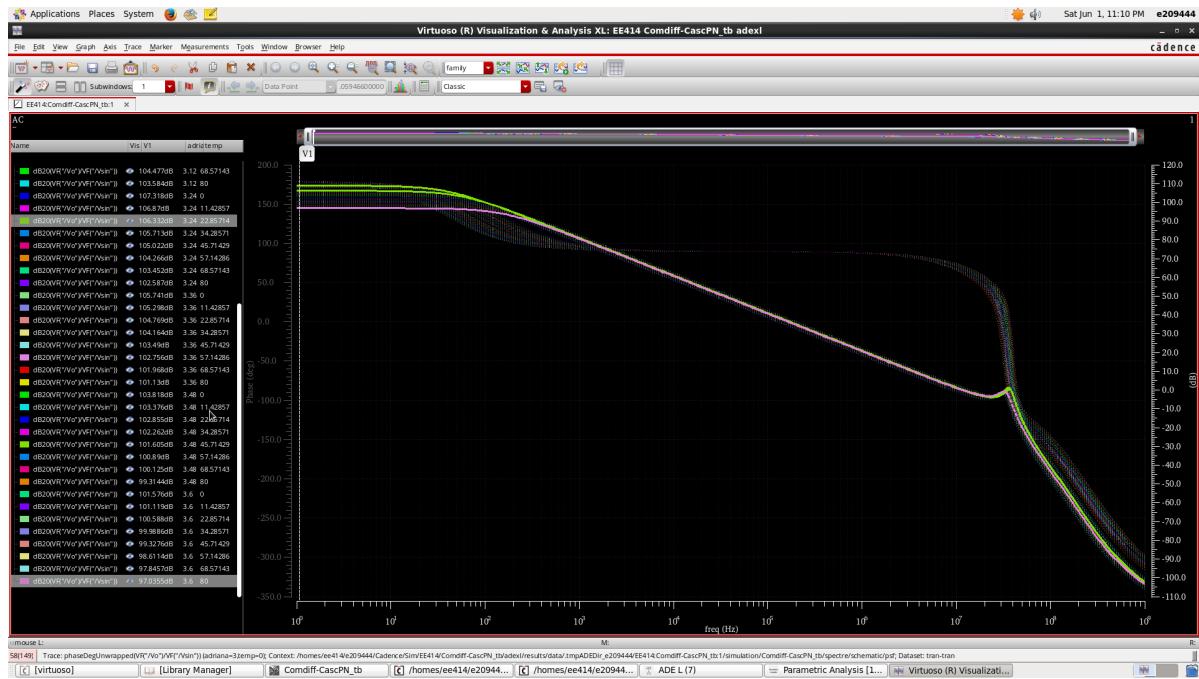


Figure 31: Temperature and Voltage Dependency of Frequency Response of the Op-Amp at High Temperatures

#### 4.4.1 Overall Dependency Tests

In this section, CMRR, PSRR and overall temperature/supply dependency of the OP-AMP is covered. As seen in *Figure 32*, at low frequency CM gain is -97dB, so CMRR value is equal to 200dB. However, at high frequencies CM gain increase up to -10dB, in this case CMRR value is equal to 115dB. As seen in *Figure 33*, power supply amplification is around -170mdB over a very large frequency scale, so PSRR value is equal to 105dB.





Figure 32: CMRR Test Result of the Op-Amp



Figure 33: PSRR Test Result of the Op-Amp



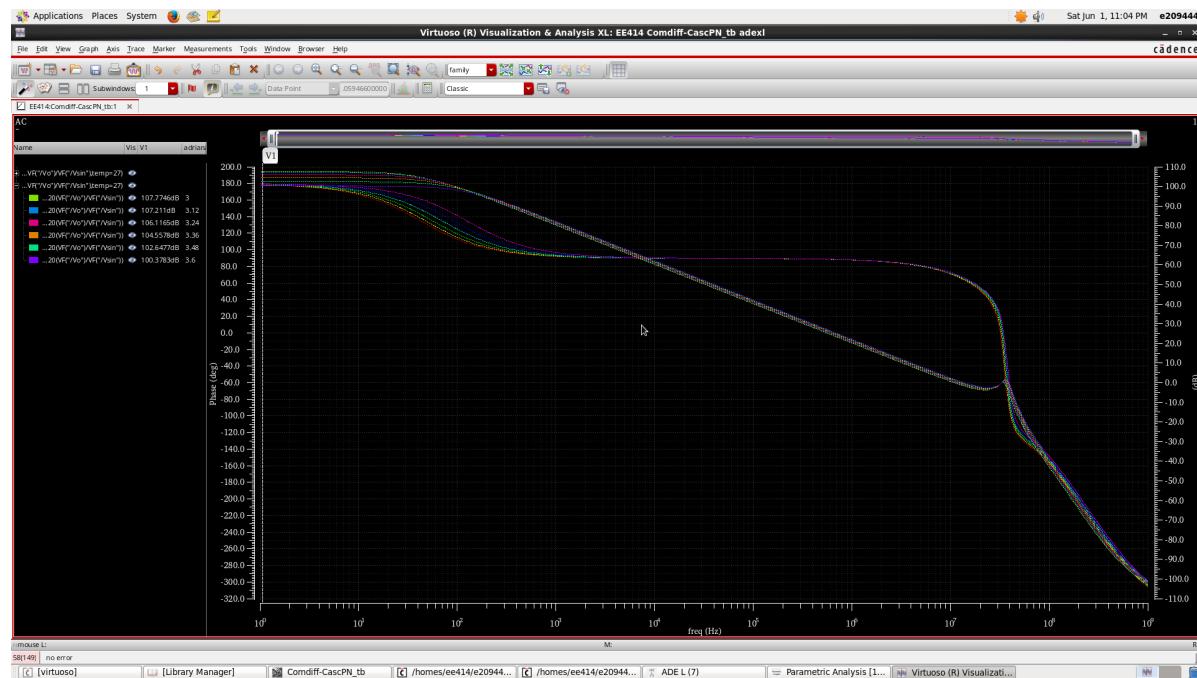


Figure 34: Supply Dependency of the Overall Op-Amp

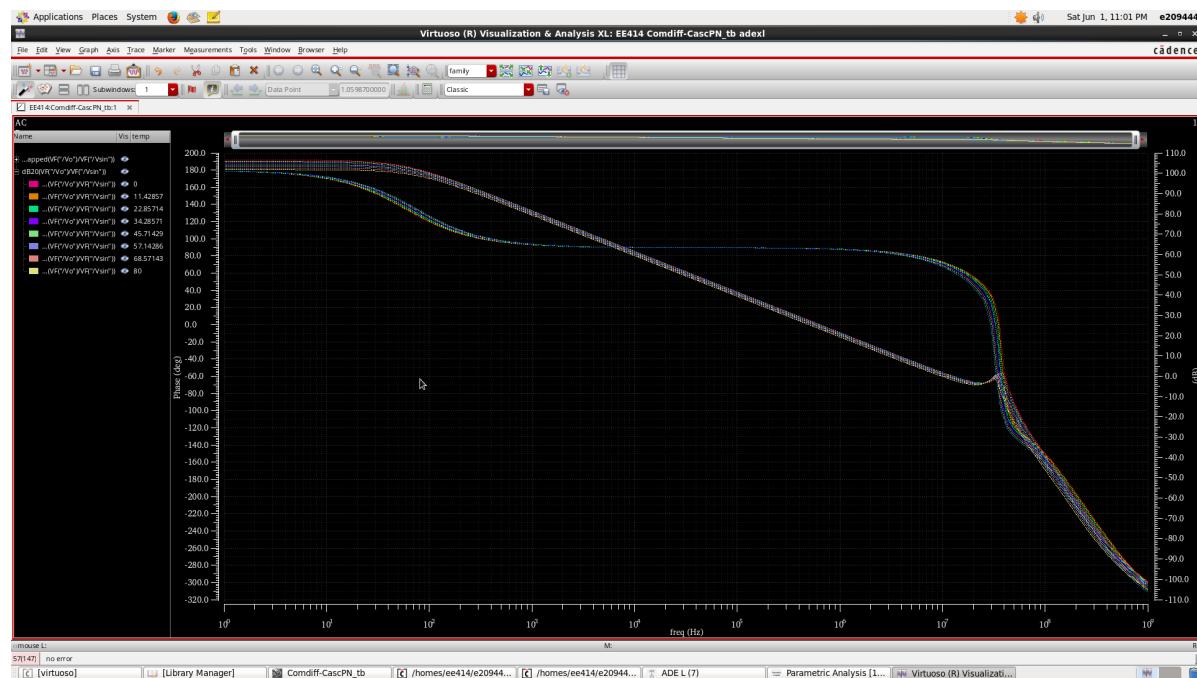


Figure 35: Temperature Dependency of the Overall Op-Amp



## 4.5 Slew Rate Analysis

As can be seen from the *Figure 36*, slew rate performance of the design is around 8V /  $\mu$ sec for both cases, namely, input low to high and input high to low.

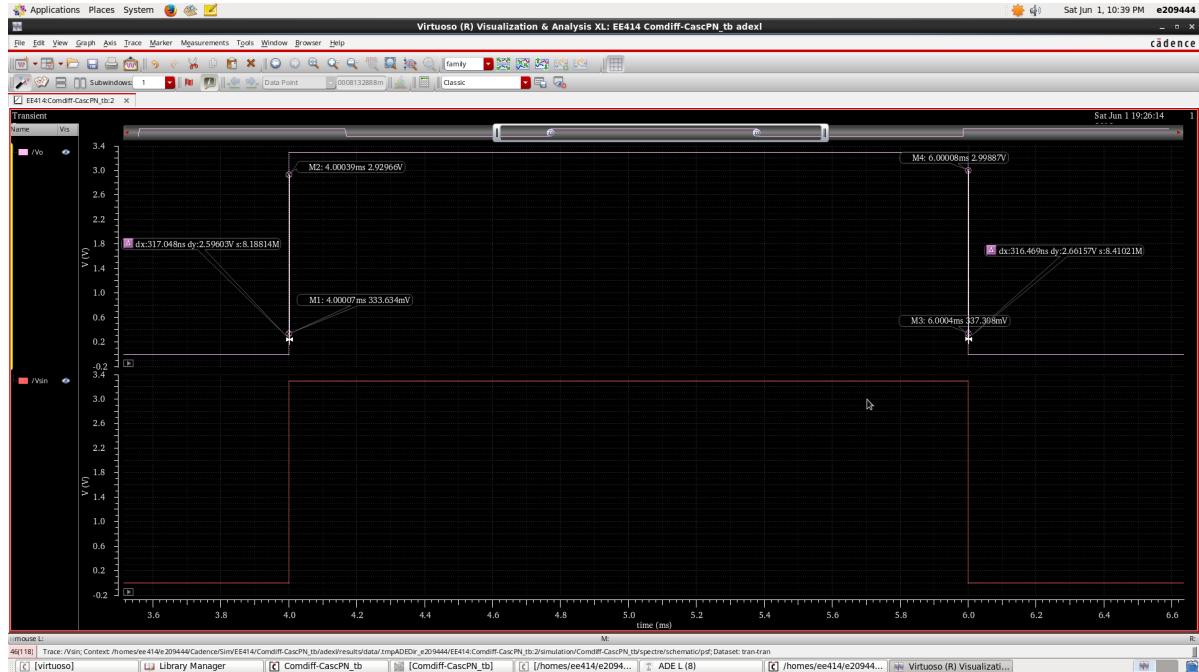


Figure 36: Slew Rate Test Results of the Op-Amp

## 4.6 Power Analysis

In this section, overall power consumption of the OP-AMP is covered for different type of input signals. The consumption under different conditions can be examined at *Table 4*. Actual results can be investigated from *Figures 37 to 40*.

Table 4: Power Analysis of the Op-Amp with Different Input Signals

Input Type	Connection Type	Power Dissipation
DC	Buffer	1.562 mW
Square (Large Signal)	Buffer	1.193 mW
Sinusoidal (Large Signal)	Buffer	1.607 mW
Sinusoidal (Small Signal)	Amplifier	1.607 mW
Average		1.492 mW



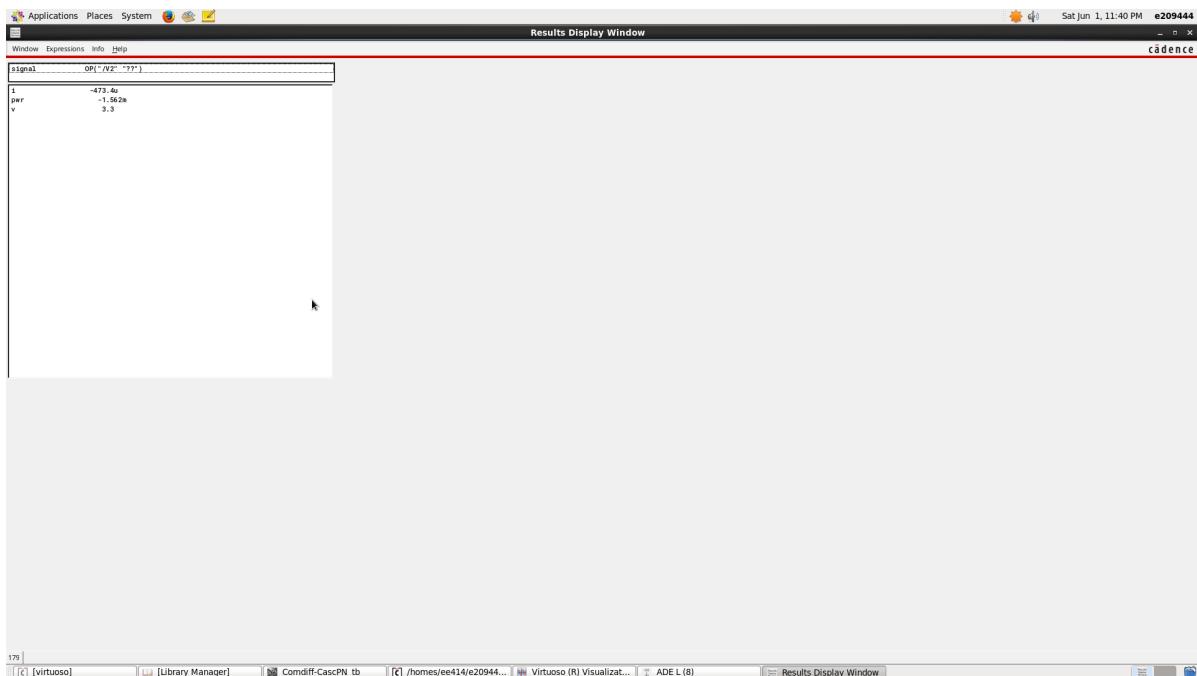


Figure 37: Power Consumption of Design for DC Input

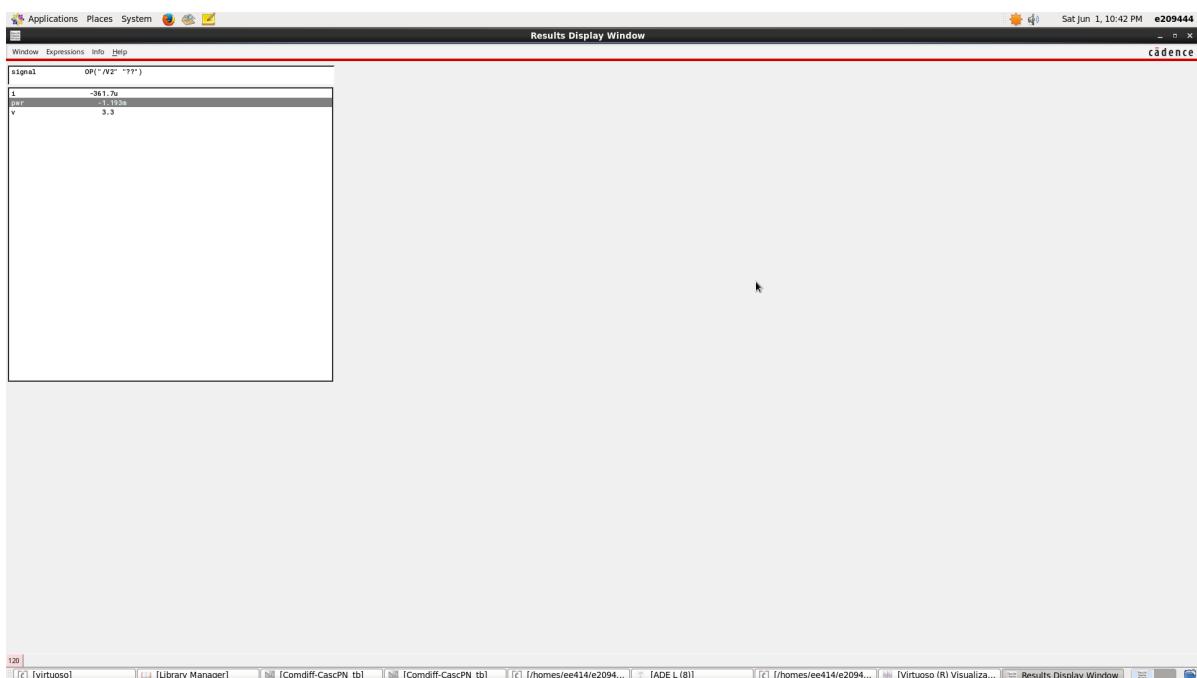


Figure 38: Power Consumption of Design for Square Input



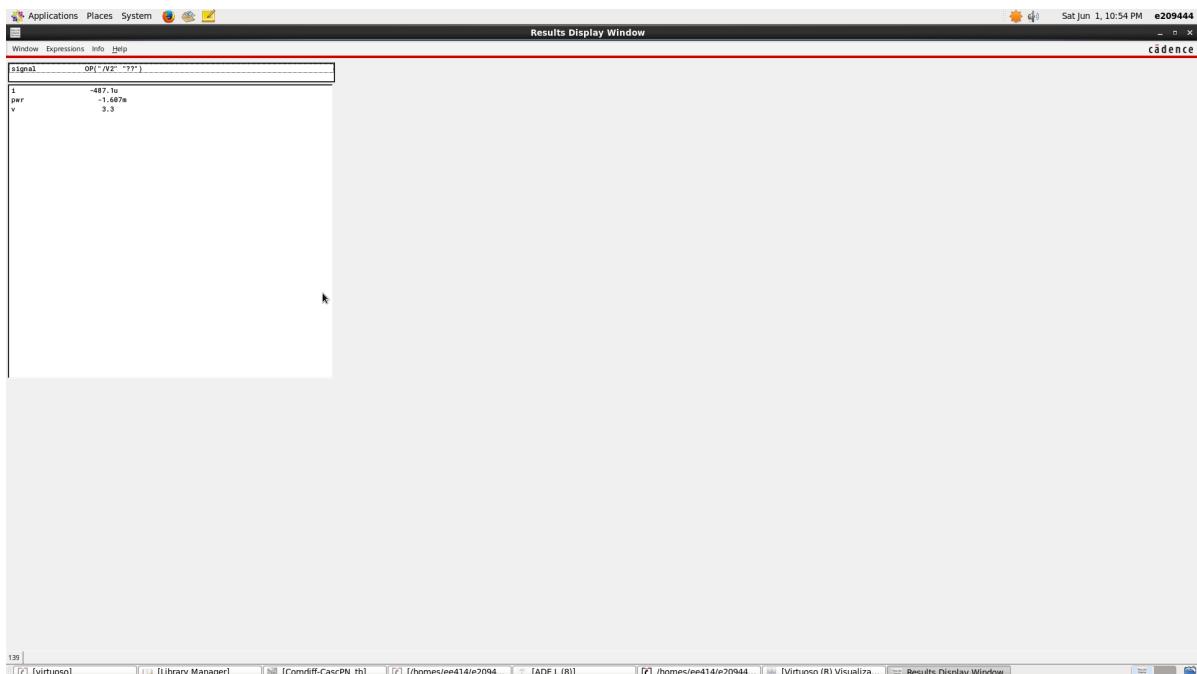


Figure 39: Power Consumption of Design for Sinusoidal Input

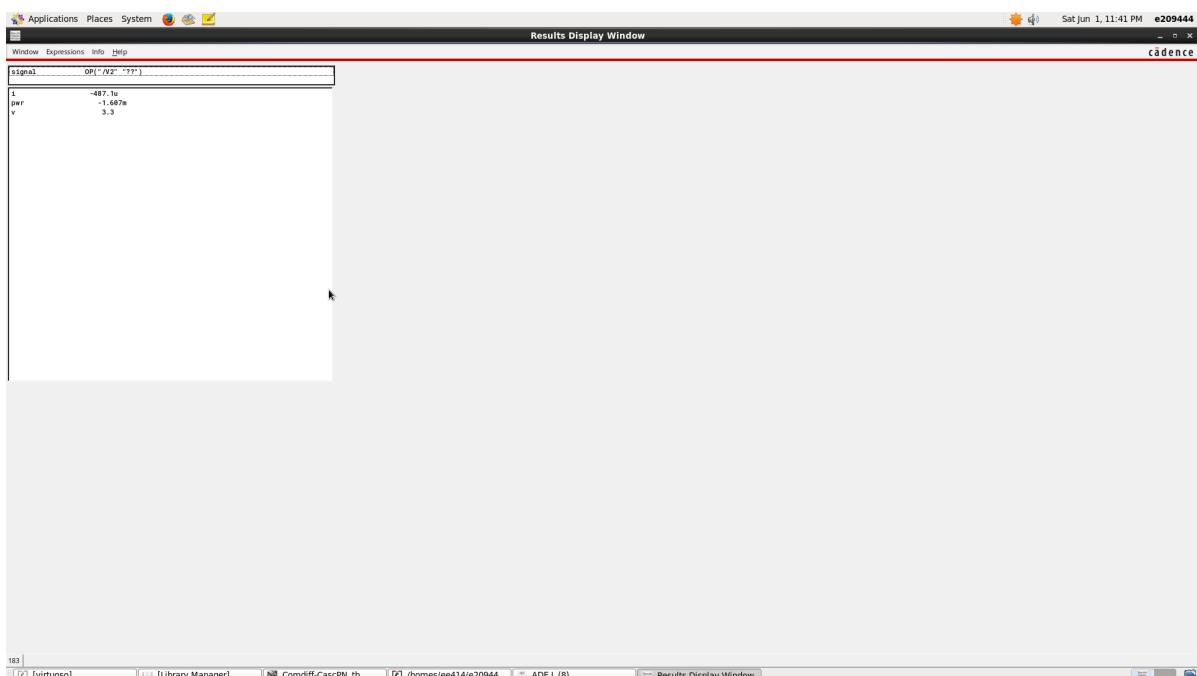


Figure 40: Power Consumption of Design for Small Signal Smplification



## 5 Conclusion

All in all, OP-AMP is designed according to given specs. However, all of the specs are impossible to satisfy, so power consumption, stability (phase margin), gain, PSRR, CMRR, Load performance, common mode input range, biasing specs are satisfied. The other parameters such as slew rate, gain-bandwidth product are sacrifice.

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