Postlab 1

1. What are the GPIO control registers that the lab mentions? Briefly describe each of their functions.

GPIOx_MODER - without configuring this register, using GPIO pins as anything aside from digital inputs is not possible.

GPIOx OTYPER - This register selects the output mode you want for each pin.

GPIOx_OSPEEDR - disables and/or reduces the speed of the peripherals, like putting them in low or high speed.

GPIOx_PUPDR - This register connects internal pull-up or pull-down "resistors" to a pin;

GPIOx_IDR – Read only bit that reports the logical state of each pin in the GPIO port.

GPIOx ODR - This register sets the logical state of configured output pins.

GPIOx_BSRR - This register is write-only: the reason is that this register is a shortcut to set and clear bits quickly in the output register.

GPIOx_LCKR - The configuration lock register locks the other configuration registers for the associated pin:

GPIOx_AFRL/GPIOx_AFRH - necessary to configure alternate functions for all 16 pins **GPIOx_BRR** - This reset-only register is essentially a copy but with the clearing bits in the lower half.

2. What values would you want to write to the bits controlling a pin in the GPIOx_MODER register in order to set it to analog mode?

0b11

3. Examine the bit descriptions in GPIOx_BSRR register: which bit would you want to set to clear the fourth bit in the ODR?

Bit 20

- 4. Perform the following bitwise operations:
- 0xAD | 0xC7 = 10101101 | 11000111 = 0b11101111
- 0xAD & 0xC7 = 10101101 & 11000111 = 0b10000101
- 0xAD & ~(0xC7) = 10101101 & ~11000111 = 0b00101000
- 0xAD ^0xC7 = 10101101 ^ 11000111 = 0b01101010
- 5. How would you clear the 5th and 6th bits in a register while leaving the other's alone? Register $\&= \sim (1 << 5 \mid 1 << 6)$
- 6. What is the maximum speed the STM32F072R8 GPIO pins can handle in the lowest speed setting?

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- Use the chip datasheet: lab section 1.4.1 gives a hint to the location. You'll want to search the I/O AC characteristics table. You will also need to view the OSPEEDR settings to find the bit pattern indicating the slowest speed.

 If V>=2 then the max frequency of max(IO)out is 2Mhz and if V<2 then it's 1Mhz
- 7. What RCC register would you manipulate to enable the following peripherals: (use the comments next to the bit defines for better peripheral descriptions)
- TIM1 (TIMER1)

RCC_APB2ENR

DMA1

RCCC_AHBENR

• I2C1

RCC_APB1ENR