Tenace Crane
ECE5780

Lab 3 Prelab

1. Relevant registers/configuration options, and summary of the output data produced.
2. Time-base unit
3. The PSC register divides the input clock frequency to the timer. The PSC can divide the input clock by any integer value that fits in its 16-bit width.
4. The value in the ARR register is the trigger point at which the timer resets and begins to count a new period.
5. The output compare mode modifies the output of a GPIO pin whenever the timer's counter matches the value stored in the CCRx register. Depending on the configuration, an output compare channel can set, clear, or toggle its pin on a counter match.
6. A high-frequency rectangular-wave signal where every period is a ratio of on and off time. Represents an analog voltage ranging between the low and high voltages of the digital signal.
7. Allowing a pin to connect directly to internal peripherals of the STM32F0.
8. STM32F072xB datasheet in table 13, STM32F072x8/xB pin definitions