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ECE5780

Lab 6 Prelab

1. Hysteresis changes the voltage threshold depending on the currently detected digital state. It moves the threshold around in order to be an improvement over simple thresholding which doesn't account for rapid transitions and noise ripples.
2. Quantization is the process of mapping a high-resolution signal to a manageable lower-resolution one.
3. Nyquist theory explains the relationship between how often you sample an input signal and whether or not you'll be able to tell what it is afterwards. Sampling too slowly doesn't represent the signals and can lead to something called aliasing.
4. 4096
5. The peripheral must be stopped, with no enable/set bits set other than in the RCC peripheral.
    a. 1. Ensure that ADEN = 0 and DMAEN = 0. 2. Set ADCAL = 1. 3. Wait until ADCAL = 0. 4. The calibration factor can be read from bits 6:0 of ADC_DR
6. • DAC_DHR8Rx – 8-bit right-aligned (data in bits 0-7)
   • DAC_DHR12Rx – 12-bit right-aligned (data in bits 0-11)
   • DAC_DHR12Lx – 12-bit left-aligned (data in bits 15-4)
   The left-aligned mode is typically used for selecting the upper bits of a 16-bit number, allowing the DAC to act on 16-bit data without any conversion or shifting. (with some minor loss in precision provided by low-order bits)

7. DAC_DHR8R1
8. I want to know more about how to handle aliasing, why it's bad, and how it happens.