Analog 2.0 **documentation**

Vol. 7

# Making an envelope generator generator


**Version: 2.1**

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# 1. About this document

**This document is an envelope jet for the analog synthesizer system Analog2.0.**

**I will explain how to make a neller module.**

**This document should be produced by the user with reference to the following documents.**

**It is written on the premise of.**

**--Analog2.0 Starter Kit**

**--vol.4 Manufacture of noise generator and mixer**

**--vol.5 Production of VCA**

**--vol.6 VCO production**

**Change log**

| Version date | | Changes |
|---|---|---|
| 2.0 2.0 | 2009/11/19 | Analog2.0 Document version 2.0<br>--Reviewed the circuit design.<br>--Revised the document accordingly. |
| 2.1 2.1 | 2009/12/14 | -Fig . 2-7 Corrected an error in the wiring diagram.<br>Inv output and Non-Inv output are reversed. |

## 2. **Envelope generator module-Generator module production** 2.1.

**Production flow The module production flow is the same every time as follows.** -Obtaining **parts** - **Manufacturing the board-Installing the parts on** the board - **Installing the panel parts-** Checking **the wiring of the board-Checking** the **operation**

### 2.2. **Outline of the module to be manufactured** 2.2.1. **Functions**

**In this article, we will build an Envelope Generator (EG) module.**
**As shown in Figure 2-1 by EG, the gate signal is input and the envelope information called ADSR is input. Output.**

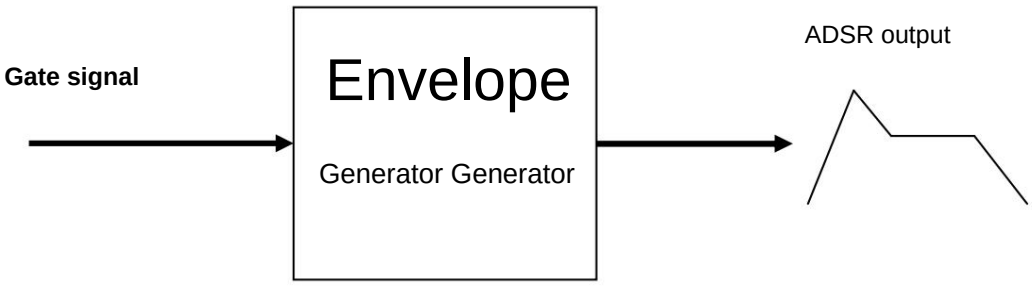



**Figure 2-1 Conceptual diagram of envelope generator generator**

**Figure 2-2 illustrates the relationship between the EG's inputs and outputs. First, in the initial state with no gate input, the output is also zero. When the gate signal rises, the EG starts operating. First, the output rises from zero to the maximum. This rise time is set by Attack Time (A). Attenuation begins when the output reaches its maximum. This speed is set by Decay Time (D). As long as there is a gate input, it will settle to the level set by Sustain Level (S) after attenuation.**
**increase. And when the gate is turned off, it attenuates towards zero. This speed is set by Release Time (R). In this way, the EG generates a time-varying CV pattern that changes the sound of the synthesizer.**

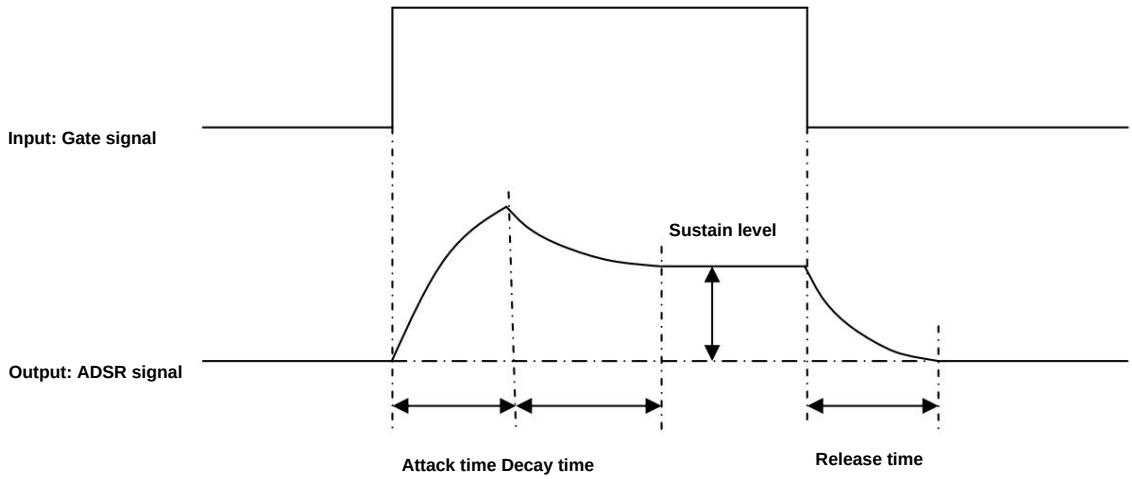



**Figure** 2-2 **Inputs and outputs of the envelope generator**

### 2.2.2. **Positioning in the system**

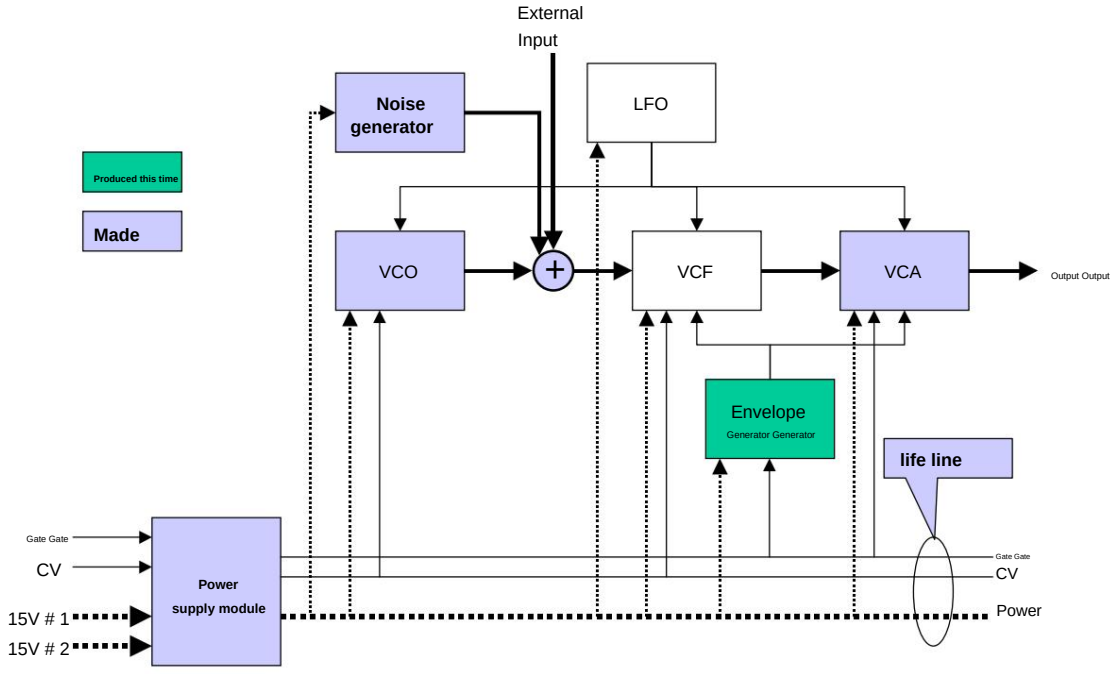



**Figure 2-3 shows the position of the EG in the configuration of the Analog 2.0 production system. EG is It is the main control module of Analog2.0 and changes the operation of sound processing modules such as VCF and VCA.**

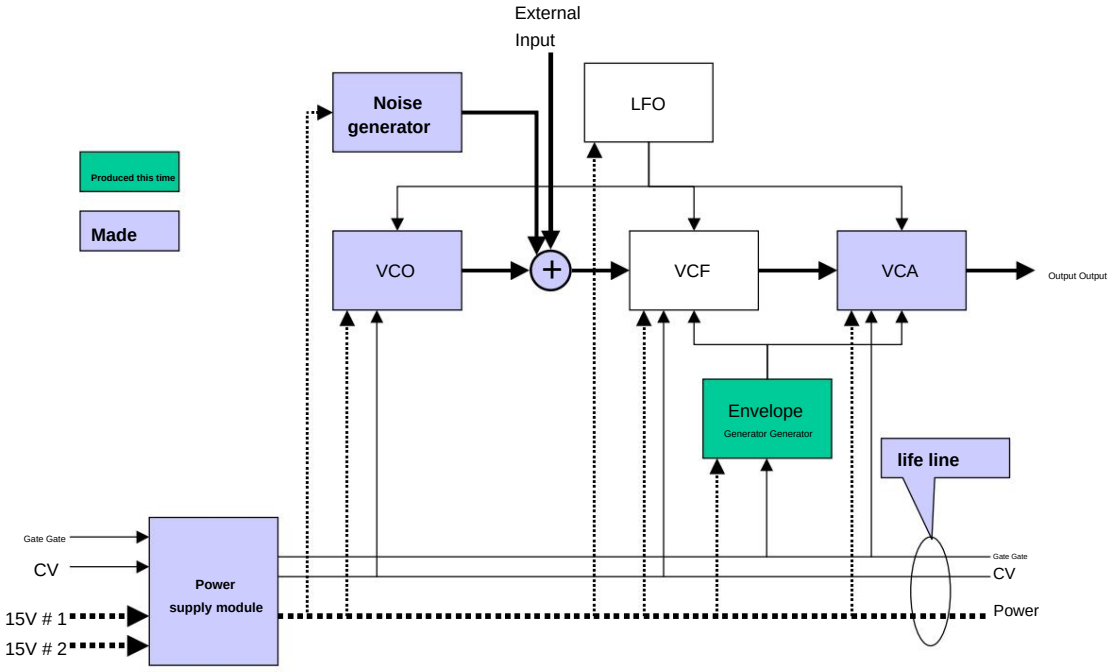



**Figure 2-3 Positioning of EG**

**Within the panel, the EG is positioned as shown in Figure 2-4.**

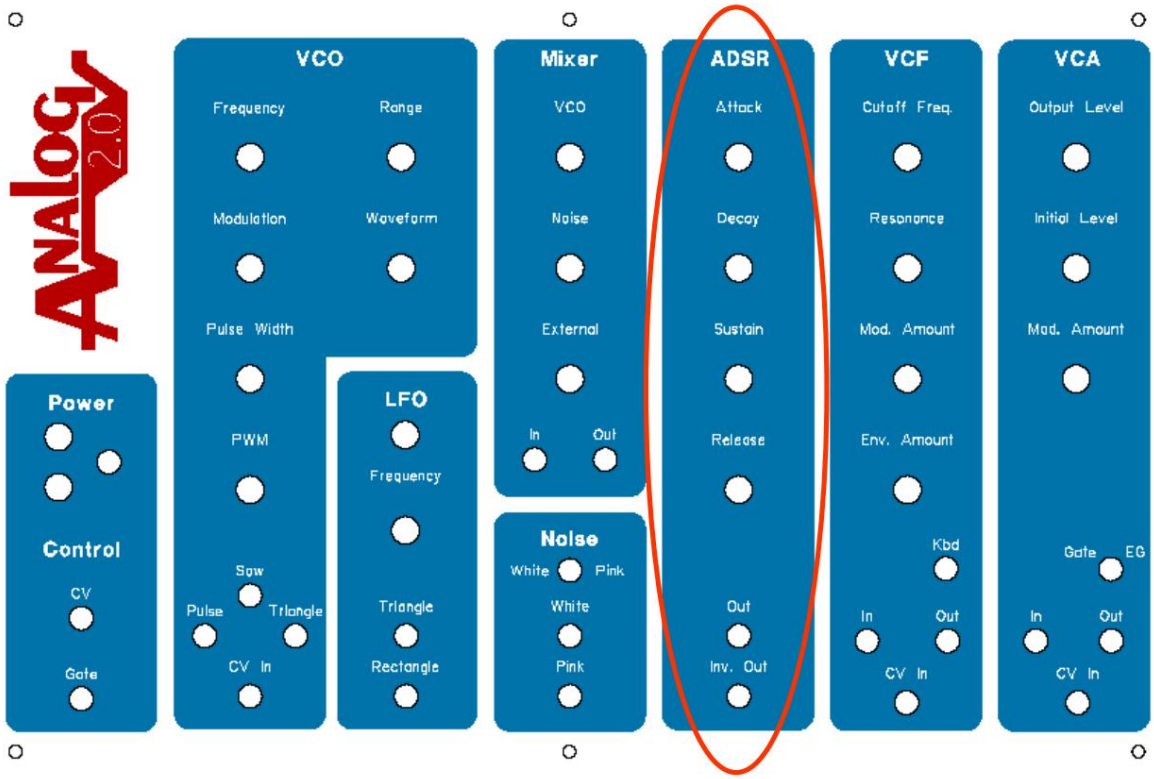


**Figure 2-4 Positioning in the panel**

### 2.2.3. **Specifications**

**The specifications of the EG are as follows.**

-Input **gate level: off 0V on 5V**

-Output **signal level: 0 to 8V (non-inverting output) 0 to –8V**

**(inverting output)-Parameters : Attack Time / Decay Time / Sustain Level / Release Time**

## 2.2.4. **Circuit**

**The circuit diagram of the EG to be manufactured is shown in Figure 2-5.**

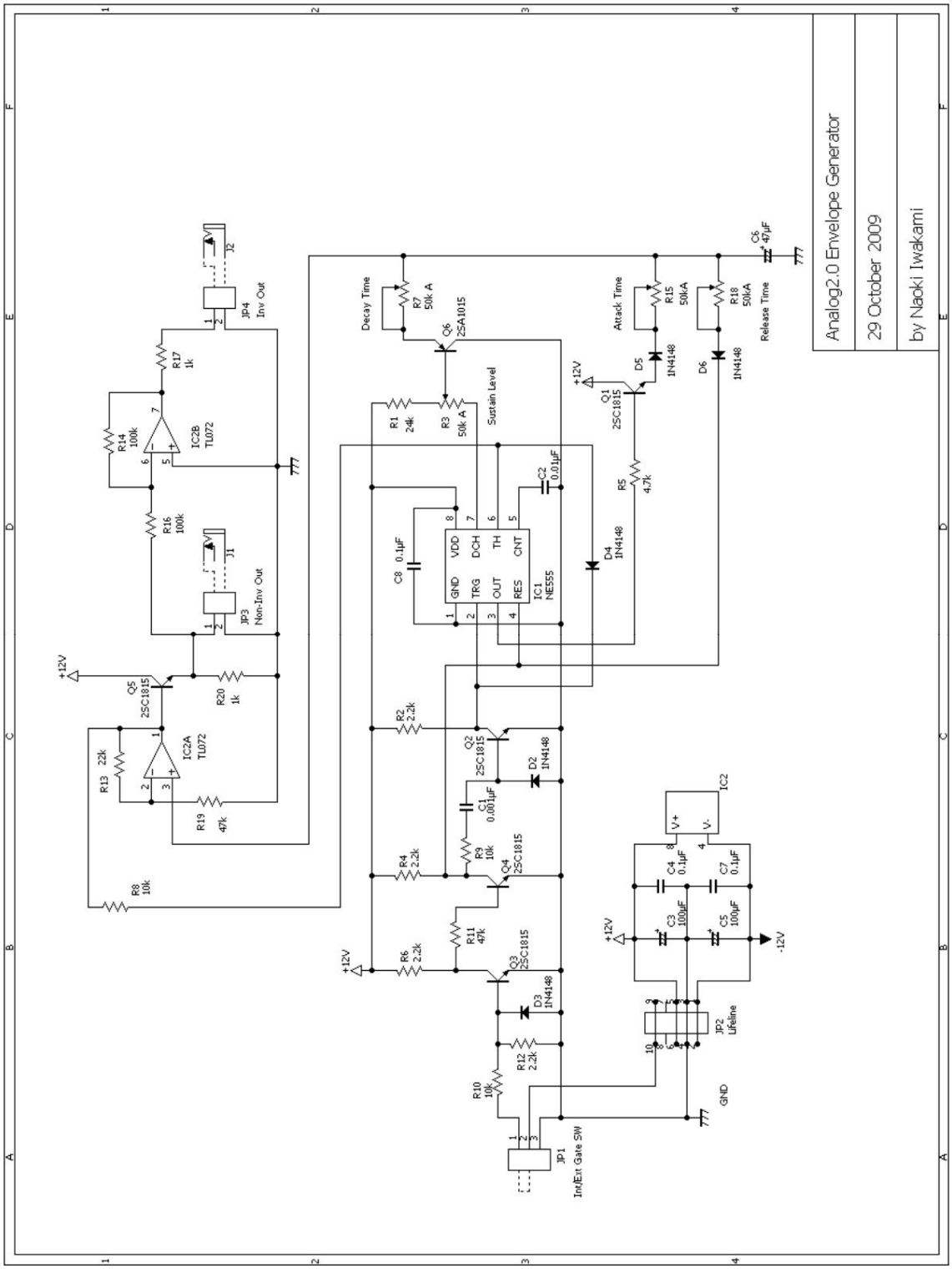



**Figure 2-5** EG **module circuit diagram**

## 2.3. **Obtaining parts**

**Well then, it's finally time to start production. The parts required for production are as follows. For production So, get these parts first.**

**Note: Diode numbers are missing D1 and start with D2. There is up to D6, but it is a must All you need is five.**

**Table 2-1: Parts required for EG production (inside the board)**

| parts number | Device name | Value / model number | Remarks |
|---|---|---|---|
| C1 | Multilayer Ceramic Capacitor | 0.001ÿF | Ceramic Capacitor is also acceptable |
| C2 | Multilayer Ceramic Capacitor | 0.01ÿF | Ceramic Capacitor is also acceptable |
| C3 | Electrolytic Capacitor | 100 ÿF | |
| C4 | Multilayer Ceramic Capacitor | 0.1ÿF | Ceramic Capacitor is also acceptable |
| C5 | electrolytic capacitor | 100 ÿF | |
| C6 | electrolytic capacitor | 47ÿF | |
| C7 | Multilayer Ceramic Capacitor | 0.1ÿF | Ceramic Capacitor is also acceptable |
| C8 | Multilayer Ceramic Capacitor | 0.1ÿF | Ceramic Capacitor is also acceptable |
| D2 | diode | 1N4148 | |
| D3 | diode | 1N4148 | |
| D4 | diode | 1N4148 | |
| D5 | diode | 1N4148 | |
| D6 | diode | 1N4148 | |
| IC1 | timer IC | NE555 | |
| IC2 | operational amplifier | TL072 | |
| JP1 | pin header 2.5mm pitch 1x3 | | Int / Ext Gate SW |
| JP2 | pin header 2.5mm pitch 2x5 | | Lifeline |
| JP3 | pin header 2.5mm pitch 1x2 | | Non-Inv Out |
| JP4 | pin header 2.5mm pitch 1x2 | | Inv Out |
| Q1 | transistor | 2SC1815 | |
| Q2 | transistor | 2SC1815 | |
| Q3 | transistor | 2SC1815 | |
| Q4 | transistor | 2SC1815 | |
| Q5 | transistor | 2SC1815 | |

| | | | |
|---|---|---|---|
| Q6 transistor | | 2SA1015 | |
| R1 carbon resistance | | 24kÿ | 1 / 4W 5% |
| R2 carbon resistance | | 2.2kÿ | 1 / 4W 5% |
| R3 variable resistor | | 50kÿ A | |
| R4 carbon resistance | | 2.2kÿ | 1 / 4W 5% |
| R5 carbon resistance | | 4.7kÿ | 1 / 4W 5% |
| R6 carbon resistance | | 2.2kÿ | 1 / 4W 5% |
| R7 variable resistor | | 50kÿ A | |
| R8 carbon resistance | | 10kÿ | 1 / 4W 5% |
| R9 carbon resistance | | 10kÿ | 1 / 4W 5% |
| R10 carbon resistance | | 10kÿ | 1 / 4W 5% |
| R11 carbon resistance | | 47kÿ | 1 / 4W 5% |
| R12 carbon resistance | | 2.2kÿ | 1 / 4W 5% |
| R13 carbon resistance | | 22kÿ | 1 / 4W 5% |
| R14 carbon resistance | | 100kÿ | 1 / 4W 5% |
| R15 variable resistor | | 50kÿ A | |
| R16 carbon resistance | | 100kÿ | 1 / 4W 5% |
| R17 carbon resistance | | 1kÿ | 1 / 4W 5% |
| R18 variable resistor | | 50kÿ A | |
| R19 carbon resistance | | 47kÿ | 1 / 4W 5% |
| R20 carbon resistance | | 1kÿ | 1 / 4W 5% |

**Table 2-2: Parts required for EG production (outside the board)**

| | | | |
|---|---|---|---|
| J1 | 3.5mm pin jack | | Non-Inv Out |
| J2 | 3.5mm pin jack | | Inv Out |

## 2.4. **Attaching parts to the board**

**Figure 2-6 is the wiring diagram of the printed circuit board to be manufactured this time. Pads not connected to this board**

**Are arranged in large numbers. This is a universal board. Use it when modifying the circuit**

**Please.**

**Note 1: This board has one jumper wire, but it is printed on silk screen.**

**plug. Remember to install the jumper wire as shown in Figure 2-6.**

**Note 2: The resistance next to R11 (opposite R6) is R1. It may not be visible because it overlaps with the letters of D6**

**I can't.**

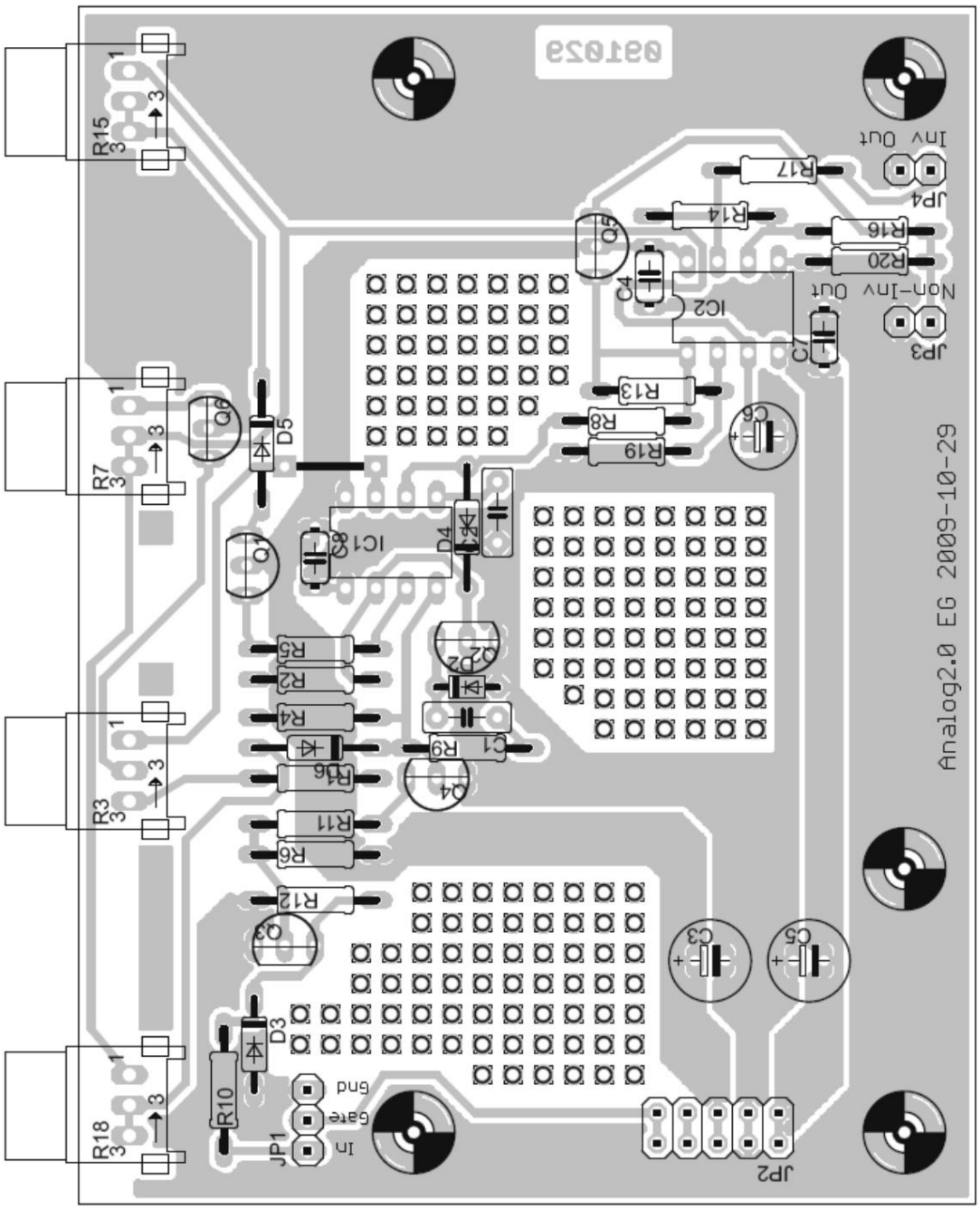
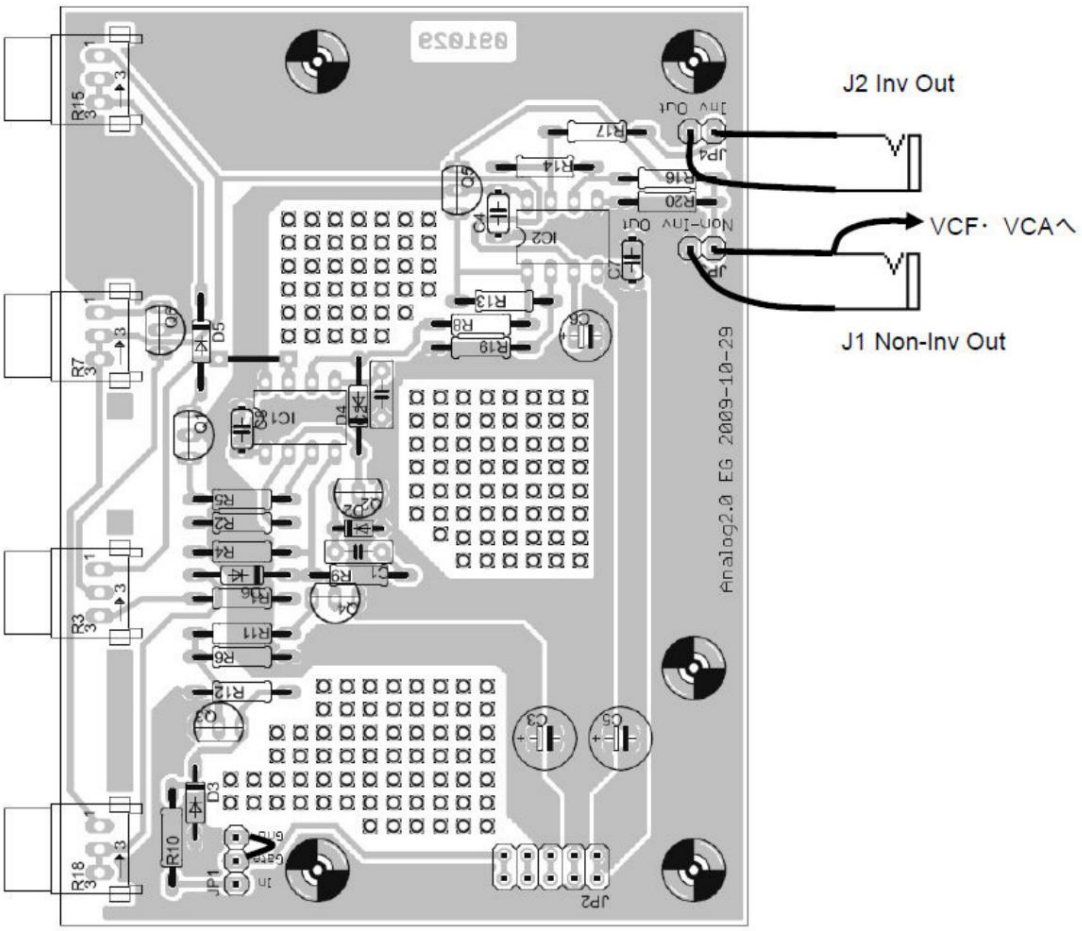


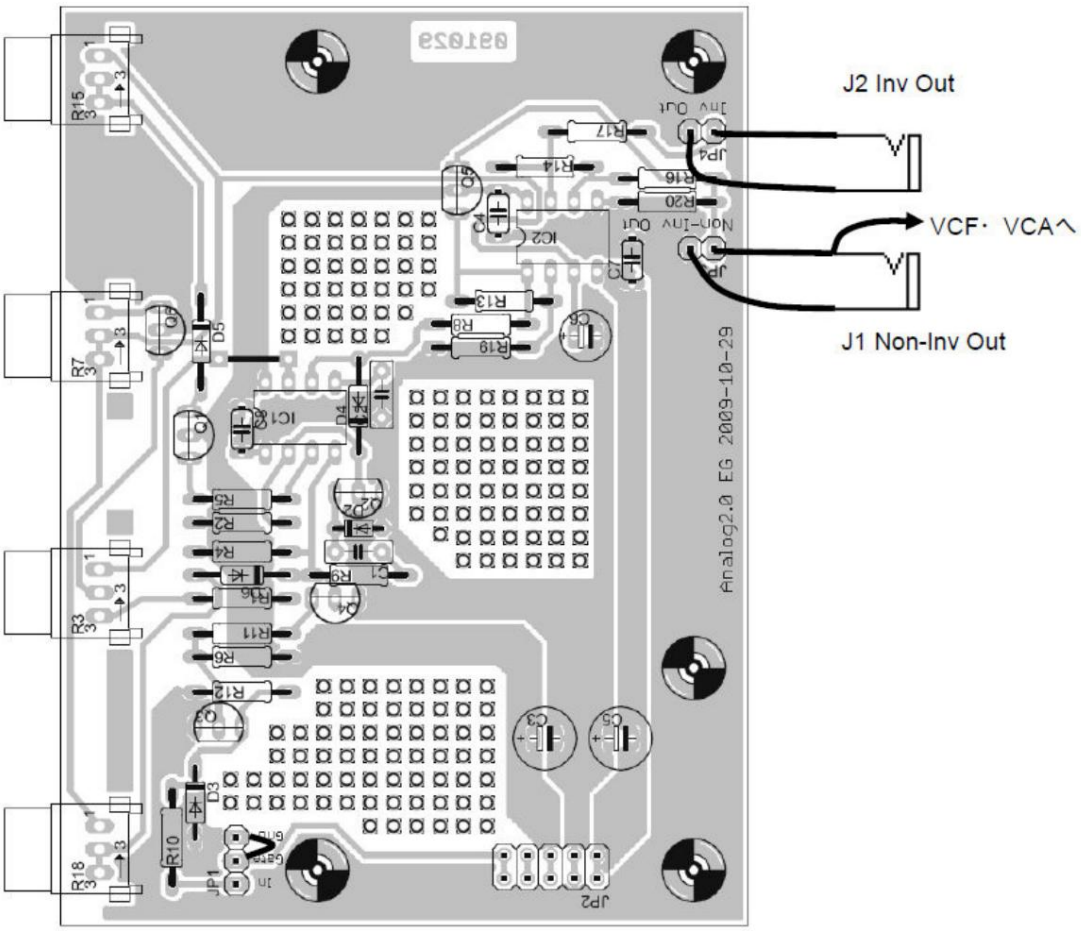

**Figure 2-6 Wiring diagram of EG board**

## 2.5. **Installation of panel parts**

**After installing the board parts, wire the parts to be attached to the panel (parts outside the board).**




**Connect the pin header and the mini jack with lead wires as shown in Figure 2-7. The non-inverting output goes out to the jack and then extends to connect to the EG In endpoint of each of the VCF and VCA modules. The VCF module is not yet complete, so just prepare the connector and leave it unconnected.**
**JP1 jumpers that are used in PC parts can be used. (Fig. 2-8)**




**In the actual wiring diagram shown in Fig. 2-7, the lead wires are routed large to make the connection easier to see, but in the actual wiring, try to make the lead wires as compact as possible. The photo in Figure 2-9 is an example of mounting the board on a panel. Figure 2-10 shows the implementation on the panel from the front side. As you can see from the photo, the board is fixed by tightening the volume shaft with nuts.**

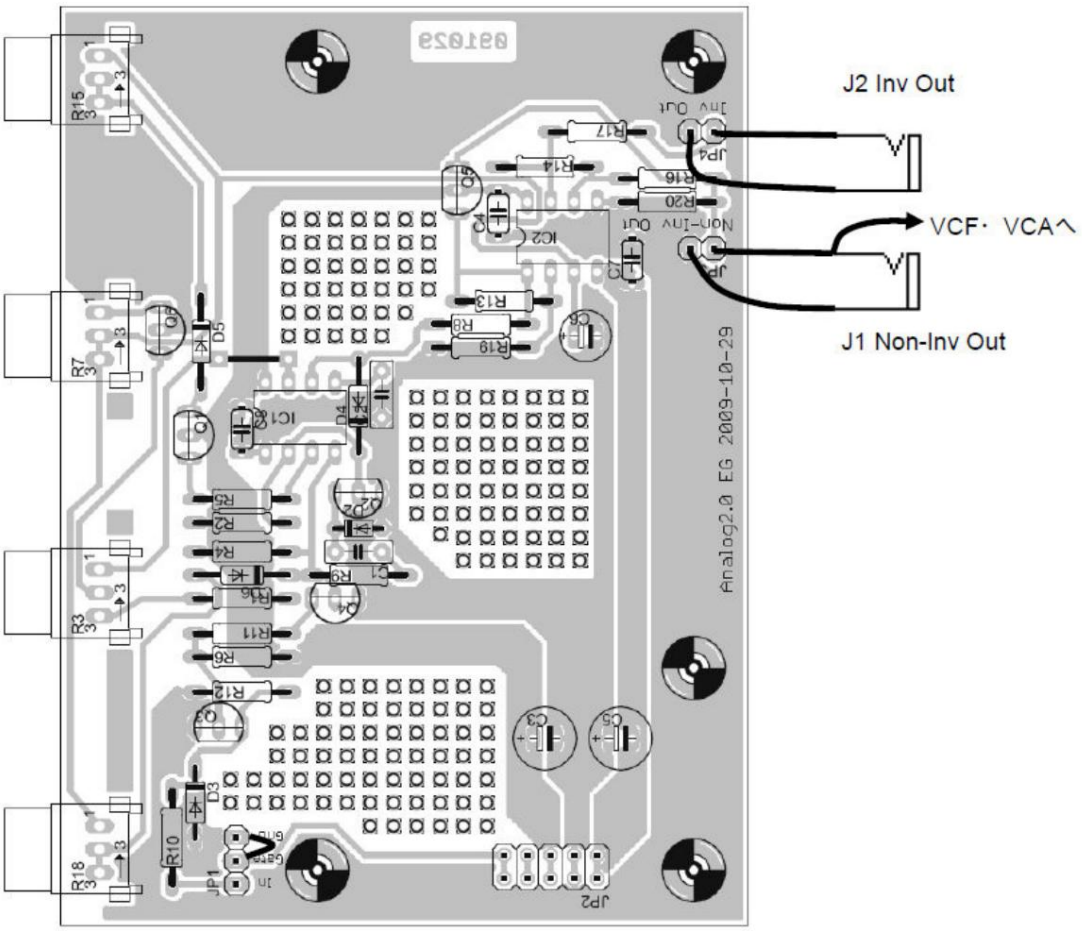



**Figure 2-7 Wiring of panel parts**

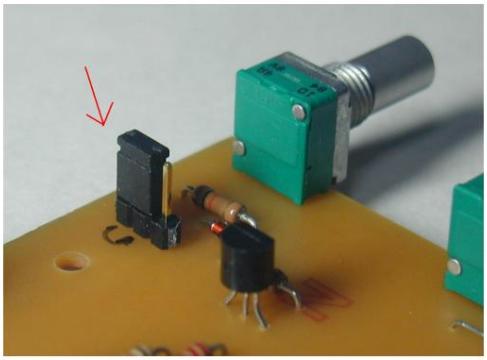


**Figure 2-8 How to install the jumper**

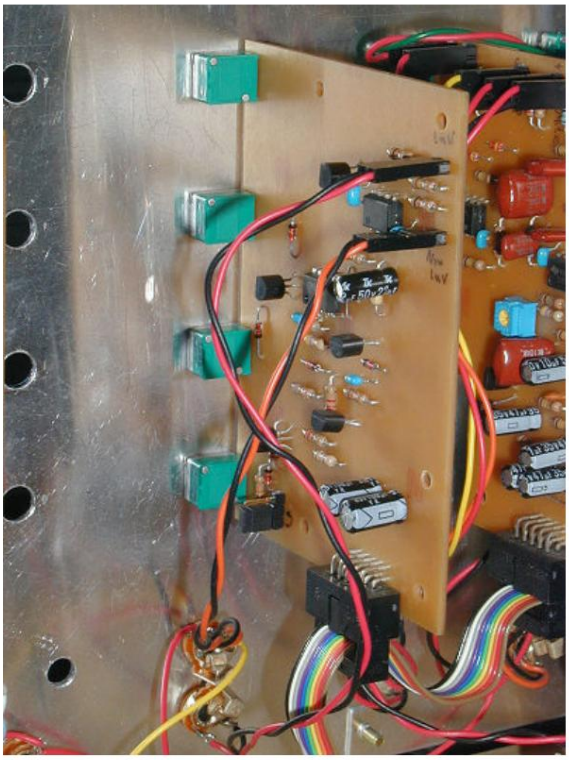


Figure 2-9 Mounting example on the panel (back side)


Figure 2-10 Implementation example on the panel (front side)

2.6. **Checking the wiring on the board**

**At this point, the assembly of the EG module is complete. As always, be sure to check the wiring before turning on the power. In the unlikely event that there is a wiring error, not only will it not operate normally, but in some cases the parts will be damaged. Check the checklist below to see if the wiring is correct.**

**[] Is the resistor installed in the correct place and with the correct value? [] Is the capacitor installed in the correct place, with the correct type and with the correct value? [] Is the electrolytic capacitor installed in the correct orientation? [] Is the diode installed in the correct place and in the correct orientation? [] Is the transistor installed in the correct place and in the correct orientation?**

**[] Is the IC installed in the correct location and in the correct orientation?**

**[] Is the jack pin header installed in the correct place? [] Turn the board over**

**and check the soldering points. The adjacent copper foil pattern is Han**

**Is there a solder bridge that is short-circuited in the da?**

**[] Is there any place where the soldering is immo soldering? If the body of the part is shaken and the lead at the soldering point moves, it is almost certainly immo solder. The potato solder will peel off over time, so if you find it, re-solder it.**

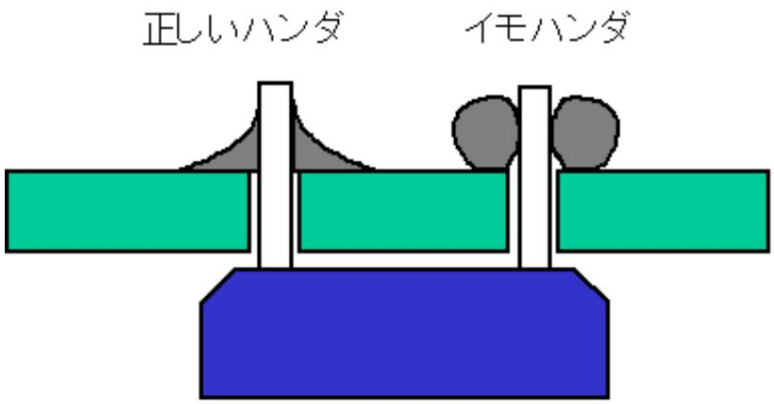



**Figure 2-11 Correct solder and immo solder**

2.7. **Operation check**

**Now, let's check the operation. Since there are no adjustment points this time, we will only check the operation. Movement**

**Please prepare the following to confirm the work.**

--MINI **Board or a device that generates a gate signal**

-Analog **tester**

**This time, I will use an analog tester. Digital testers are not suitable. Anna**

**If you do not have a log tester, check the operation based on the sound from the VCA.**

**To hear the sound from the VCA, increase the noise volume of the mixer and connect the VCA output to the amplifier.**

**Follow the procedure below to check the operation.**

**1. Connect the MInI Board to Analog2.0 2. Turn**

**on the power 3. Set the knobs as follows ÿ A:**

**Minimum, D: Minimum, S: Maximum, R: Minimum 4. Tester for EG output Hit. The range**

**of the tester should be larger than 12V.**

**5. Press any key on the MInI Board to generate a gate. Along with this, the output of EG is 8V**
**Make sure it goes up to a certain degree.**

**6. Move S to the midpoint and regenerate the gate. Make sure that the output of EG goes up to about 4V**
**Admit.**

**7. While increasing the value of A, generate a gate several times. Confirm that the rise of EG gradually slows**
**down. At the rising edge, when the output of the EG reaches the maximum, 4V rapidly**
**Depressed to a degree.**

**8. Set the value of A appropriately and raise the value of D to generate gates several times. Standing**
**The speed at which the value drops from the maximum value to the value of S after rising gradually slows down.**
**Confirm.**

**9. Turn the gate on and off several times while increasing the value of R. Exit from gate OFF**
**Confirm that the damping of the force slows down to the beginning.**

**After confirming normal operation, the production of the envelope generator is completed. This is finally**
**You can now create and play sounds with CV / Gate.**