Analysis of CMOS based NAND Gate on 28 nm technology

Aditya Agarwal, BITS Pilani, K K Birla Goa Campus

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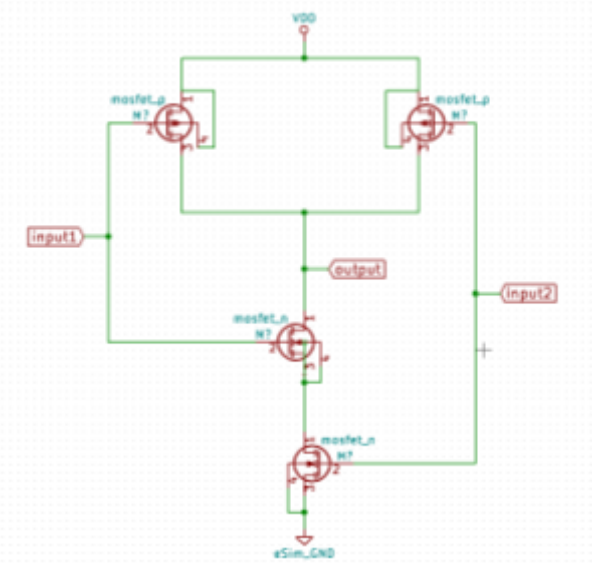
Abstract

In this paper, I am going to design a CMOS based NAND gate using 28 nm technology. I will be using synopsis software to implement and analyze the circuit. NAND Gate is an universal gate and is an important part of electronic circuits. This complete design and implementation is done using VLSI technology which has features such as high speed, low cost, small size and low power.

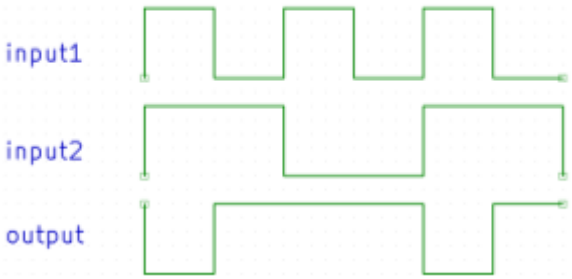
Reference Circuit



Reference Circuit Details

A NAND gate is a logic gate which produces an output which is false only if all its inputs are true. Here we have implemented a NAND gate which has 2 inputs and 1 output. NAND gate using CMOS will be designed using 2 PMOS and 2 NMOS devices. The 2 PMOS will be connected in parallel with each other and in series with the 2 NMOS. Inputs will be between the NMOS and PMOS pairs, and the output will be between the PMOS and NMOS connection. In the circuit waveform, we will verify this implementation using clock pulse.

Reference Circuit Waveforms



References

[1] Balraj Singh, Mukesh Kumar, J. S. Ubhi. Analysis of CMOS based NAND and NOR Gates at 45 nm.

[2] Kapil Mangla, Prof. (Dr.) Anil Kumar. Study and Analysis of NOT and NAND gate using various low power techniques.