A fast sub-nanosecond time-resolved autocorrelator

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1 Introduction

1.1 Motivation and objective

The motivation behind this project was inspired by a problem encountered in certain ion trap experiments, where PMT (photomultiplier tube) is used to collect light from ion illuminated by laser light. As the photons from ions enter the PMT, laser light also scatters into the PMT, mixing with the real signal (the photons from ions). Specifically, the system we are working with has mode-locked (ML) laser pulses coming into the trap at a certain rep. rate, 80MHz, with a 10 picosecond pulse width, as represented in Figure 1. During the time when a ML pulse is present, the PMT signal will have a high spike for 10 picosecond due to the photons from laser coming into the PMT. Afterwards this 10ps time interval the signal is an exponential decay, at which point only the photons from the ions are going into the PMT. This pattern repeats at the rep. rate of the laser, which is every 12.5ns.

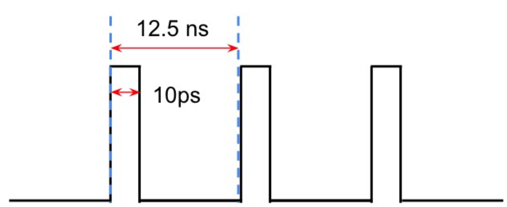

Figure 1: The repetition rate of mode-locked laser pulses is 80MHz and 10ps pulse duration.

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Therefore, our **objective** for this project is to be able to create a narrow (sub-nanosecond wide) "window" as shown in Figure 2, scan it in time through across the PMT signal using autocorrelation to take out the noise spikes in the signal.

1.2 Possible approaches

Before we settled on this solution of performing autocorrelation as proposed in our "objective", we have searched for other possible methods to achieve the same result.

There are generally two routes we may take to tackle this problem. One method is to time tag the photon arrivals, and one is to create some kind of gate. Since it is known to us that at the first 10ps of every 12.5ns, the signal during that time contains high level of noise from ML laser, and if now we know the arrival time of the photons, we may select out and statistically subtract the photons arriving during that time interval. This method utilizes time-interval measurements, and from doing literature research, we found there has been a lot of well-studied event-stamping techniques to reach picosecond-, and even sub-picosecond-, time resolution for time stamping events. For example, one

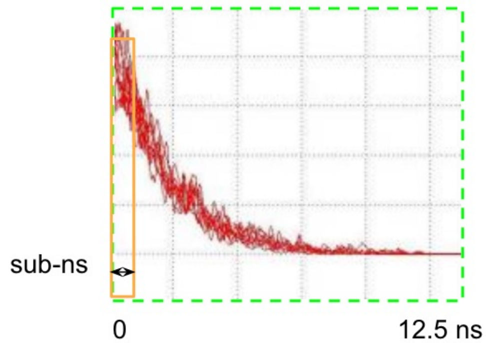

Figure 2: Looking at a12.5ns time frame of the PMT signal, where for 10ps duration there is a high spike in the signal due to the ml laser light. The rest of the signal is normal ion lifetime decay.

could use very small (μm size)-CMOS-based TDC (time-digital converters) to get down to 1 to 2 ps resolution with low power consumption. One could also add in more oscillators to further sub-divide the clock cycle in a TDC to improve the resolution. However, TDC has very low data storage capacity and data retrieval rate, making it highly unsuitable for our experiment of interest.

Another more straightforward approach is to gate the PMT input every fast, in a sense, this is like a shutter for camera. Gating the input means we will be blocking out the photos hitting on the photocathode for some duration of time, and unblock the gate. But photocathode has a relatively long (compared to the how fast our electronics has to be) dead time, so it takes a while for the photocathode to recover and responds to the next photon.

With these issues in mind, we came to the another gating scheme where we look at the output of the PMT instead of the input. This led to our objective where we perform electronics logics to filter out the noise in the signal by having a auto-correlator that scans the signal in time.

2 Proposal

2.1 Proposed design

The idea of our proposed design (Figure 3) is to take a 80MHz square wave TTL signal, split it and introduce a phase delay between the two split signals. These two signals with a time delay are fed to to XOR or AND gate, and th output will be a more narrowly spaced square wave signal. This signal with higher frequency, together with the PMT's TTL signal are then fed through and AND gate.

When implementing the circuit, with such strict requirement on time resolution, we need to be very careful with the timing of each component in the circuit, rise/fall time of the component, and impedance matching of the traces.

2.2 Parts Needed

Item	Unit Price	Quantity	Total
HMC721LC3C (a 14 Gbps XOR gate), Mouser	\$150	1	\$150
HMC726LC3C (a 14 Gbps AND/NAND gate), Mouser	\$150	2	\$300

Table 1: Parts needed for the proposed design and budget.

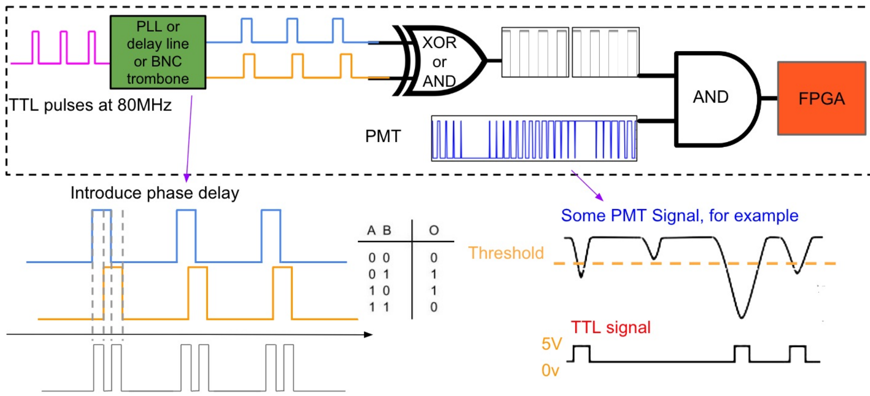

Figure 3: Overall scheme of our proposed design, where 80MHz TTL square wave signal is split and phase delayed. The resulting signal from the first the XOR (or AND) gate is pulse sequence with narrower width, which is put through an AND gate with the PMT signal.

2.3 Planned Timeline

- Week 3: Build and test the circuit, basically, have a prototype of a slow version to make sure logic works. Purchase parts.
- Week 4: Improve on the prototype to push for as fast as possible. Calculate the timing, rise/fall times, impedance matching for the fast design. Run some simulations of convolution of two functions.
- Week 5: Improve on the design based on prototype. Start and finish implementing the actual design with fast electronics.
- Week 6: Testing, debugging and improving.
- Week 7-8: Finialize the product. Test out with ion trap system and obtain actual results.
- Week 9 Catching up on anything incomplete. Writing up report and working on final.

2.4 Evaluation Metrics

1. Prototype(s) of slower version and output data. (20%)
2. Design (including calculations of timing, impedance matching of traces, and simulation of expected logic function outputs) of fast electronics. (60%)
3. Completion and implementation of actual workable produce. Test results from using the fast autocorrelator on the real experiment. (20%)