

Construction of a nanosecond gating circuit for PMT noise elimination

Kayla Rodriguez, and Scarlett Seejia Yu
University of California Los Angeles, Los Angeles, CA 90024, USA

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1 Introduction

In this report, we detail and present our electronic project progress and outcomes, from literature research results, to our first prototypes, to making improvements and designing a printed circuit board, and to soldering and testing the circuit.

1.1 Background motivation

The motivation of this project arises from a problem encountered in certain ion trap experiments, in which a PMT (photomultiplier tube) is used to collect ions fluorescence induced by laser light. As the photons from ions enter the PMT, laser light also scatters into the PMT, mixing with the ion's fluorescence signal. Specifically, the system we are working with has mode-locked (ML) laser pulses coming into the trap at the repetition rate of 80MHz, with around 10 picosecond temporal pulse width (visualized in Figure 1).

During the time when a ML pulse is present, the PMT signal will consequently have a high spike for 10ps duration due to laser photons scattering into the detector. After this time interval the signal decays exponentially as only photons emitted from ions are entering the PMT. This pattern repeats at the 80MHz rep. rate of the ML laser, which is every 12.5ns.

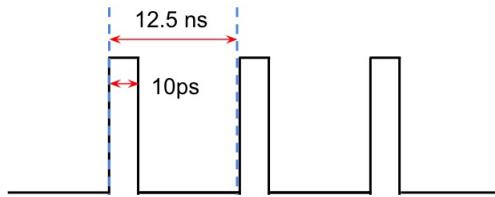


Figure 1: The repetition rate of mode-locked laser pulses is 80MHz and 10ps pulse duration.

Objective: Given the above system and issue, the objective of our electronic project is to design a solution to filter out the ML laser scattering noise in the PMT signals to obtain a clear fluorescence signal that is coming just from the ions.

1.2 Literature research and proposal

An immediate solution appeared to be just making a very fast shutter to block the PMT during presence of the ML laser, however, a picosecond shutter is highly non-trivial. Even with such fast electronics gating the input means we will be blocking out the photos hitting on the photocathode for some duration of time, but

photocathode has nanosecond-scale dead time, so it takes a while for it to recover and respond to the next photon.

Some literature research on other possible approaches suggests that there are generally two routes to tackle: One approach involves essentially event-stamping the arrival time of each photon, and other approach is to perform some gating.

Since it is known to us that the signal during the first 10ps of every 12.5ns interval contains noise from the ML lase, if we time tag the photon arrival time, we can statistically subtract out the photons arriving in that time frame. This kind of time-interval measurement can reach picosecond, or even sub-picosecond resolution. To implement, for example, one could use very small μ m-CMOS-based TDC (Time-Digital Converters) to get down to 1ps resolution with low power consumption. One could also add in more oscillators to further sub-divide the clock cycle in a TDC to improve the resolution. However, TDC has low data storage capacity and data retrieval rate, making it highly unfeasible for our experiment of interest.

Now as manipulating the PMT input (shutter method) and output (time-tagging of photons) both present significant hurdles, we turned to another scheme where we apply some gating before the final PMT output [1].

This led to our proposal where we use analog circuit with logic gates to filter out the noise in the signal. The principal is shown in Figure 2. The 80MHz mode-locked laser TTL (transistor-transistor logic) signal is split into two separate signals, with a phase delay created relative to each other. These two signals go into a XOR gate, which outputs a signal with pulses of narrower width. The purpose of this step is to create a square-wave signal at the same frequency of the laser signal but with sub-nanosecond temporal pulse width (We see later that XOR must be changed to an AND to for this). This output is then inverted, and along with the PMT TTL signal go into a AND gate.

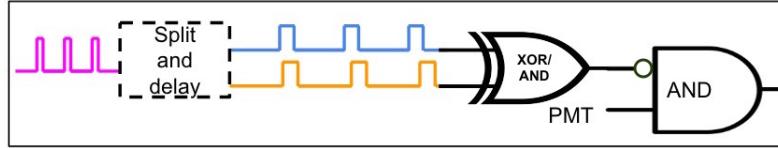


Figure 2: Initial proposed gating scheme

Figure 3 is a simulation on falstad of the our proposed design. Two identical square waves with where one phase delayed by 35° w.r.t. the other are inputted to XOR gate, which then go to the AND gate along with the PMT signals. Notice the XOR output has twice the frequency as desired,because this time delay happens on both the rising and falling edge.

2 Design versions

2.1 Overview

Over the course of the project, we first built and improved proof-of-concept prototypes to test out the scheme, and to better understand potential issues and limiting factors. With the breadboard prototypes working, we moved on to designing a faster and more modular printed circuit board (PCB) version.

2.2 Logic prototypes

The first step in implementation is to make and test a slow version of our proposed scheme with readily accessible parts in lab. We used the most straight-forward method to create the time delay, which is to have two BNC cables of different lengths.

The added time delay is verified to be linearly proportional to the added BNC cable length, as shown in Figure 4. The fitting also provides reference to quickly calculate the time delay for any length of BNC.

Using the longest and shortest cables in lab, a 125 ns time delay is created. Then, different XOR gates are tested with square wave as inputs and 300MHz oscilloscope, starting with the slowest XOR gate made

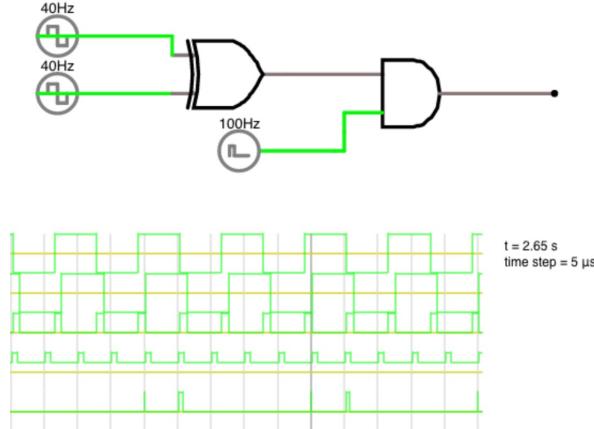


Figure 3: Circuit simulation. The top two waveforms are the phase-delayed inputs, and the third waveform is the XOR output. The fourth waveform is an arbitrary square wave to simulate the PMT signals, and the last is the output of the AND gate.

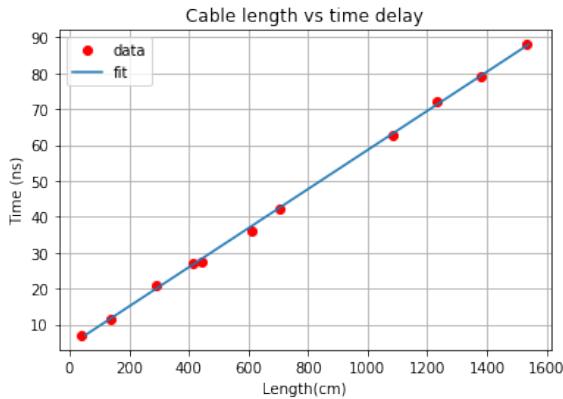


Figure 4: Linear relationship between added cable length and time delay between two signals.

from five NANDs, to XOR gates available in lab, and to the faster purchased XOR gate. Table below shows the propagation delays of the each type of the XOR chip used.

Type	Model	Propagation delay
NANDs in lab	SNX4LS00	9ns
XOR in lab	CD4070B	6.8ns
Purchased XOR	7AC11086	3.8ns

Note that only propagation delay t_{pd} is provided on all the datasheets; there is no reference to the rise/fall times.

The output results of each chip are as following:

1. The first XOR is made of five NANDs, which is too slow to resolve the time delay and the output is noisy, thus no reasonable output is obtained with this.
2. The XOR chip in lab is able to resolve nanoseconds of delay, as shown in Figure 5.

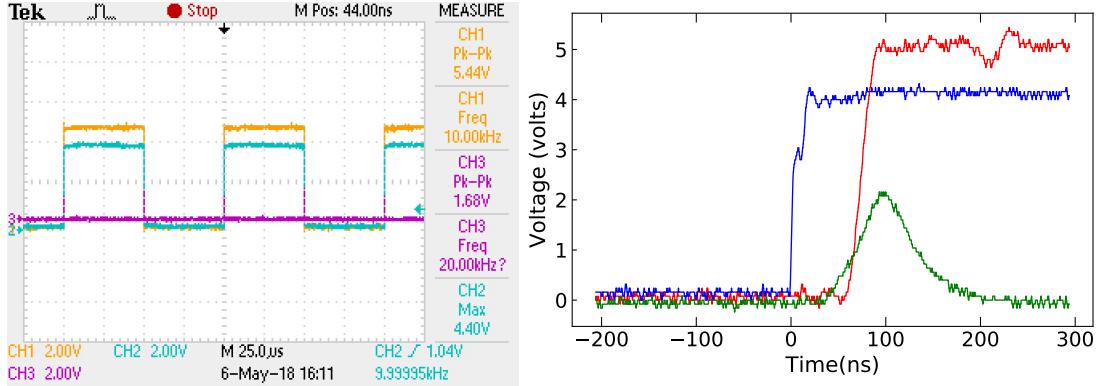


Figure 5: Lab XOR gate. (Left) The yellow and green are the inputs, and pink is the output of lab XOR. (Right) Zoomed-in plot of the signals showing the gate output with around 65ns width.

We can see that the logic works, yet the output is not exactly as desired because of the slow rise time, so instead of seeing a square pulse, we have a triangular pulse.

- With a faster XOR chip, we can see in Figure 6 that the rise time is much faster than before. By changing the attenuation on the scope probe from x1 to x10, we get much cleaner square-wave output as desired. The only trade-off is the attenuated voltage amplitude, which is not essential at this stage.

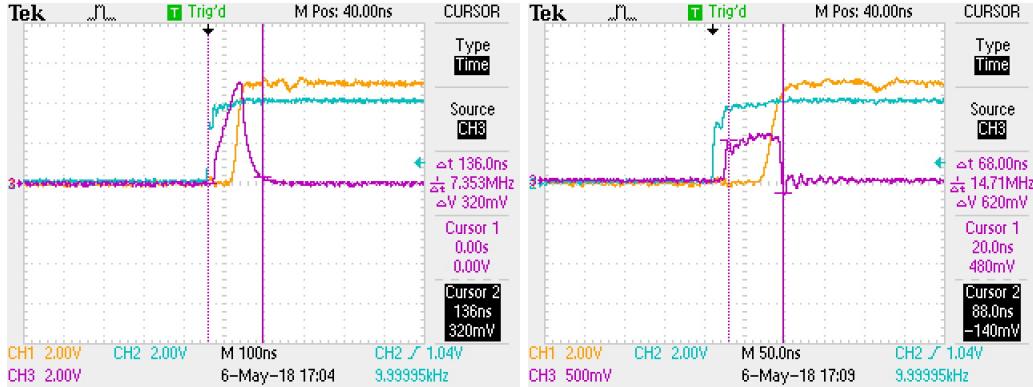


Figure 6: Fast XOR gate. (Left) The pink peak is the XOR output with x1 attenuation on the scope probe. (Right) The pink pulse is the XOR output with x10 attenuation.

The final step is to take the inverted output of the XOR gate obtained above and the PMT TTL signal together to an AND gate. The Rigol DG1022 Waveform Generator is used to simulate the PMT noise signal, and NOT chip is used to invert the XOR output. The resulting AND output is shown in Figure 7, where the region with inverted XOR output pulse sees a deletion of signal. This means that during the nanosecond window created from XOR, no PMT signal is let through the AND gate, effectively "gating" out that part of the PMT signal.

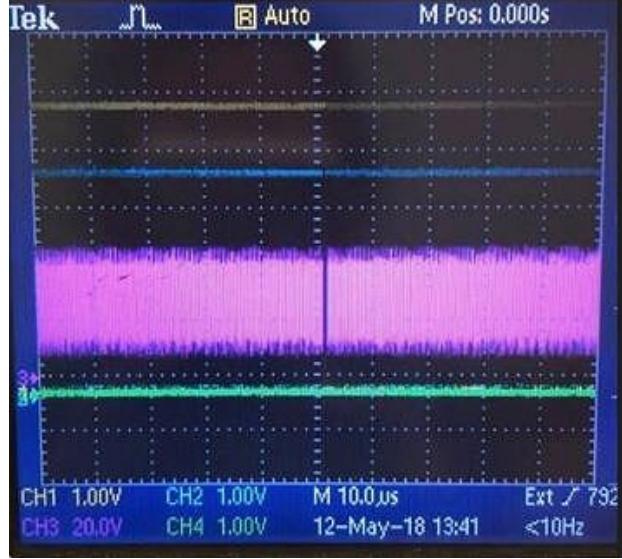


Figure 7: Final output of the AND gate, the blue and yellow are the two inputs for XOR, green is the simulated PMT noise, and pink is the AND output.

2.3 Main problems and fixes

Several noticeable main problems encountered during the prototyping process are:

1. XOR output has double the frequency of the inputs, as XOR gate triggers on both the rising and falling edges of the time-delay window. It is important for this output to have the same as frequency as the input 80MHz laser signals to ensure we filter out the right photons in the PMT.

The solution is to change the XOR to a Schmitt-trigger AND gate and invert the AND gate inputs. This is done by using the OnSemi NL7SZ58 malfunction gate.

2. The laser TTL signal is too low for the logic gate operation. According to the Spectral Physics Tsunami Manual [2], the 3955 control box's MONITOR connector only outputs a signal of only maximum 800mV and it goes below 0V, as shown in Figure 8.

The fix is to place a comparator after the laser TTL input, and with an adjustable voltage reference for the comparator using a potentiometer. This can be done for the PMT signal as well.

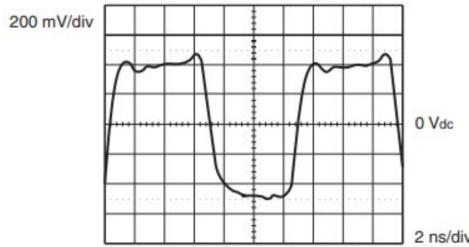


Figure 8: MONITOR signal for laser taken from the manual. [2]

3. Adding the comparators has its own issue. The comparator's datasheet [3] claims that it has a minimum input rating of -200mV (lower rail as GND), thus our laser TTL signal could break the comparator with the negative voltage. The fix is to include a voltage divider.

Lastly, instead of using BNC cables to create delay, a more modular and flexible alternative is to add RC delays in both of the inputs. By picking certain resistor and capacitor values, one can control the time delay between two signals.

2.4 Improved version with printed circuit board

Taking above issues and fixes into considerations, an improved design is made and shown in Figure 9.

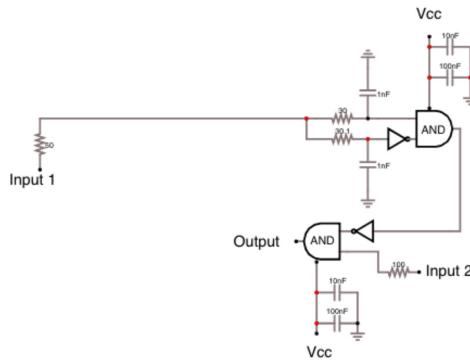


Figure 9: Improved circuit design

2.4.1 PCB designing

Next step is to take the circuit design and make a printed circuit board with it. The PCB designing is done on Eagle, and from researching on high-speed PCB design, some main design rules are followed, and other circuit improvements are made:

1. **Wire Lengths:** The part of the board with logic gate is placed very close together to ensure the short signal paths.
2. **Wire Shapes:** The wire paths are connected with either 45-degree wire connections or circular.
3. **Impedance Matching Resistors:** On the signal inputs, impedance matching resistors are placed.
4. **Buffer gates:** Used to clean up the signal to ensure a nice sharp TTL output.
5. **Decoupling capacitors:** Used to protect against power surges.

After several revisions, the final circuit scheme is shown in Figure 10, and the board design is shown in Figure 11.

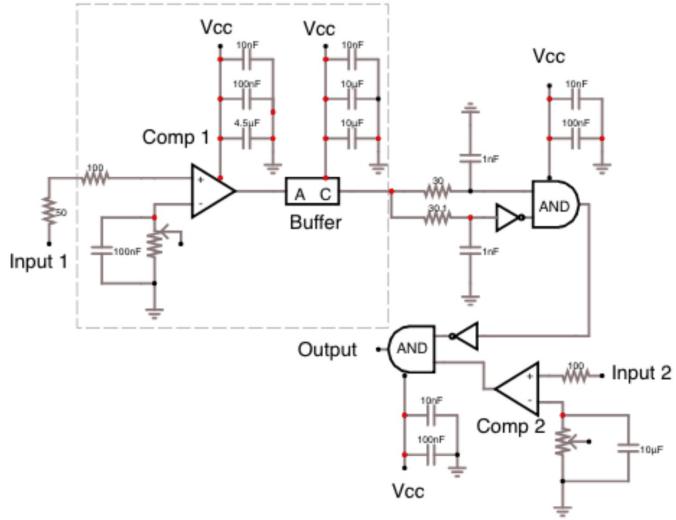


Figure 10: Final PCB design on Eagle

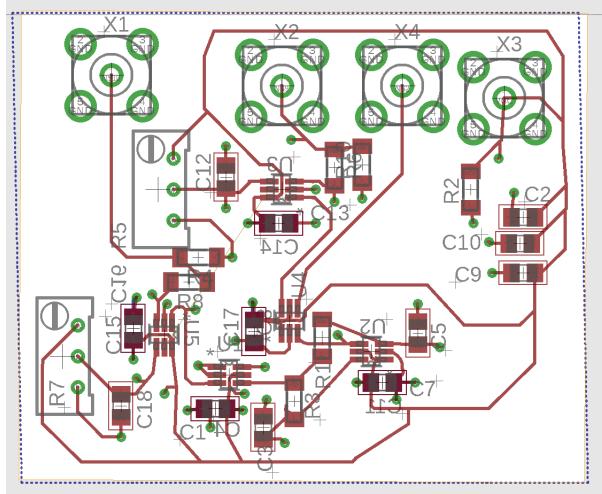


Figure 11: Final PCB design on Eagle

2.4.2 Assembling parts on PCB

The parts on the board mainly consist of various capacitors and resistors, potentiometer, SMA connectors, multifunction chips, comparators, and op-amps.

During soldering the solder temperature is kept around 350K, and each part is tested as it gets soldered:

1. **Powers:** All powers input are checked every time before anything else.
2. **Comparators:** Two comparators are in the circuit. To test them, a square wave signal of 200mV to 800mV is used.
3. **Buffer:** Once the comparators are working, then testing the buffer is easy, as the output should match the input.

4. RC delay: Only the difference between the two RC time constants matter, so by picking the same capacitor value, the time difference scales as the difference in resistor values. In our case, both capacitors are chosen as 1nF , and R_1 is $100\ \Omega$ and R_2 is $194.3\ \Omega$.

A mistake on the board design was realized (inverted a wrong input on the second AND gate) during the soldering, and this has been fixed by manually rerouting the connection with a thin wire.

The final soldered board is shown in Figure 12.

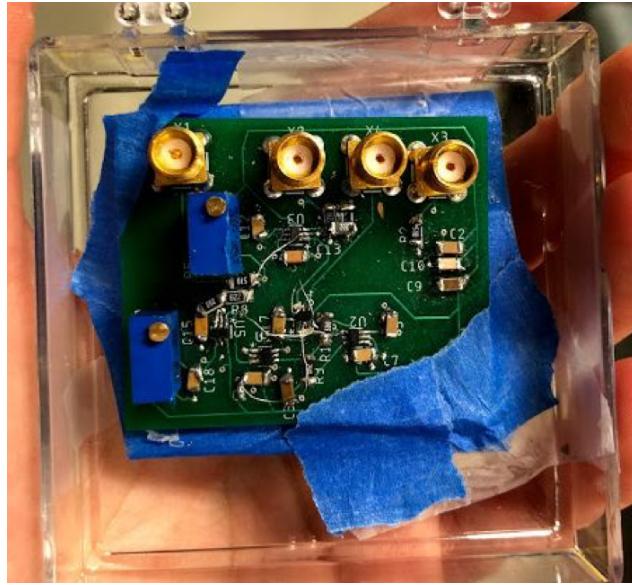


Figure 12: The soldered board, housed in a plastic box with drilled connector holes.

3 Test results

For testing the board on the experiment, the two inputs given are the laser and PMT TTL signals, as shown in Figure 13.

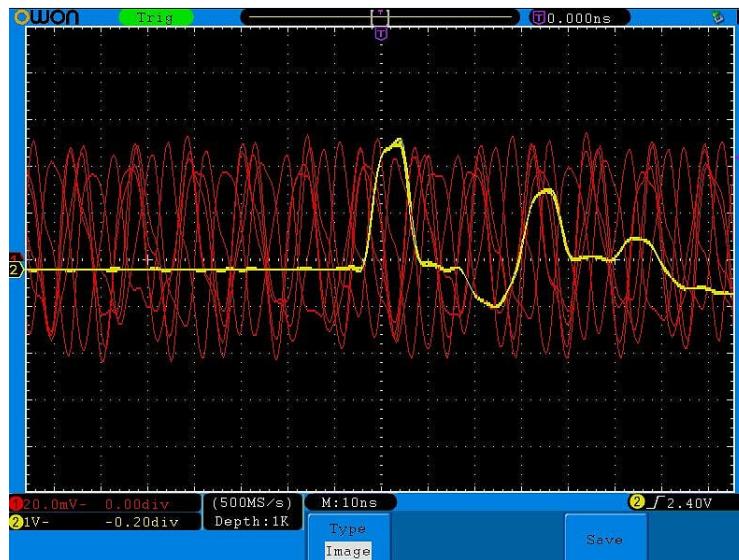


Figure 13: The red pulses are the laser TTL, and yellow is the individual PMT pulse

Notice that there is quite a bit of ringing on the PMT input signal, and this is eliminated by adjusting the potentiometer to raise the comparator reference value. The PMT signal is cleaned to be just peaks without any ringing, as shown in Figure 14.

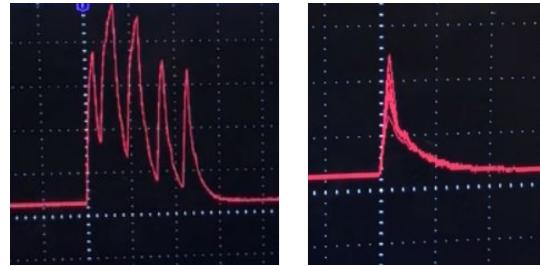


Figure 14: One the left is the input individual PMT peak with ringings, on the right is the output of the comparator with a clean PMT peak.

The output of the first AND gate is shown in Figure 15, where pulses of around 3.2ns width are created. As one can see, the there is still a some slow rising and falling (The Schmidt-trigger rising edge on the second AND gate should help). This nanosecond width is mostly limited by the chip, and with a faster AND chip, it is possible to get shorter time..

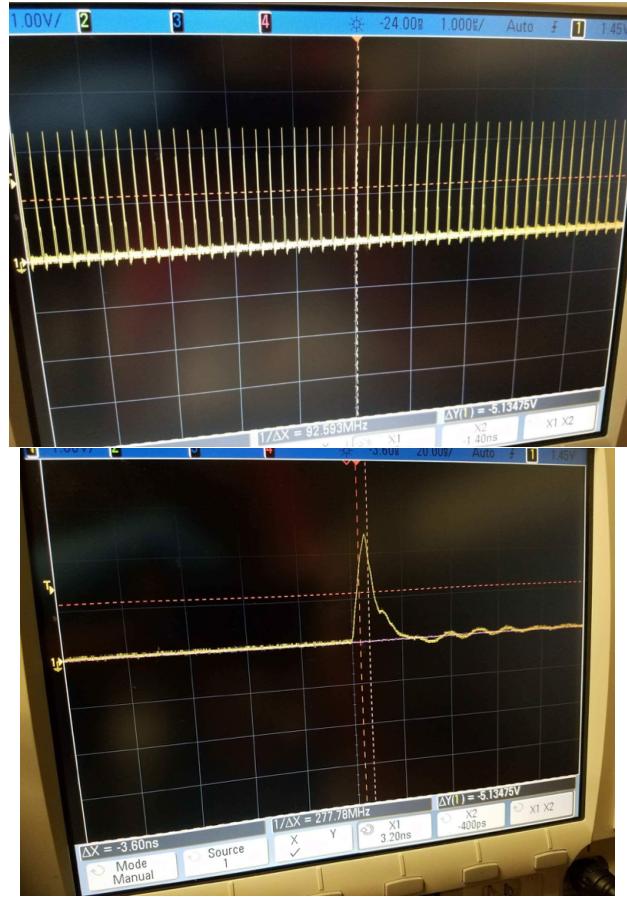


Figure 15: (Top) The output of the first AND gate. (Bottom) A closer look at the individual spike reveals a nanosecond pulse width.

After checking each of the the circuit with the input signals, the second AND gate output is read out

with a GHz scope. The result video was shown in our presentation, where one could see the PMT spikes. To really know whether our circuit is gating out the right photons, we would need the laser to be mode-locked to test out, which did not happen during the week of testing.

4 Remarks and summary

In short, we prototyped and implemented a nanosecond time-resolved gating circuit, which can be used for PMT noise elimination. The one thing we still would like to do is to test out the circuit with the mode-locked laser going, this can be done easily now (as of the time of writing), since the experiment seems to be back and running again. There is, of course, room for further improvements. Some immediate improvements are to try out different resistor values on the RC delays to create different delay values, get some faster AND chips, or looking for transistors that have much higher time-resolution.

4.1 Budget

Finalized Budget:			Proposed Budget:		
Items	Quantity	Price	Items	Quantity	Price
Printed Circuit Boards	4	176.00	fast XOR	2	300
AND gates	15	4.17			
SMA	8	39.04			
Comparators	12	50.28			
Grand total:		\$269.49			\$300.00

Table 1: Budget comparison table

4.2 Timeline

Our timeline changed quite a bit from our proposed one. We expected to finish the project around week 8, but when we decided to do a PCB, this extended the timeline. During the time we expected to be finished, we were testing the PCB and testing on the experimental setup.

	Planned	Actual
Week 3:	Build and test prototype	Made and the prototype with lab parts
Week 4:	Improve the Prototype	Tested out different prototype versions
Week 5:	Improve prototype and design fast circuit	Improved on prototype resolution.
Week 6:	Testing, debugging	Discussed and designed improved version of circuit.
Week 7:	Test in experiment	PCB designing
Week 8:	Test in experiment	Final PCB revisions, 6 drafts total, order board
Week 9:	Debugging	Soldering, testing the board
Week 10:	Debugging further	Testing in the experiment

Table 2: Comparison of the timelines.

4.3 Finalized evaluation metric

Prototype(s) of slower version and output data. (25%)

Circuit improvement and designing of the board. (35%)

Completion and implementation (printing and soldering) of actual workable board (25%). Test results from using the board with real experiment's inputs. (15%)

5 Acknowledgements and references

The authors like to gratefully acknowledge the help of the instructor - Christian Schneider, and the TA - Tony Ransford. In addition, thanks to Prof. David Saltzberg for providing BNC cables and SMA connections, and Peter Yu for lending us some soldering tools.

1. Tony Ransford
2. Spetral Physics Tsunami Manual
http://neurophysics.ucsd.edu/Manuals/Spectra-Physics/232A_Rev_D_Tsunami_User_Manual.pdf
3. Comparator <http://www.analog.com/media/en/technical-documentation/data-sheets/6752fc.pdf>
4. *Compilation of High-speed PCB Design Considerations*