PHYSICS 118, 2018

A sub-nanosecond time-resolved gating circuit

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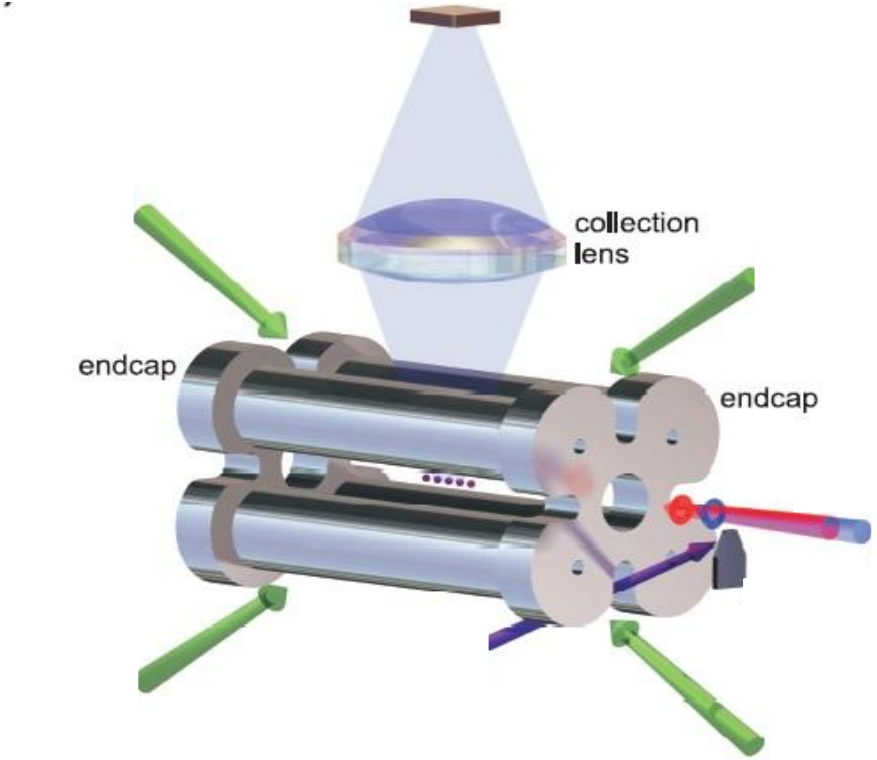
Department of Physics and Astronomy, UCLA

Dated: June 5th, 2018

Background story - system and objective



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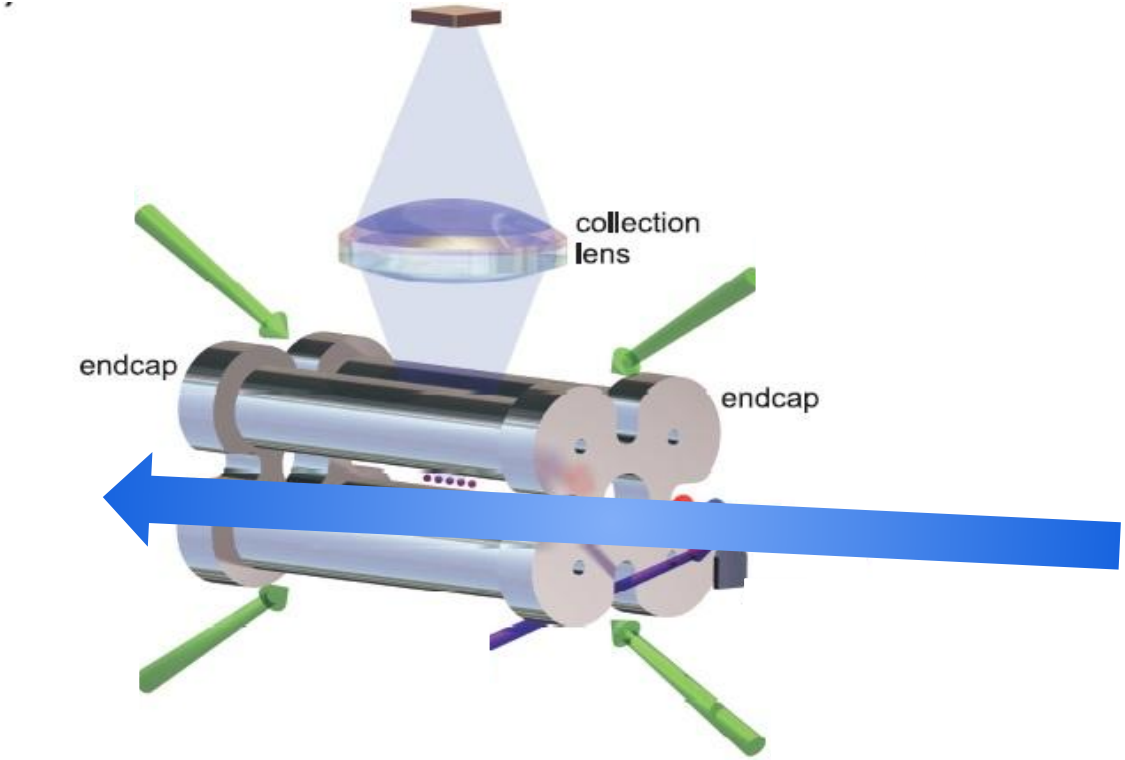

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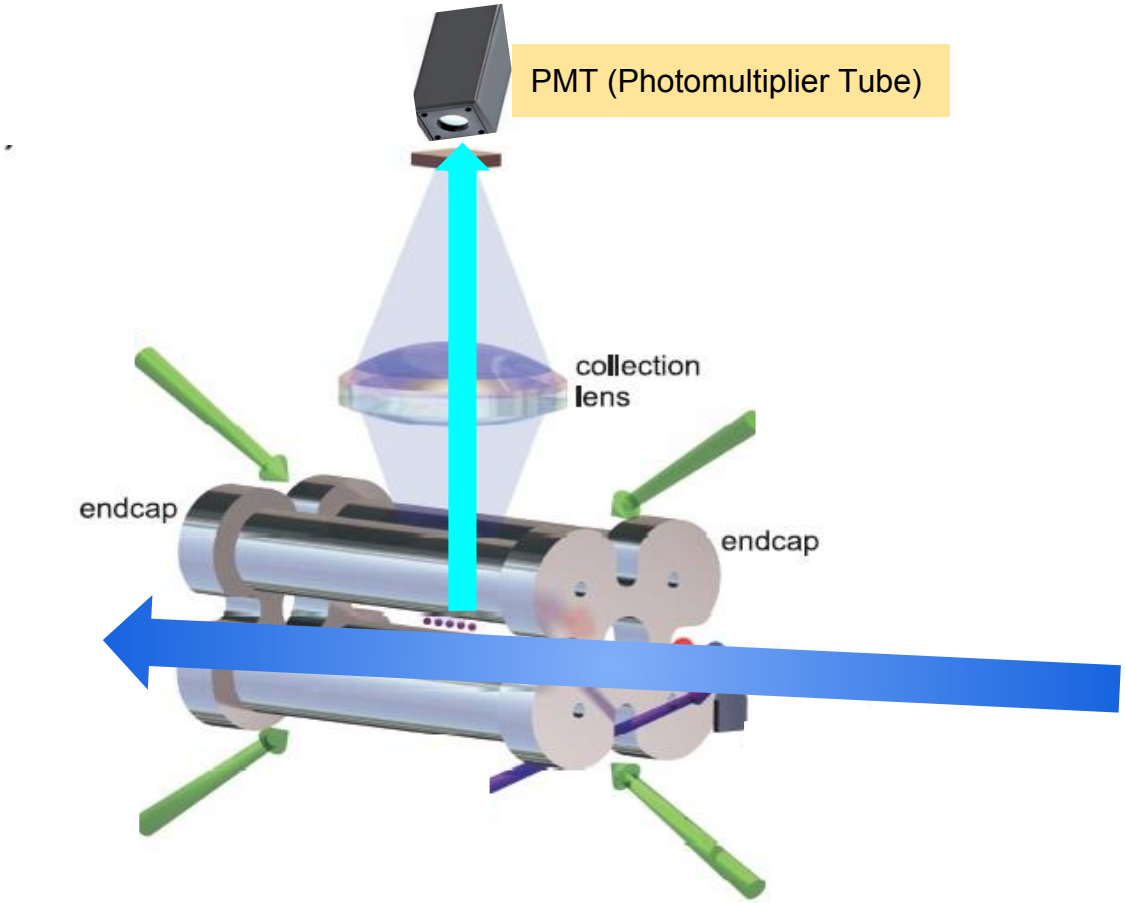

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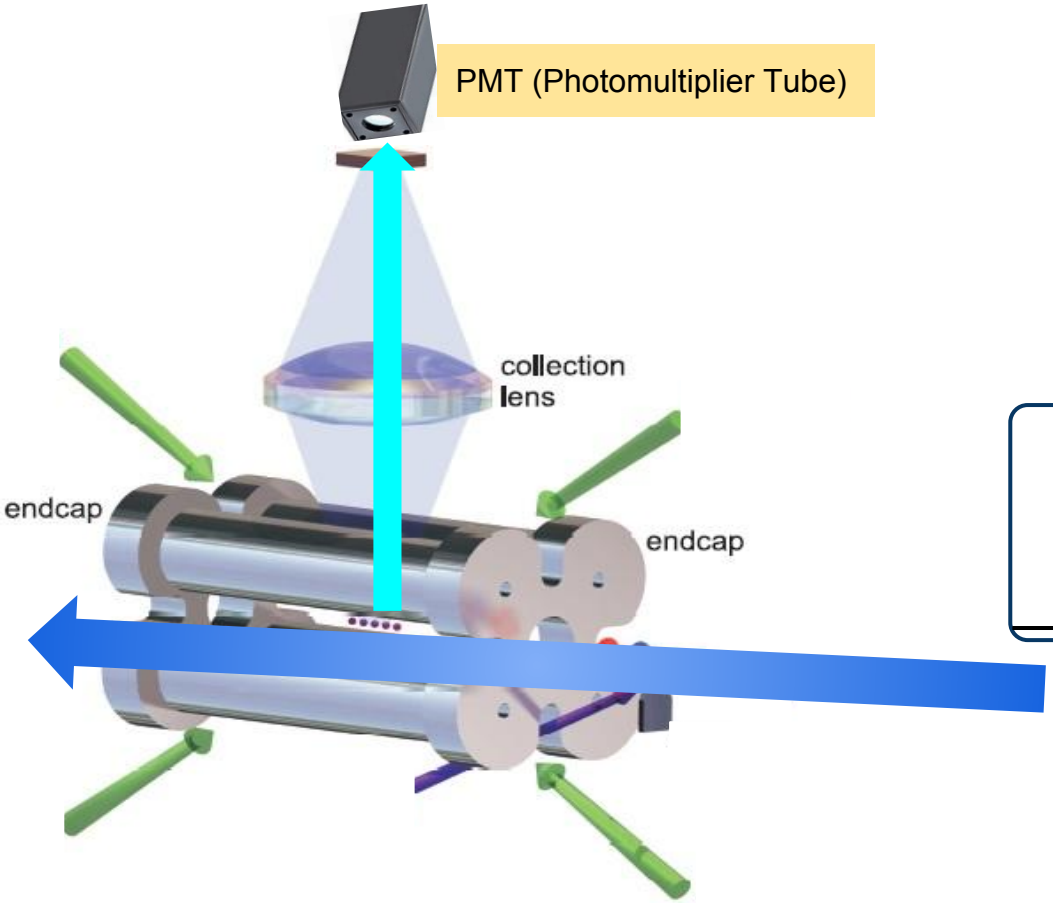

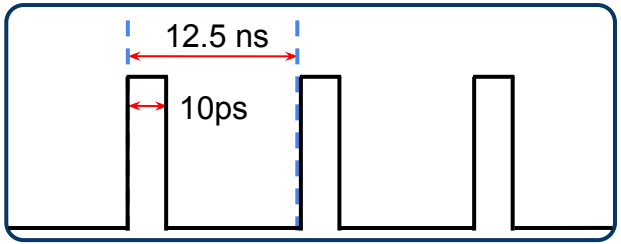

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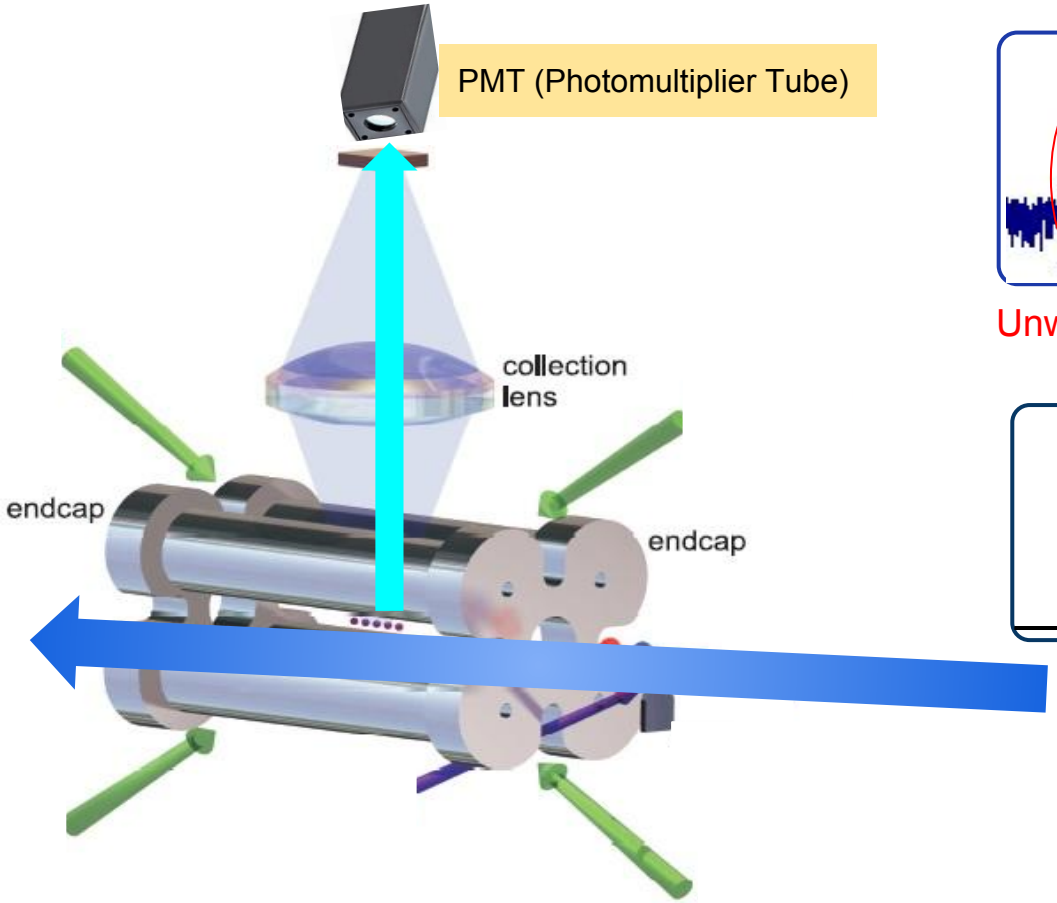
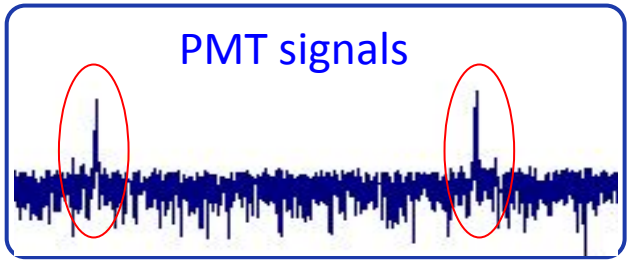
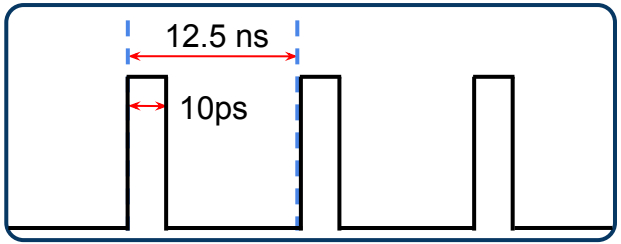




Unwanted spikes from laser pulses



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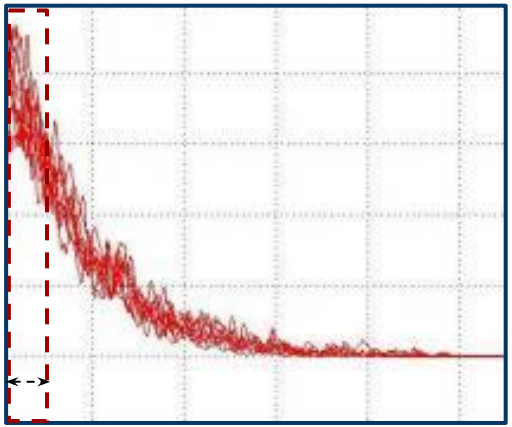
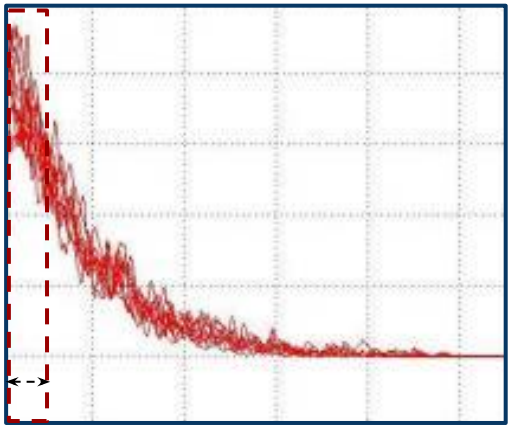


How to take out this pico-second signal?

Background story - system and objective



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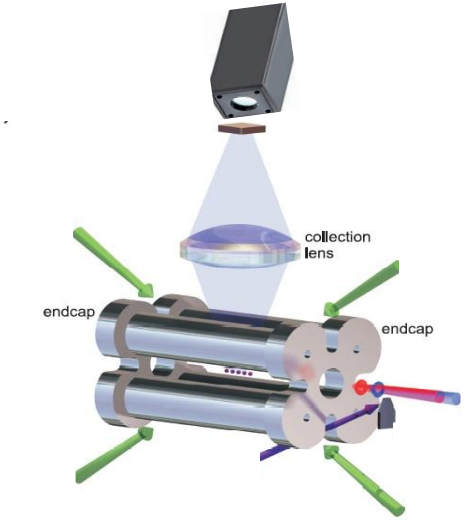

Picosec fast shutter?

Time tagging? $$$

Search for Possible Approaches (Week 2)

Two routes:

- Time tag the arrival time of each photon.
  - Eg. Use ***very*** small (um) CMOS-based TDC (time-digital converter)
  - Eg. Subdivide the clock cycle in a TDC. But **low data storage and retrieval rate.**
- Some sort of gate

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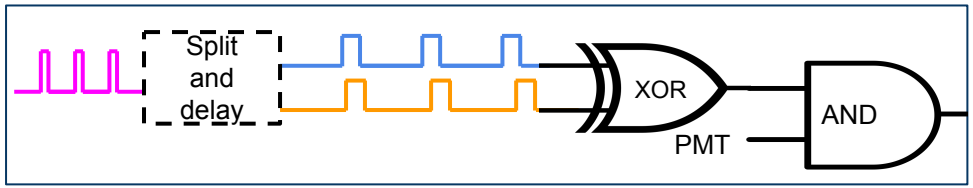
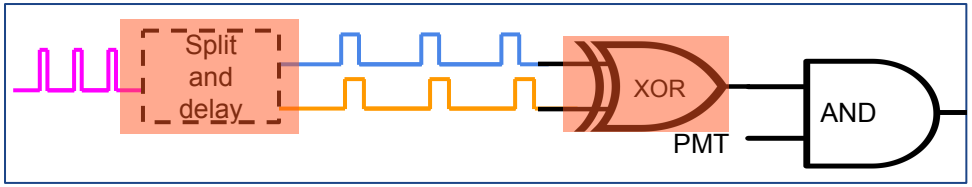
An analog solution:

Initial proposed logic

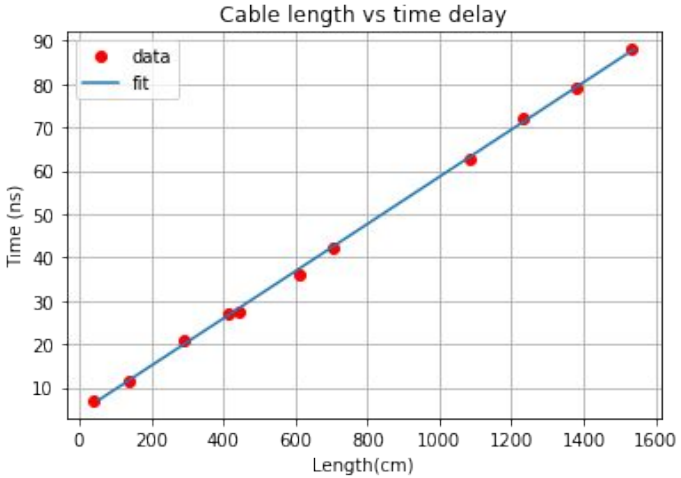


Starting out with lab parts (Week 3-4)



1. Delay: two BNC cables of different lengths
2. XOR gates: tried different types

Types	Model	T_{pd} (*ns*)
NANDS in lab	SNX4LS00	9
XORs in lab	CD4070B	6.8
Purchased XORs	7AC11086	3.8



Time delay created Δt ~ Difference in length ΔL

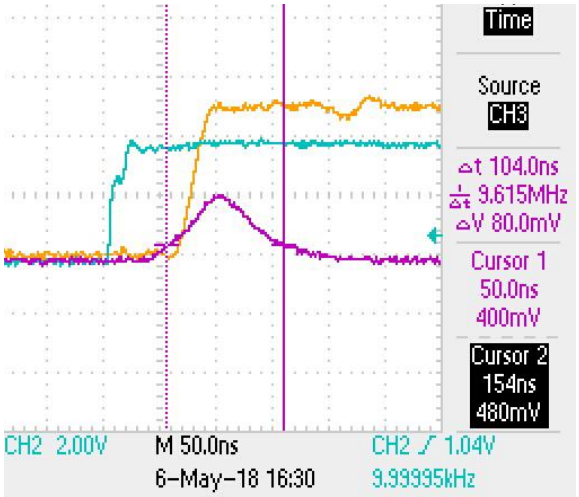
Beta versions - Result Summary (Week 3-4)

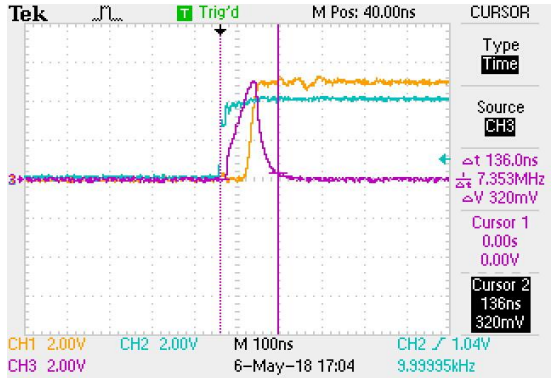
ver.	XOR type	Model	T_{pd} (*ns*)
0.9.1	NANDS in lab	SNX4LS00	9
0.9.2	XORs in lab	CD4070B	6.8
0.9.3	Purchased XORs	7AC11086	3.8

- Multiple stages, very slow.
- Output was noisy, unable to resolve the Δt delay

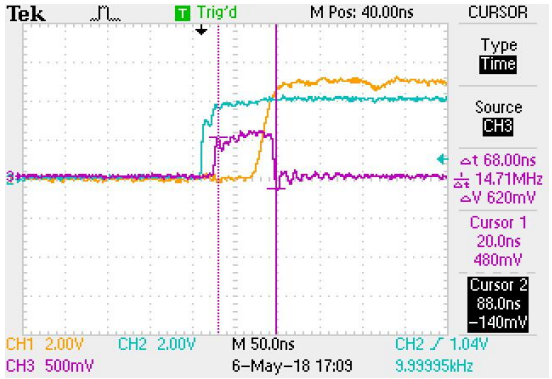
- Able to resolve hundreds of *ns*.
- Logic worked, but output not as desired.

- Clean sq-wave output with 68ns Δt, but attenuated amplitude.



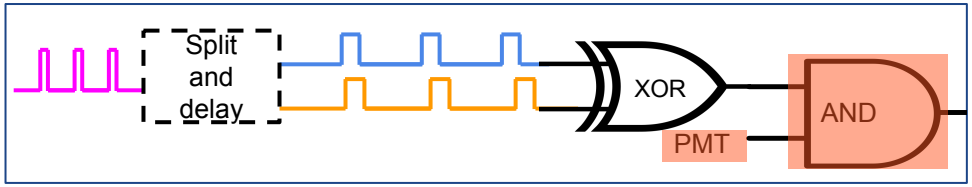


x1 attenuation



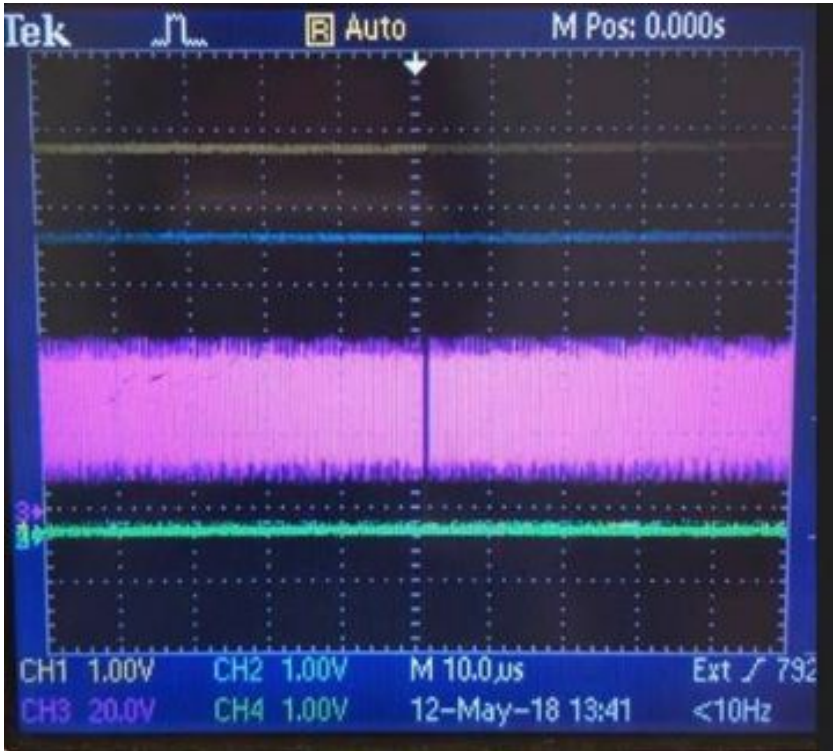
x10 attenuation

Beta versions - Final output (Week 5)



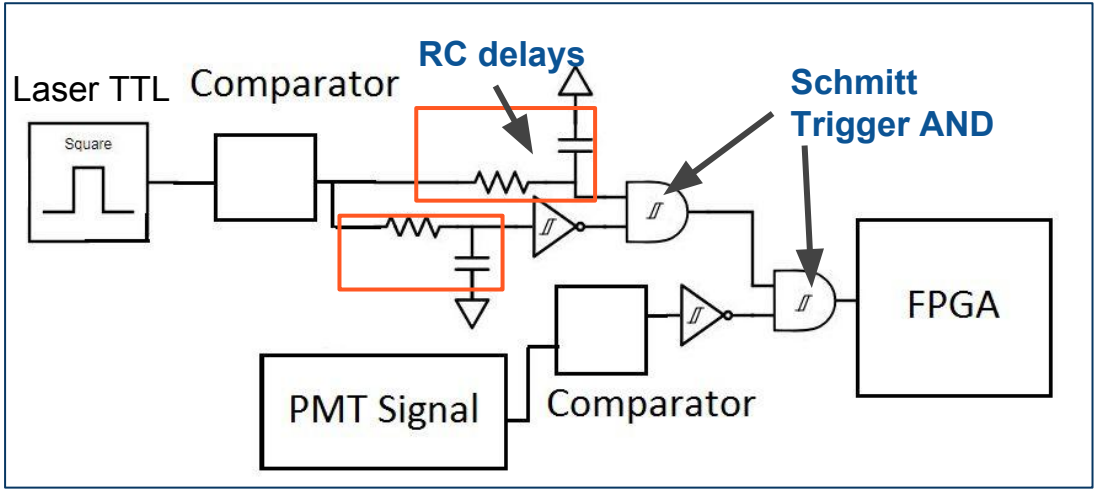
3. AND gate (from 117 lab)

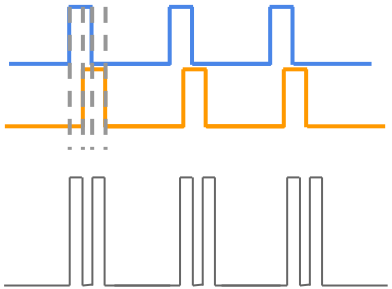
- Made with fastest XOR gates
- *Rigol Waveform Generator*: simulate the PMT noise signal to check logic.



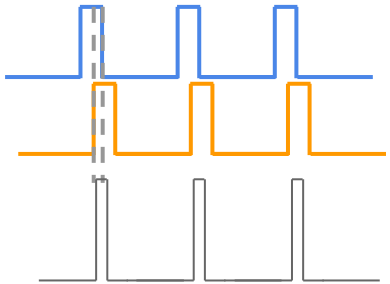
Main Problems & Design Modification (Week 5)

1. Output has 2x frequency than inputs?
   - XOR → AND w/ schmitt trigger on rising edges
2. New method of delay:
   - RC delay
3. Input amplitude (laser TTL) too low for gate operation?
   - Use comparators

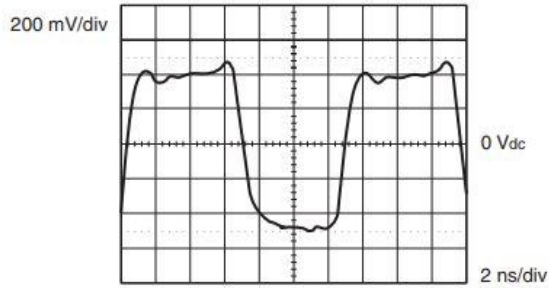




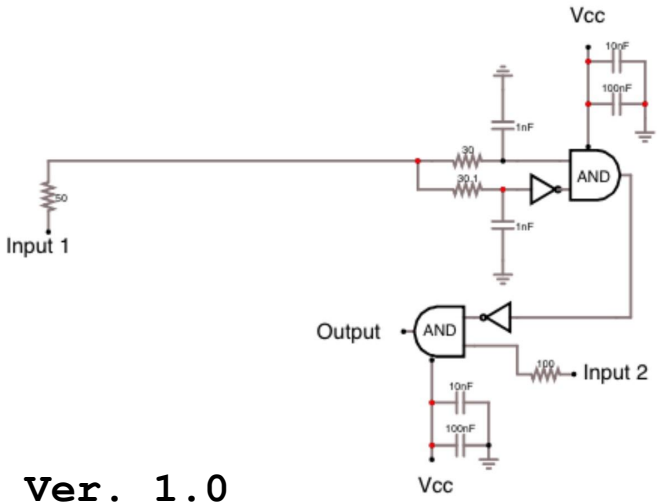
XOR



AND



Improved versions and add-ons (Week 5-6)



Ver. 1.0

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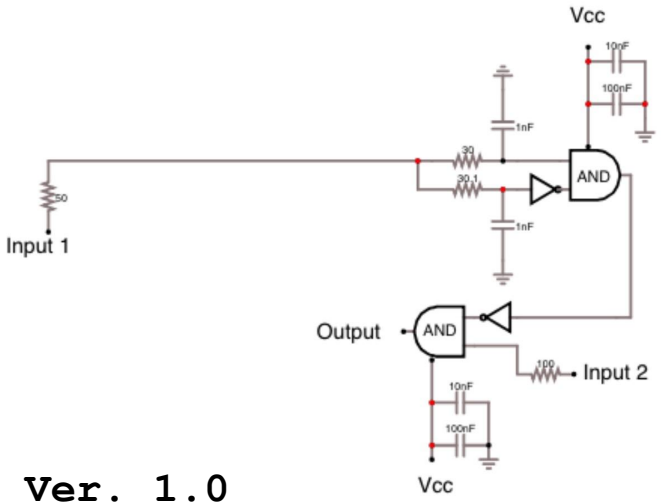

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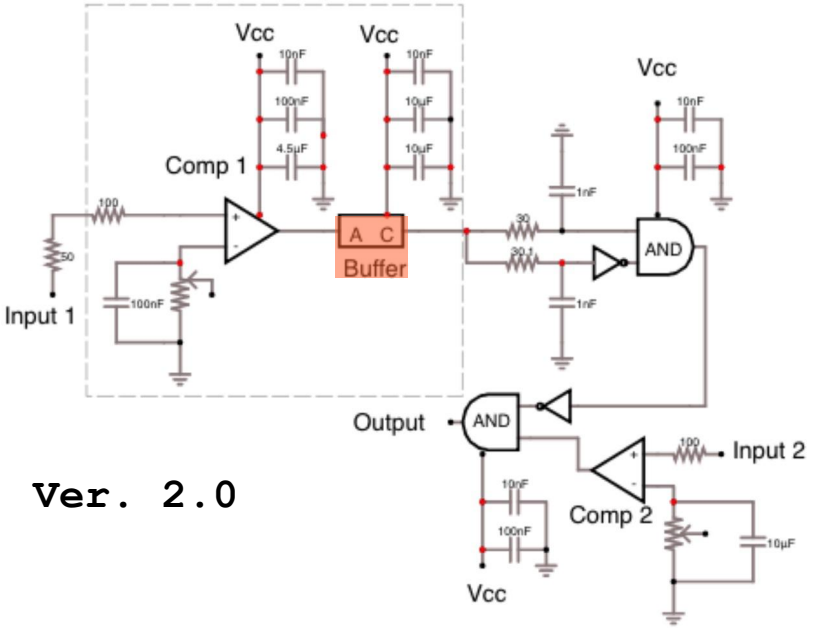

Ver. 2.0

- **Buffer gates**: take a signal that's trying real hard to be digital, clean it up and turn it into a nice, sharp TTL
- **Decoupling/bypass capacitors**
- **Impedance matching resistors**

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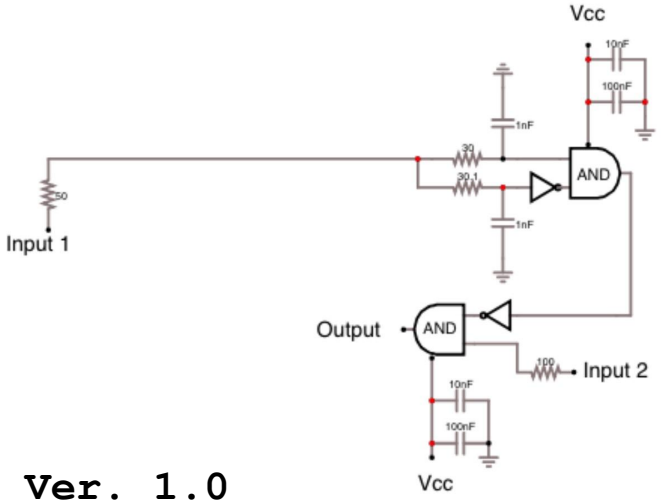

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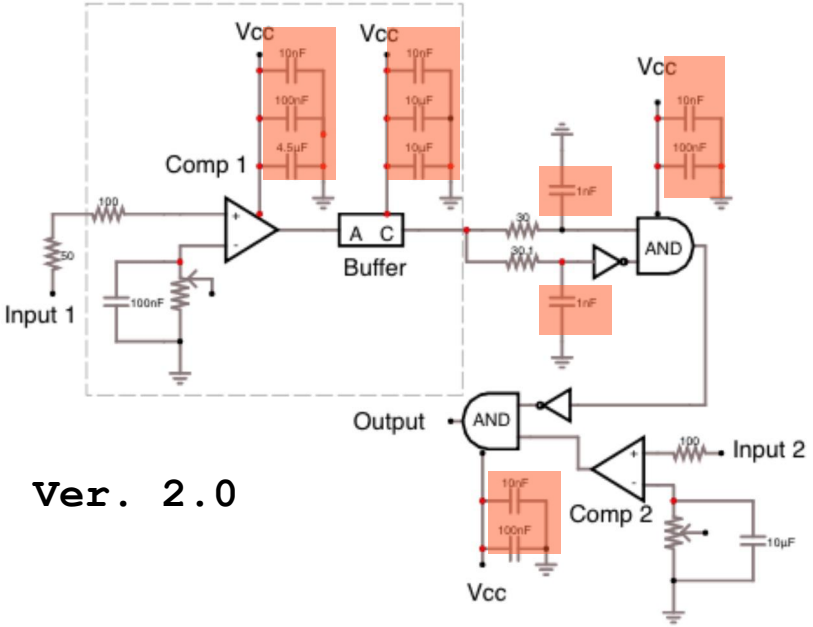

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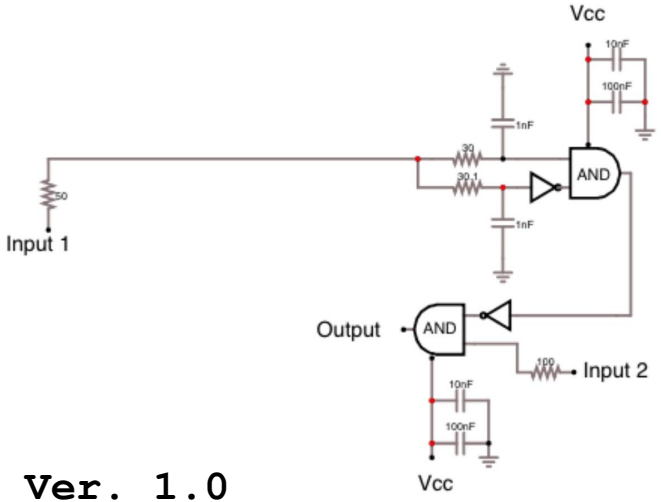

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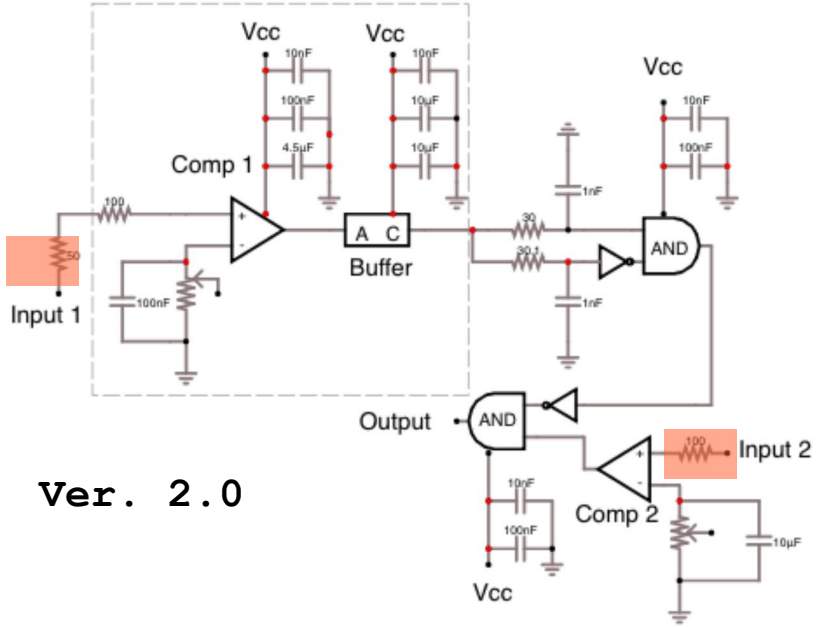

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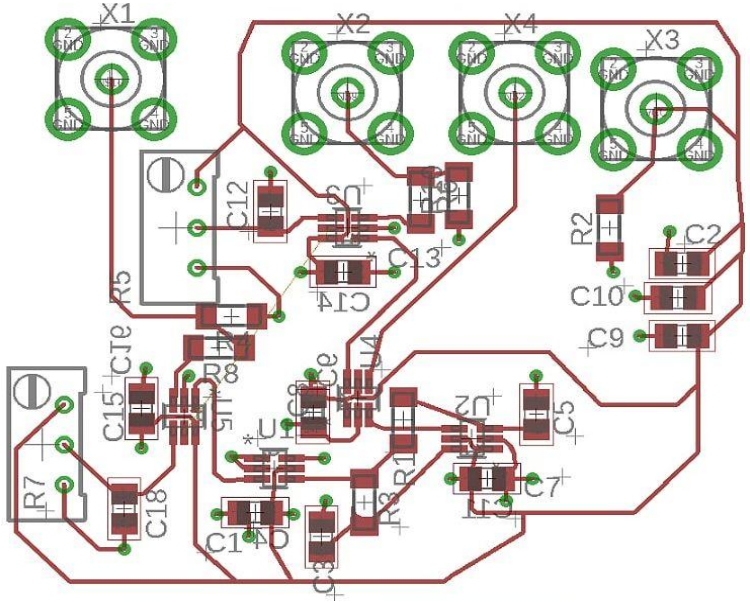
High-speed PCB Design, and Printing (Week 6-8)

Issues to consider:

Timing. Signals on the PCB arriving at the proper time relative to each other?

Integrity. Signal waveforms the same at the final point as the starting point?

Noise.What kind of noise does the signal encounter during its journey on the board?

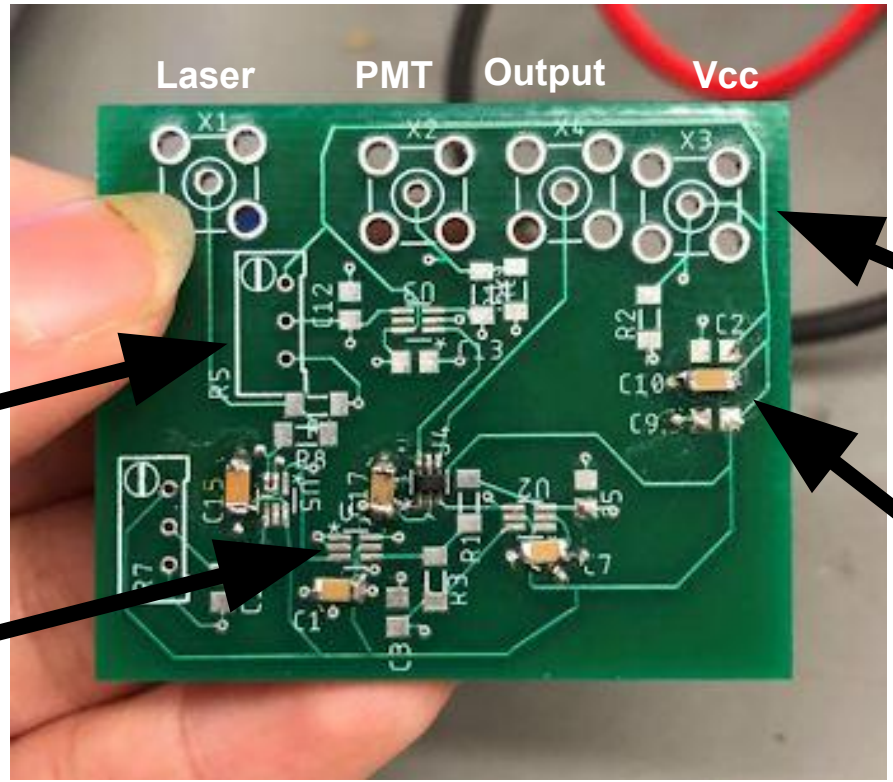


Solutions:

Impedance: Proper impedance between your transmitter and receiver.

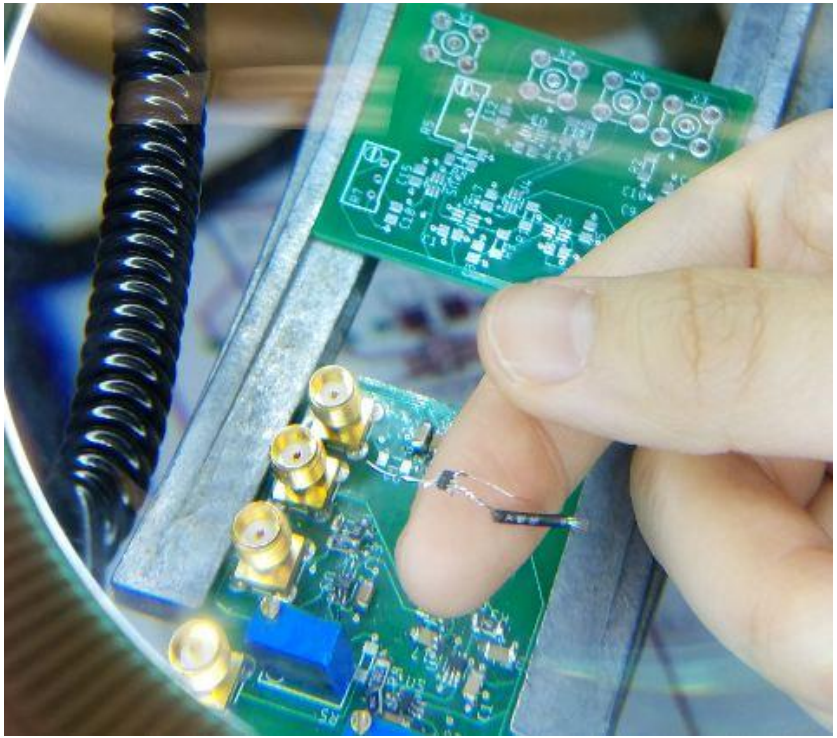
Match lengths, account for propagation delay: Match lengths of two coupled traces s.t. signals arrive at the same time.

Spacing: Close traces are the more susceptible to noise and signal interference.


Laser
PMT
Output
Vcc
X1
X2
X4
X3
PMT tuning potentiometer
Chip pads
SMA cable connectors
Decoupling capacitors

Soldering (Week 9) - a soul-refreshing learning experience

One mistake was made → manually reroute



- Keep temperature ~low
- Chip by chip, start from corner.
- Test each part as we solder.
- Be careful & patient...

Testing part by part (Week 10)

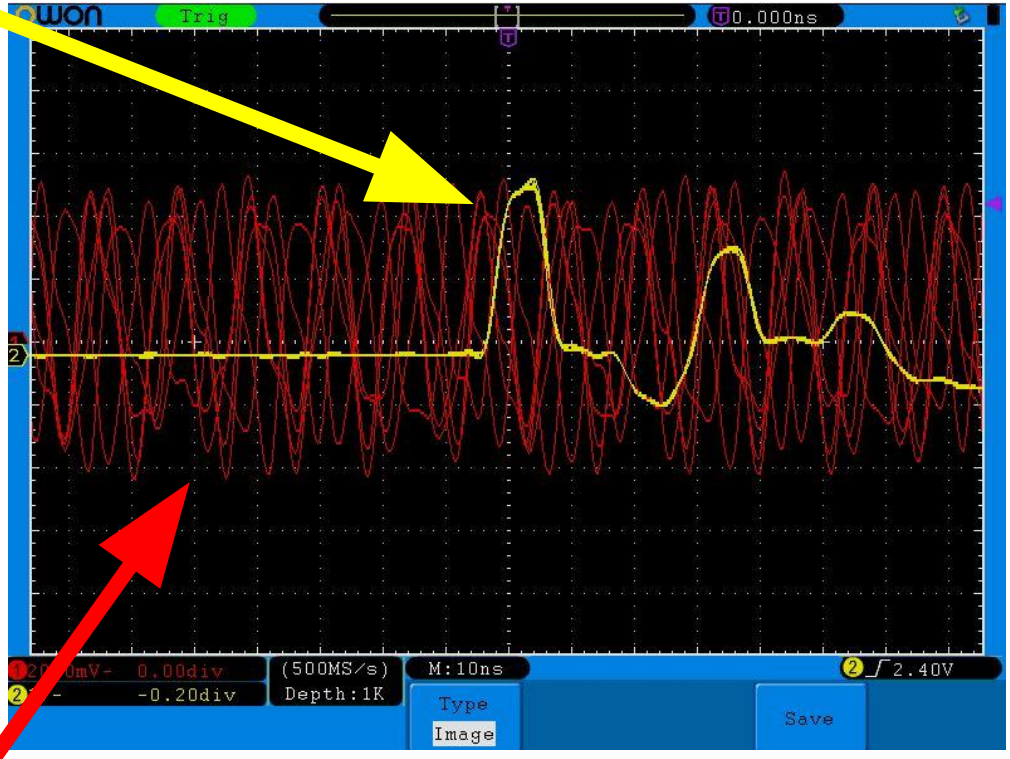
Systematically checked:

1. Power, all inputs
2. Inputs & outputs of the comparators
    a. Tuned potentiometer
    b. Tried with simple square wave
    c. Tried with real signals
3. Inputs & Outputs of gates

“A failure will not appear till a unit has passed final inspection.”

Testing with real inputs (Week 10)

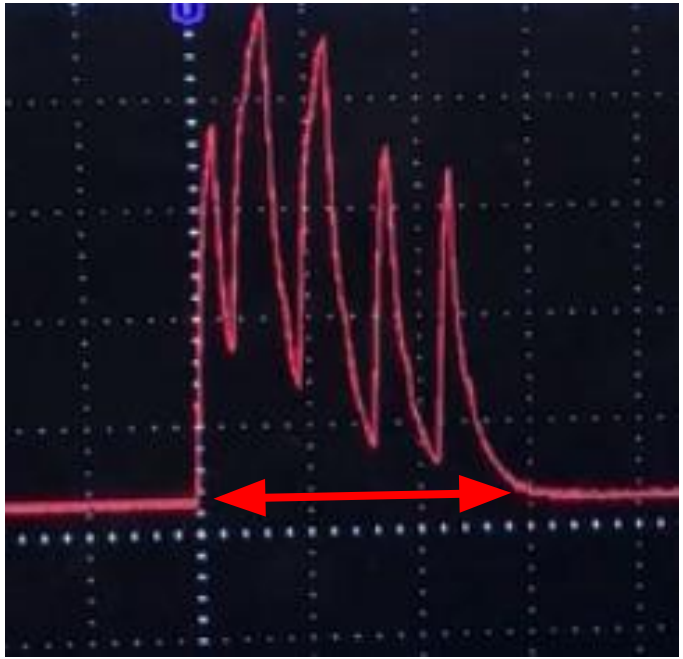
PMT

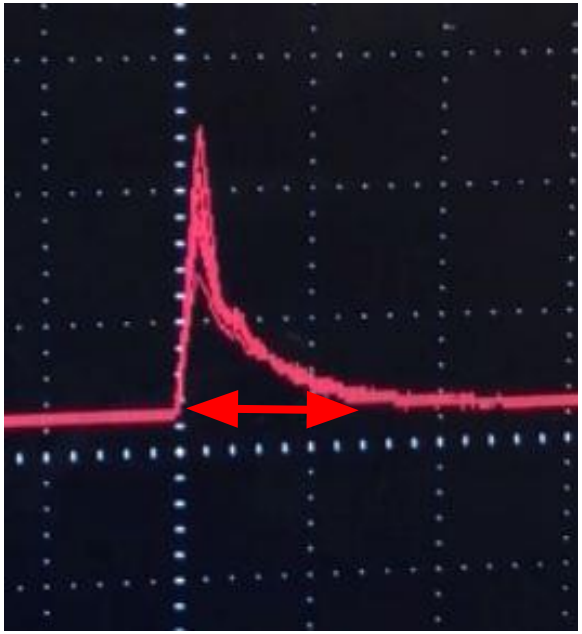


Laser

- Both signals go negative
- Noisy, has ringing

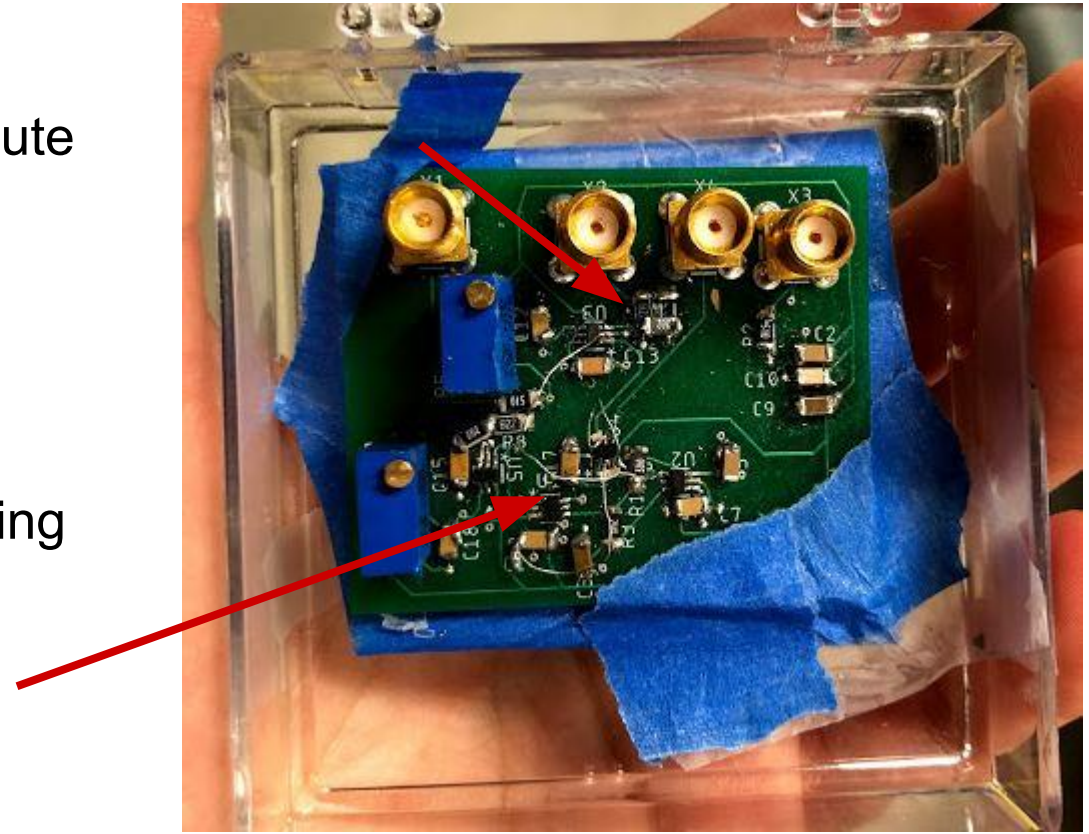
Tuning the pot to clean up





Newest problems and fixes (Week 10)

- Made the wrong connections
  - Small wires to reroute
- Needed to include a voltage divider
  - Piling resistors
- Laser signal not stable when testing
  - impedance matching



Final Budget

Items	Quantity	Price
Boards	4	176.00
AND chips	15	4.17
SMAs	8	39.04
Comparators	12	50.28

Grand Total: $269.49

Original Plan:
HMC721LC3C(FAST XOR GATE) from DigiKey. **$150 each x 2**

Previous Plan: $300.00

Acknowledgements & References

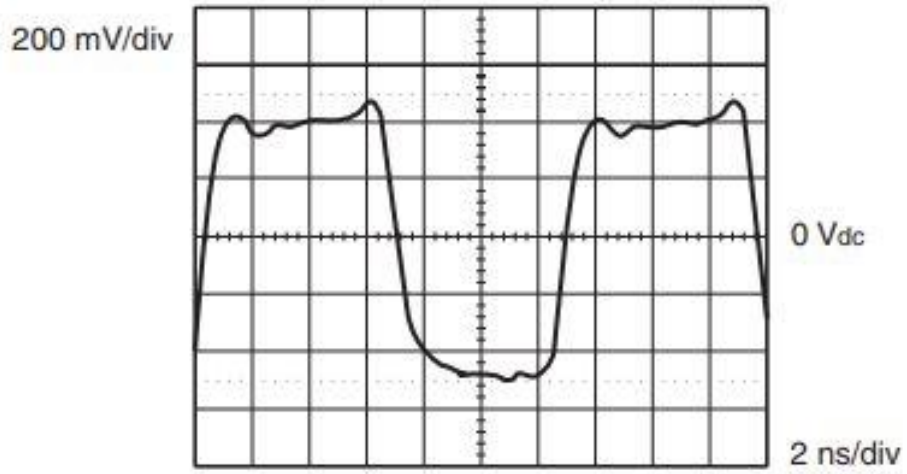
- Christian, Tony for help w/ circuit design
- Peter Yu and Prof. Saltzberg for lending us cables and soldering tools.

[1] Cheng, Zeng, etc. *Recent Developments and Design Challenges of High-Performance Ring Oscillator*
[2] Porat, Dan I. *Review of sub-nanosecond Time-interval Measurements.*
[3] Spetra-Physics Tsunami manual

Testing with real inputs (Week 10)

Laser pulse monitor signal

- Amplitude too small for logic
- No offset, goes below 0V
- Impedance matching to keep the laser locked



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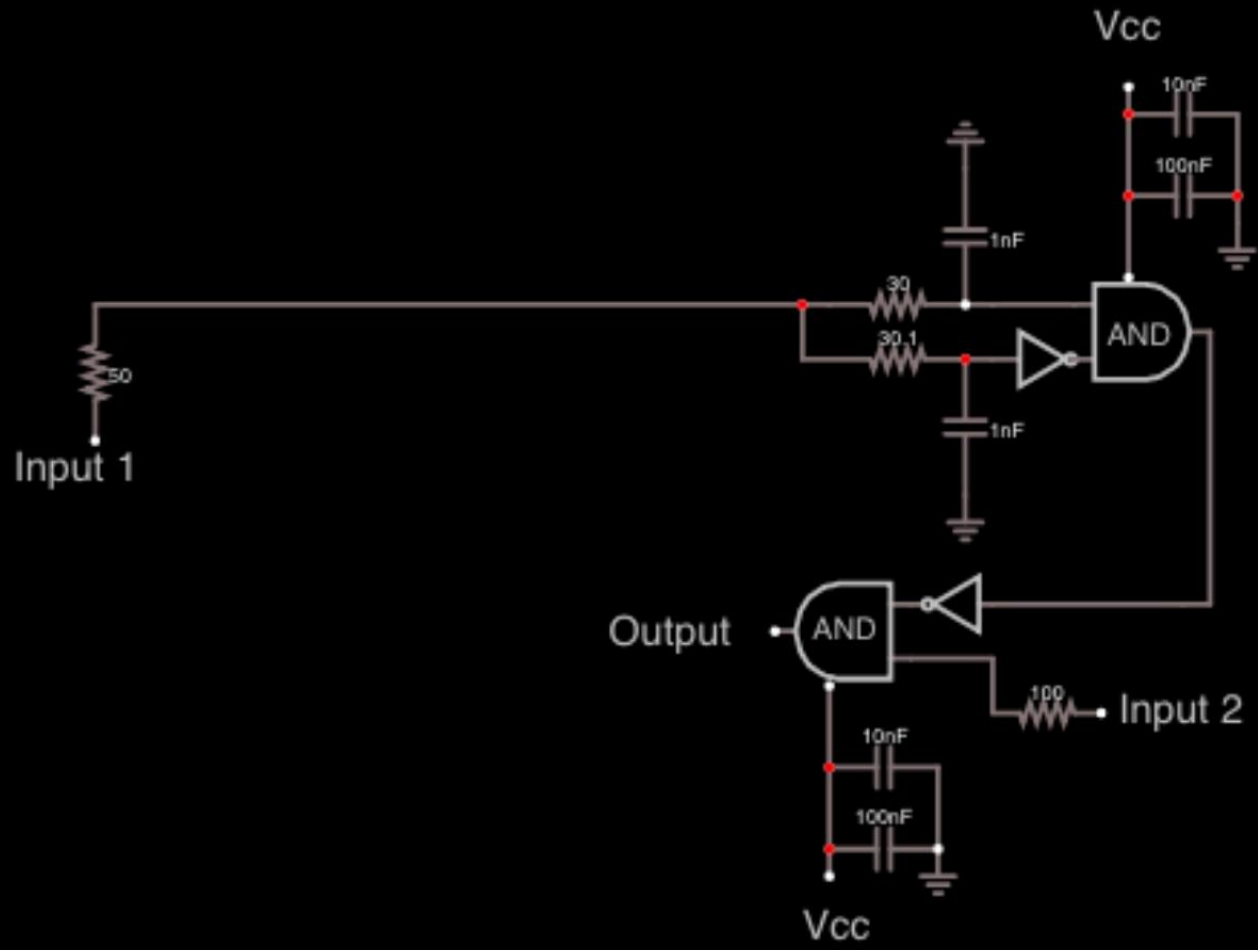
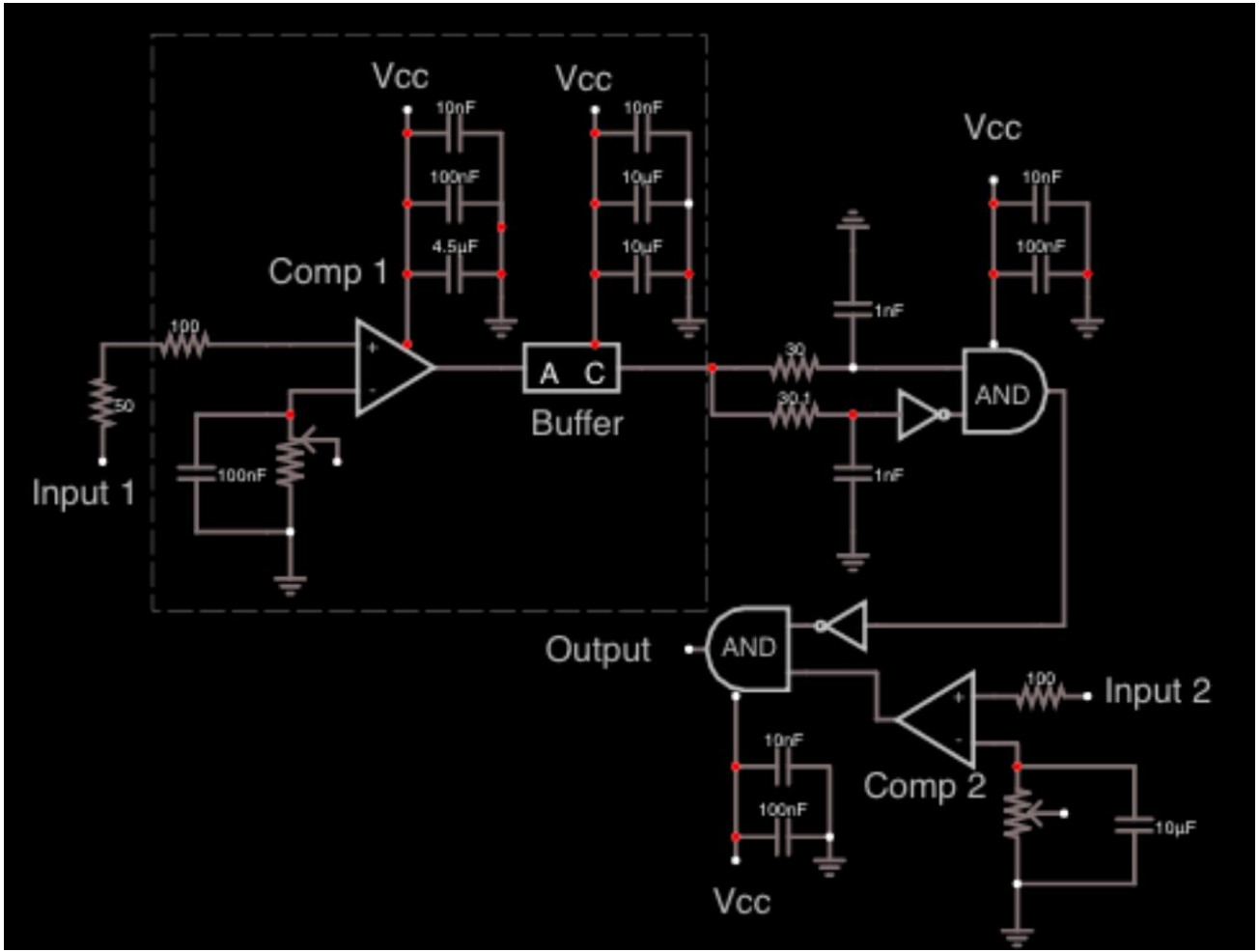
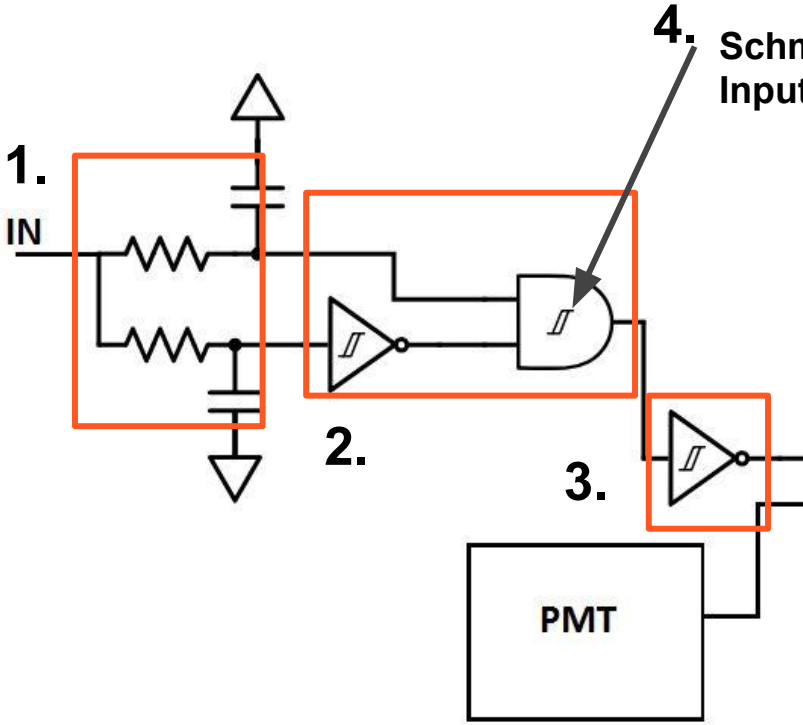

Vcc
10nF
100nF
1nF
30
30.1
AND
50
Input 1
1nF
Output
AND
100
Input 2
10nF
100nF
Vcc


Vcc
Vcc
Vcc
10nF
10nF
10nF
100nF
10µF
4.5µF
10µF
Comp 1
100
50
Input 1
100nF
A C
Buffer
30
30.1
1nF
1nF
AND
Output
AND
100
Input 2
10nF
100nF
Comp 2
10µF
Vcc

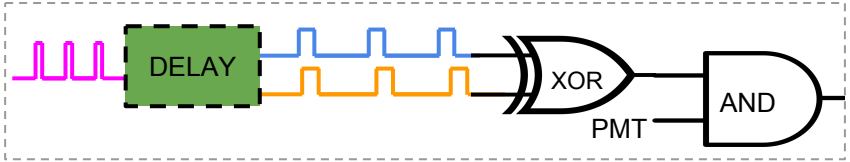
Encountered Problems & Design Modification (Week 5)

1. New method of delay
2. XOR changed to AND with inverted input
3. NOT added to work with the change from XOR
4. Schmitt Trigger inputs to trigger only on rising edges

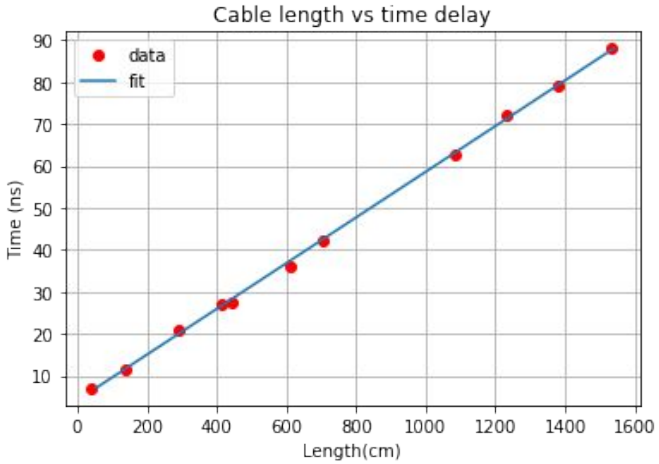


Implementing with lab parts

Initial proposed logic



1. DELAY: two BNC cables of different lengths



Time delay created Δt ~ Difference in length ΔL

2. XOR gate:

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XOR in lab	CD4070B	6.8
Purchased XOR	7AC11086	3.8

T_{pd}= Propagation delay in the chip itself, lower bound for rise time: Δt has be be > T_{pd}

Summary of prototype results:

Type	Model	T_{pd} (*ns*)
NANDS in lab	SNX4LS00	9
XORs in lab	CD4070B	6.8
Purchased XORs	7AC11086	3.8

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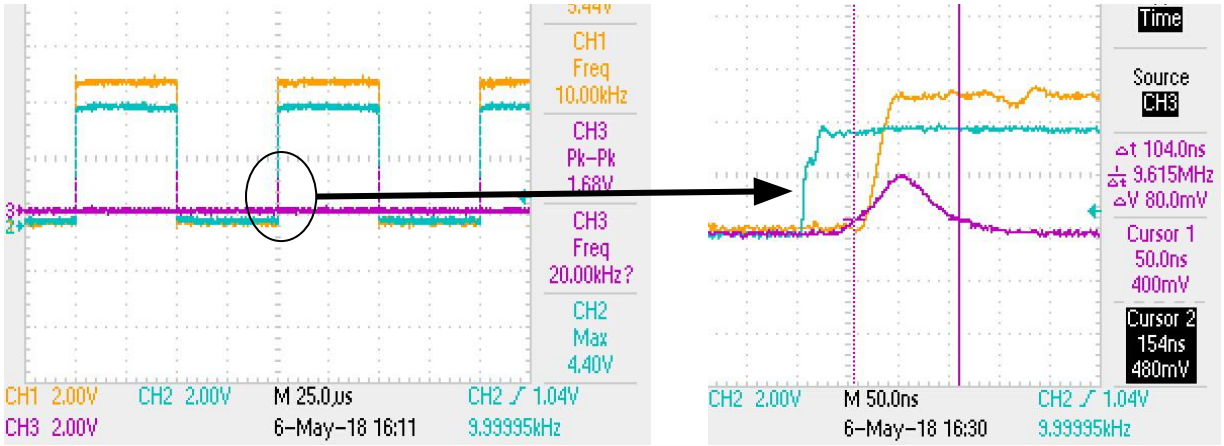
Output of this XOR was noisy, unable to resolve the Δt delay

Able to resolve hundreds of *ns* pulse width.
Logic worked, but output was not exactly as desired.



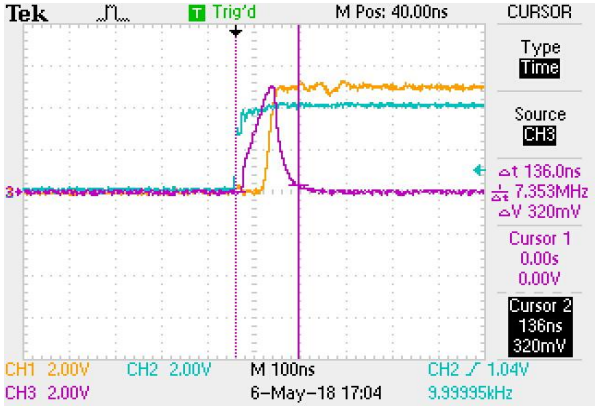
Summary of prototype results:

Type	Model	T_{pd} (*ns*)
NANDS in lab	SNX4LS00	9
XORs in lab	CD4070B	6.8
Purchased XORs	7AC11086	3.8

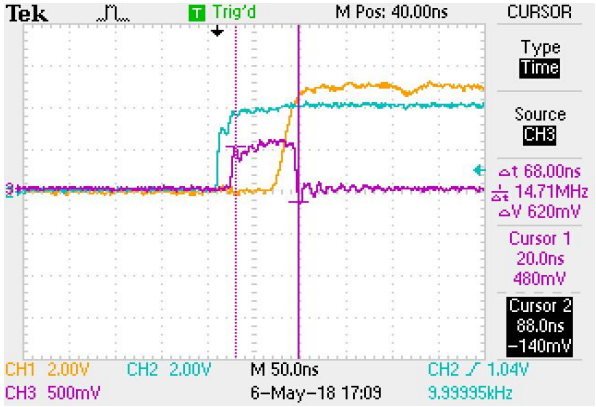
Multiple stages, very slow.
Output of this XOR was noisy, unable to resolve the Δt delay

Able to resolve hundreds of *ns* pulse width.
Logic worked, but output was not exactly as desired.

Clean square-wave output with Δt =68ns, but attenuated in amplitude.



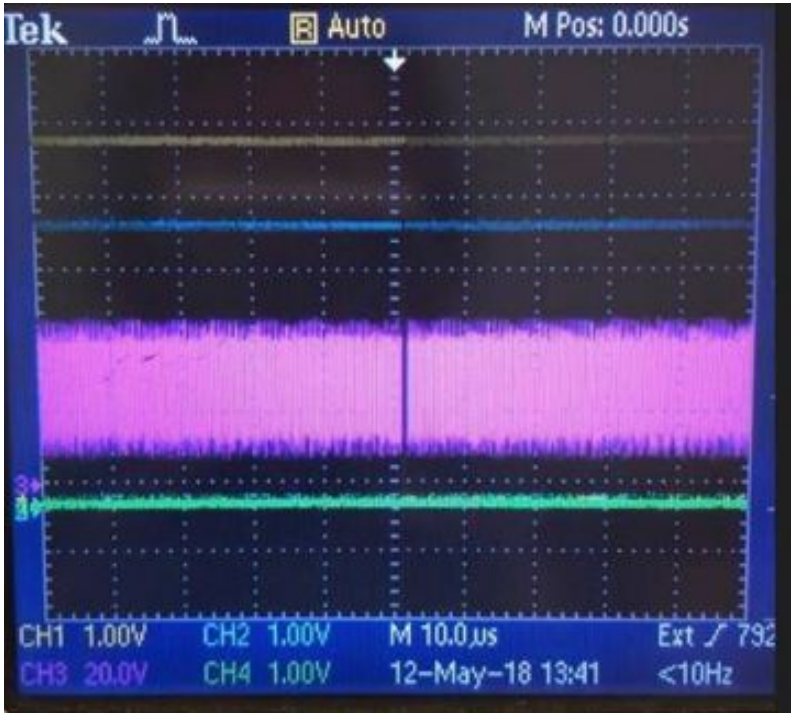
x1 attenuation



x10 attenuation

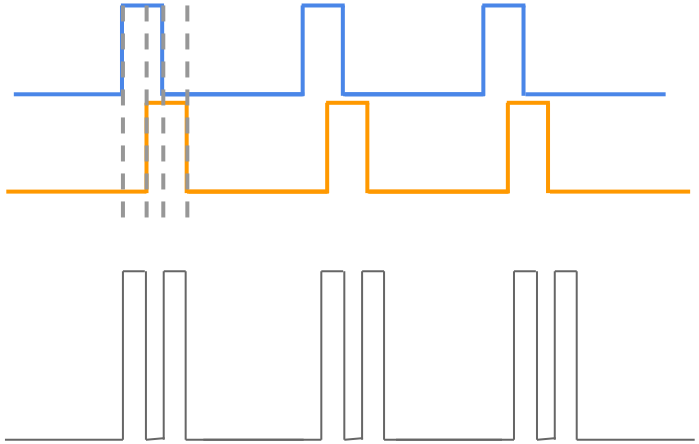
Results - Noise Subtraction

- Made with faster XOR gates
- *Rigol Waveform Generator*: used to simulate the PMT noisy signal to check logic.



Some problems found in slow prototype

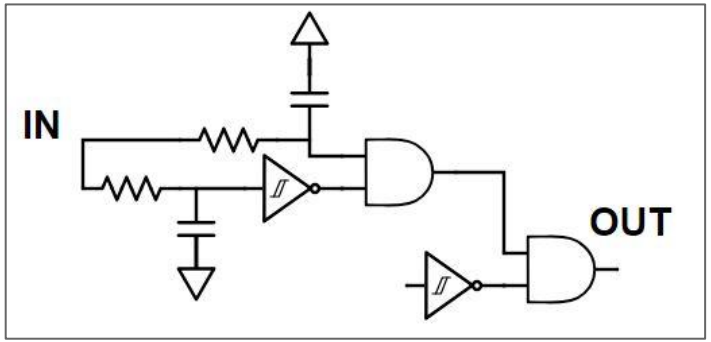
- The output peaks have 2x frequency than inputs
- Laser TTL’s amplitude is too low for gates.
- High frequency bounce and jitter
- Testing
  - Back-reflection distorting the output
  - BNC lengths



Improved design!

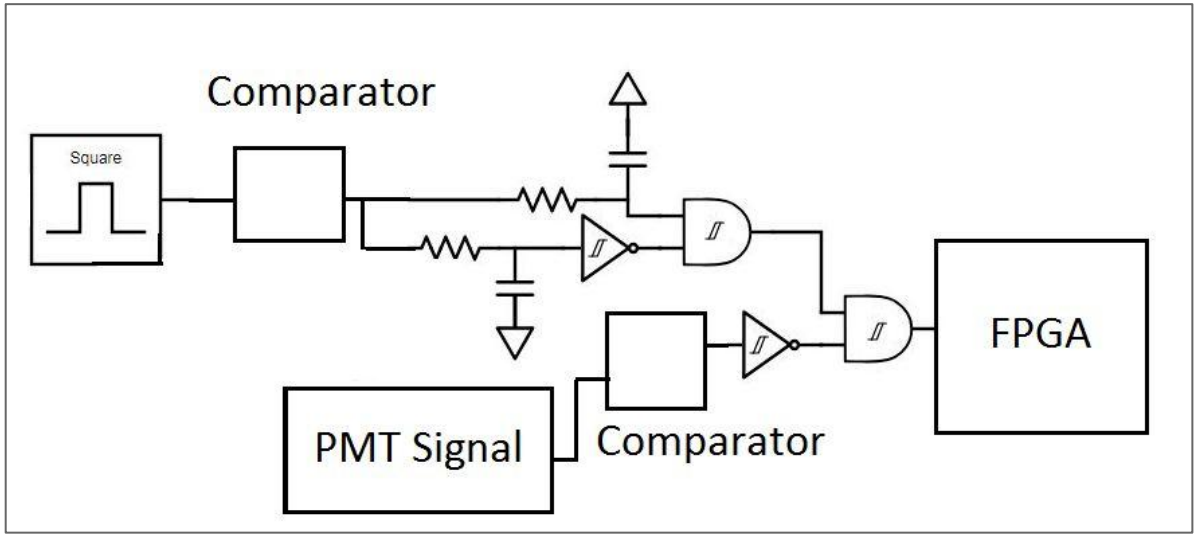
Basic logic:

- Used RC for delay
- AND gates with Schmitt trigger on inputs.



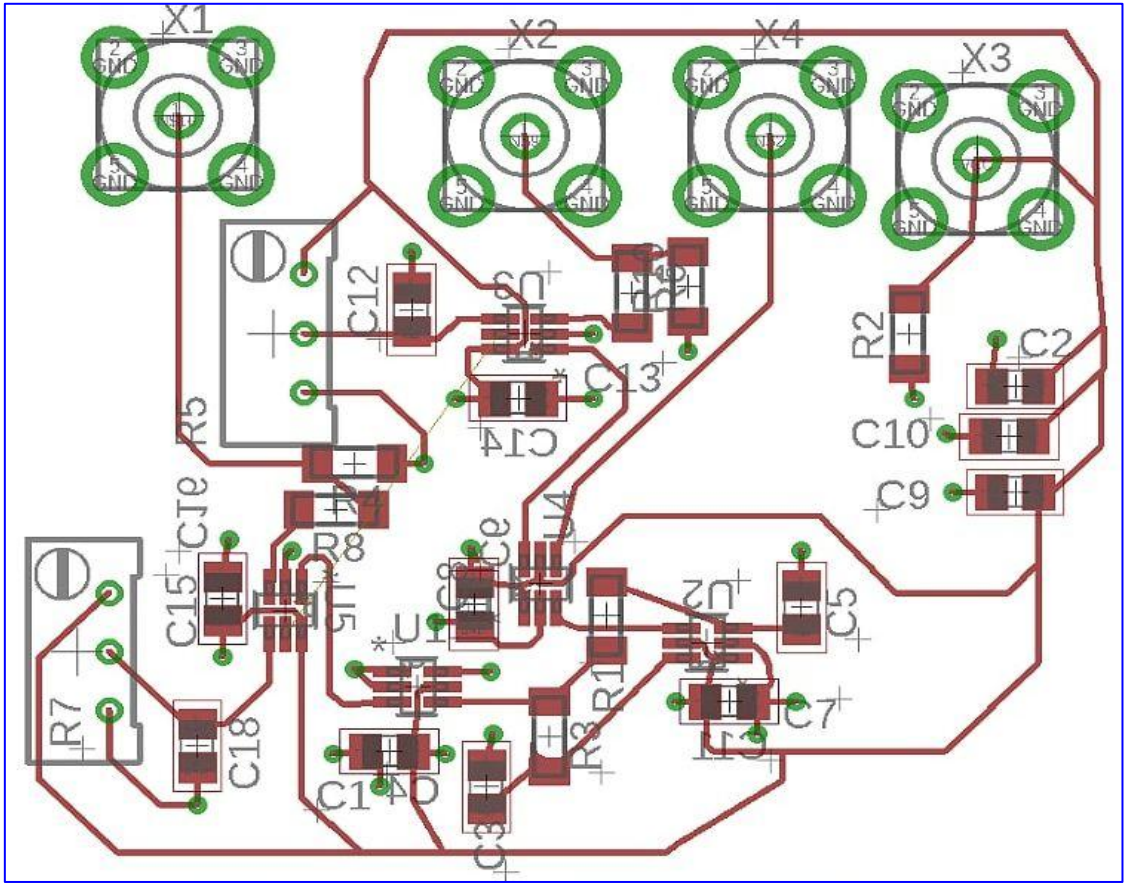
Add ons:

- Comparators on inputs
- Decoupling capacitors
- Buffers to clean up the signal.



High speed PCB board design & considerations

- SMAs to replace BNCs
- Various add-on components (capacitors, resistors, buffers, etc.) to ensure signal is nice.
- Followed high-speed PCB board design rules.
- Closely placed components
- Surface mounted parts

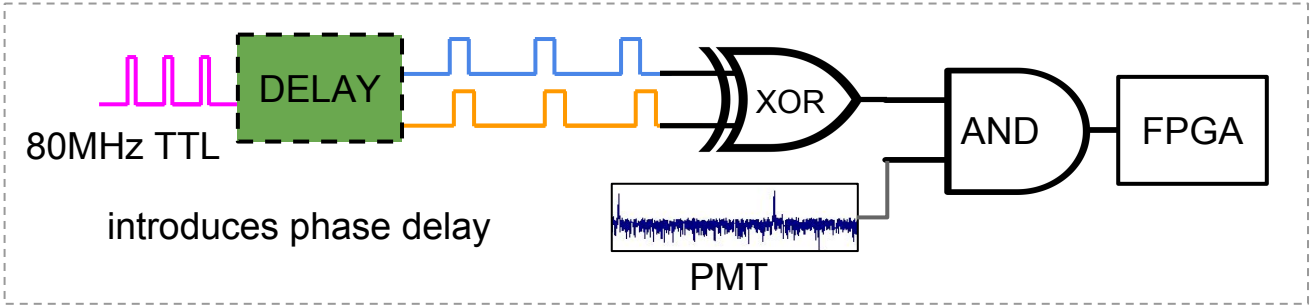


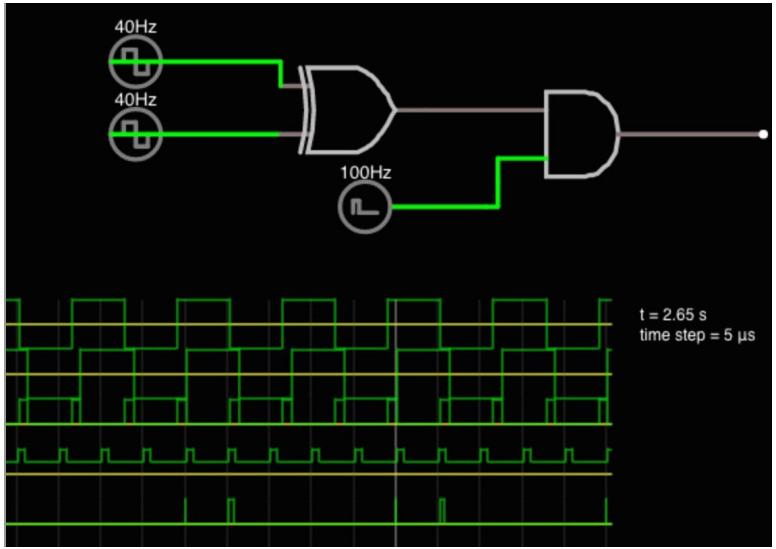
Planned	Comments and adjustments
Week 3: Build and test the circuit, basically, have a prototype of a slow version to make sure logic works.	
Week 4: Improve on the prototype to push for as fast as possible. Calculate the timing, rise/fall times, impedance matching for the fast design. Run some simulations of convolution of two functions.	
Week 5: Improve on the design based on prototype. **Start and finish implementing the actual design with fast electronics.**	We are currently starting to put together the new fast design, it's projected that the circuit board design will take a long time as timing is important. **Adjustments:** **Week 7,8- Finish the complete circuit board design on Eagle, with details of wire lengths, capacitance/resistor values, gate specs, etc., figured out.**
Week 6: **Testing, debugging and improving.**	
Week 7-8: Finalize the product. Test out with ion trap system and obtain actual results.	**Week 9: Finalize and test out the board. Write up final report.**

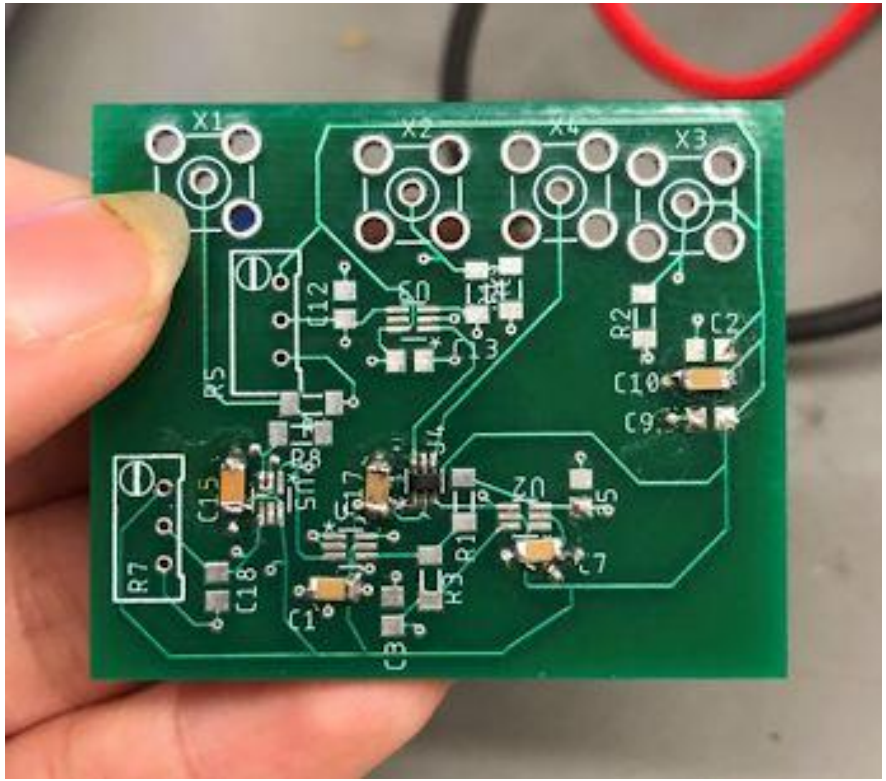
Testing the PCB

- Tested each block
- SMAs and adapters
-

Initial proposed concept

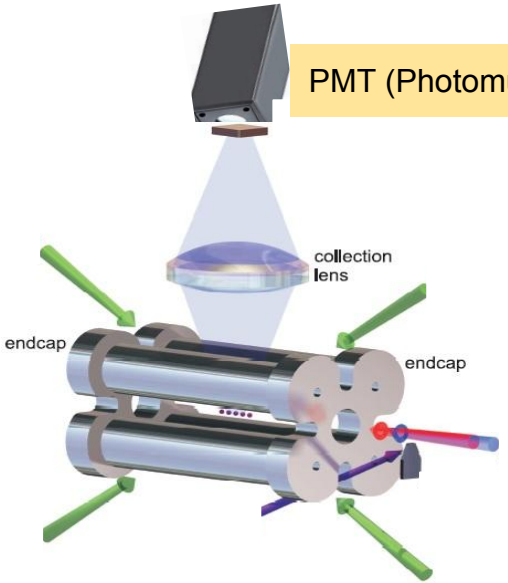


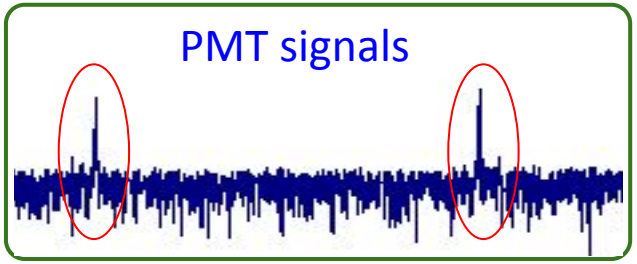



X1
X2
X4
X3
R2
C2
C10
C9
R7
C18
C1
C7
R1
C15
C17
C12
R5
R8
U2
U4
C8
R3

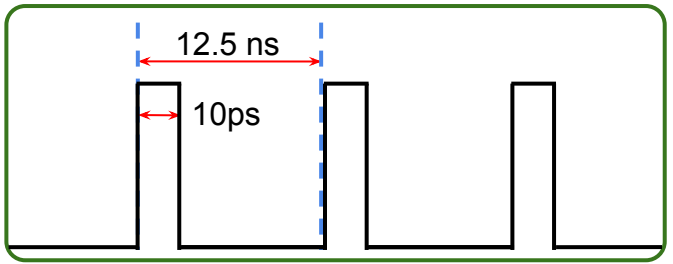
Brief overview of project

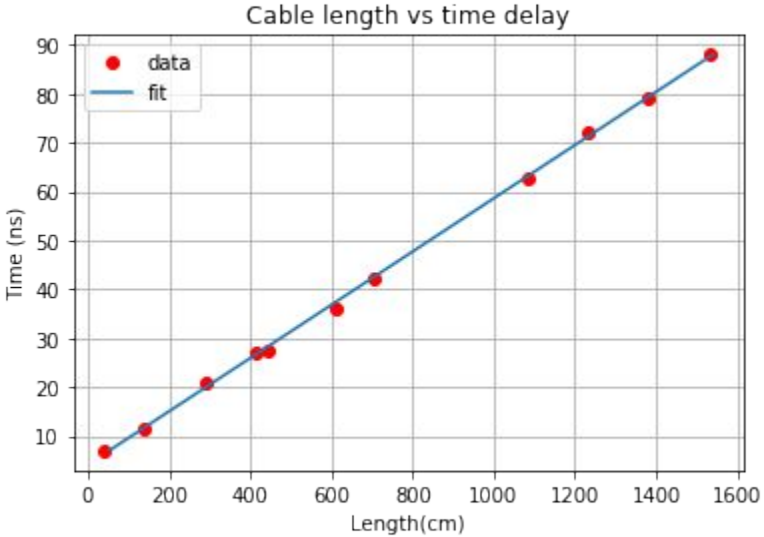
Ion trap system (for visualizing)





Unwanted spikes from laser pulses





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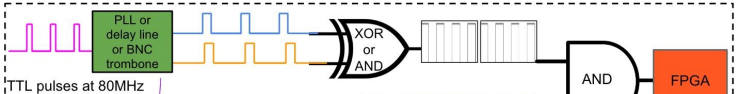
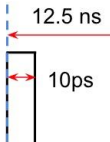
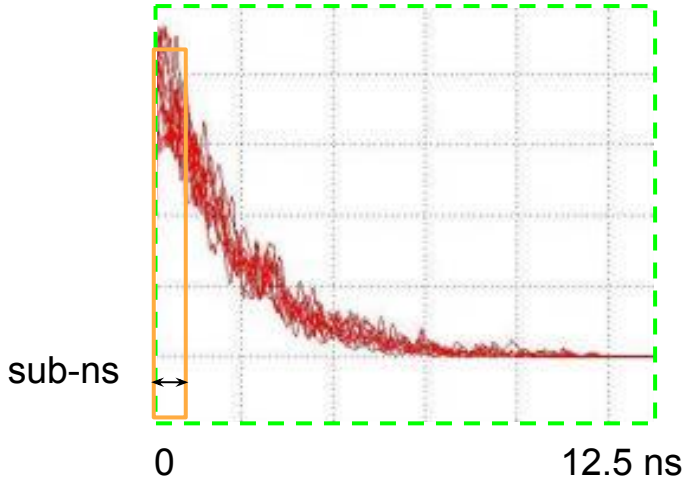
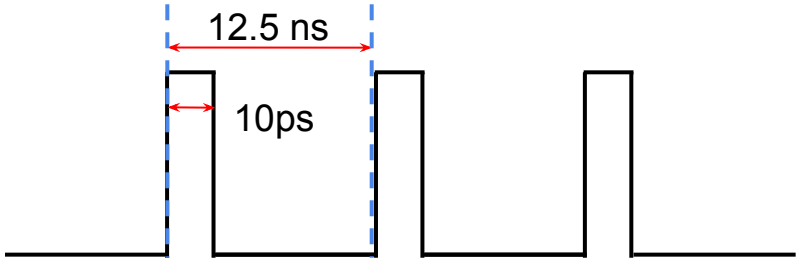




Introduction to the Problem & Objective

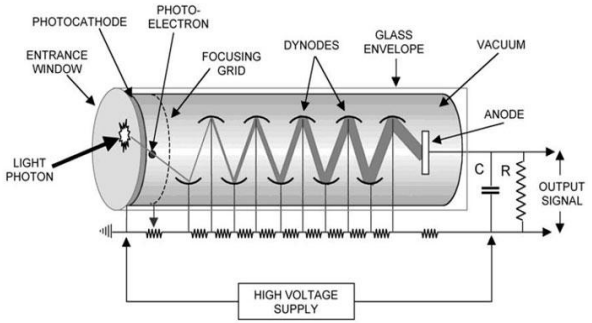




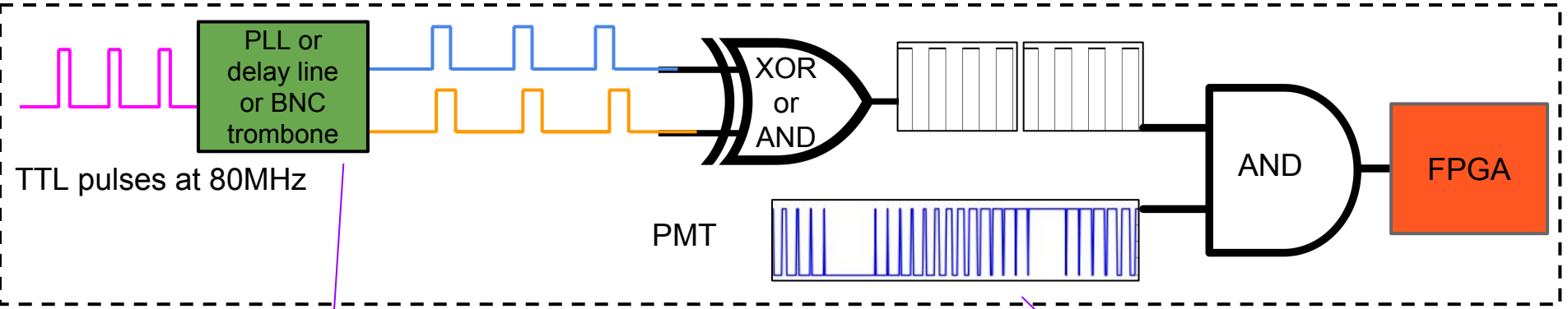
Objective: Create a sub-nanosecond or picosecond time-resolved "window" to look at the PMT signals, and scan this window in time to reconstruct the cleaner PMT signal.

Some approaches

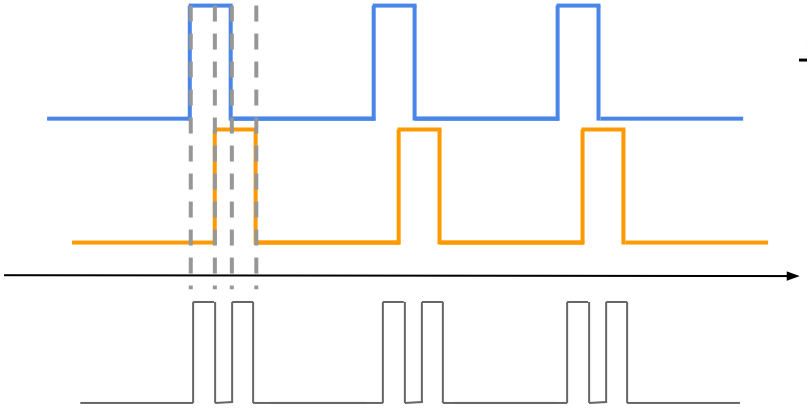
- Time tagging using time-interval measurements:
  - TDC (time-digital converter)[3,4]: output the time interval between two events.
    - Ring Oscillator TDC (1-2ps resolution), CMOS TDC (1ps), delay-line based digital TDC...
    - Issue: data storage & retrieval time.
  - Vernier method - the idea of using two clocks of Slightly different periods and the time interval between Them to be measured is expanded by a factor k
- Gating the PMT:
  - Where to gate? Photocathode has rise/fall time.
- Well then... **messing with the PMT output signals!**



Proposed design

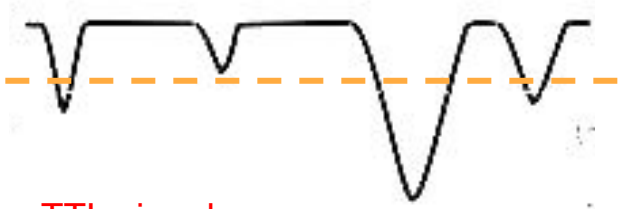


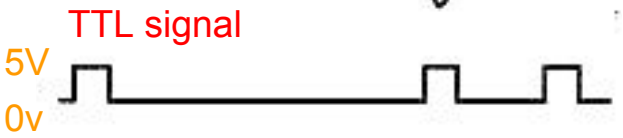
Introduce phase delay



A	B	O
0	0	0
0	1	1
1	0	1
1	1	0

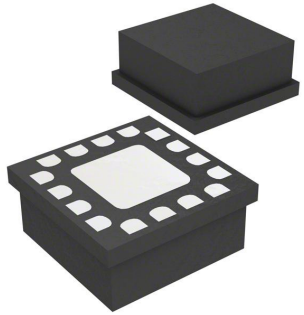
Some PMT Signal, for example





Parts, Planned timeline and Evaluation metric

- HMC721LC3C (14 Gbps, **FAST XOR / XNOR GATE**) - DigiKey
  - Fast rise and Fall times: 19 / 18 ps. Time resolution 14 GHz (70ps)
  - $150 each



Week 3: Build the **ciruitry**. Prototype a **slow version** to make sure logic works. Purchase parts.

Week 4: Improve on the **prototype** to push for as fast as possible. Run some **simulations** of convolution of two functions.

Week 5: Improve on the design based on prototype. Start and finish **implementing the actual design** with fast electronics.

Week 6: Testing, debugging and improving.

Week 7-8: Finialsize the product. **Test out** with ion trap system and obtain actual results. If time allows, try out TDC.

Week 9 -one of us won't be here (hopefully): Writing up report and working on final presentation.

Evaluation:

- Prototype(s) of slower version and output data. Simulation results. (40% for correct designs of prototype)
- Test results from using the fast autocorrelator on the real experiment. (60% actual implementation)

References

- The Almighty Tony
- Professors Whitehorn and Campbell, who provided invaluable thoughts and advice on possible designs
- Literature (lot of IEEE papers)

[1] Image from *Chapman Labs at Gatech*
[2] Image from "*An Attempt to Calibrate the Laser Induced Fluorescence (LIF) Signal used for Oil Film Thickness (OFT) Measurements in Simulating Test Rigs."*
[3] Cheng, Zeng, etc. *Recent Developments and Design Challenges of High-Performance Ring Oscillator CMOS Time-to-Digital Converters*. IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 63, NO. 1, JANUARY 2016.
[4] Porat, Dan I. *REVIEW OF SUB-NANOSECOND TIME-INTERVAL MEASUREMENTS.*

Introduction to the problem (setup of experiment):
Objective: To make a XOR gate which can perform a desired operation in 12 picoseconds
Methods (two routes, talk a lot about the available ways):
Proposed scheme and design (talk about the planned implementation):
Planned Timeline:
Parts:
Evaluation metric (two prototypes? One actual pne with fast electronics and tested out, python simulation): First test with a slower frequency breakdowns using parts that can be found in the lab, we already have a TDC that can take in two inputs, and we can put this together with a XOR gate in the lab. The two inputs for the TDC can be tested using a function generator. As the circuit gets faster, we plan to do a python simulation