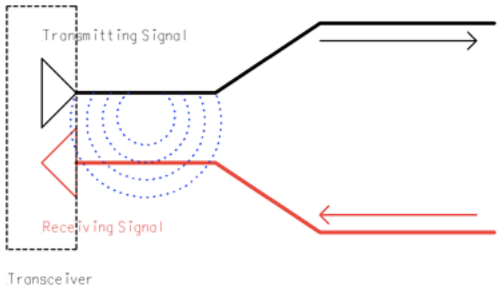
Compilation of High Speed PCB Designing Guidelines

I. What do we care in high speed PCB design

- High speed PCB design comes in when the *physical characteristics* of our circuit board (such as layout, packaging, layer setup, interconnections, etc.) start to affect our signals. Common problems include delays, attenuation, crosstalk, reflections, or emissions...
- Both *digital* and *analog* signals are prone to interference by outside environment, this is called the **Signal Integrity (SI).** On a board, let's say your have a path transmitting signal between point A and point B –a lot of things can happen along this path that can interfere and destruct the integrity of our signals. Some of the things that can interfere:
    - **Signal reflection**: when we transmit a signal along a copper trace, some of the signal gets reflected back to starting point.
    - **Signal ringing:** when there's some unwanted *shifting* in the voltage or current on your trace, which causes extra current to flow and causes delays in the arrival of our signal at its final destination.
    - **Signal noise**: when there's random *fluctuation from another signal* on your board, which can affect other signals in proximity to it.
    - **Signal crosstalk**: when two traces/copper wires are placed too close together, and RF radiation from one signal causes a disruption in the other signal.



    - **Signal timing**: when out sent signal doesn't reach the final destination in time to line up with its clock signal.
- **So generally the things we care in high speed PCB board:**
    - **Timing**. Are signals on the PCB layout arriving at the proper time relative to other signals?
    - **Integrity**. Are the signal waveforms the same at the final point as the starting point?
    - **Noise**. How much/what kind of noise does the signal encounter during its journey on the board (from transmitter to receiver)?
- **Solutions** to eliminating these problems are to consider the following in our design:

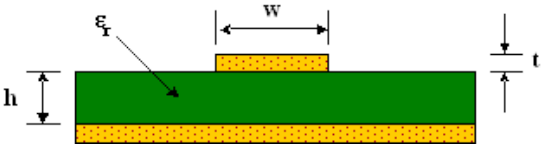
- **Impedance:** *Proper impedance between your transmitter and receiver* directly impacts the quality and integrity of your signals. This also affects how sensitive your signals are to noise.
- **Matching lengths**: Match lengths of two coupled traces to ensure signals arrive at the same time & in sync with your clock rates.
- **Spacing**: Closer traces are the more susceptible they are to noise and signal interference.

II. Key fundamentals of high speed PCB layout techniques

From TI's *High Speed Analog Design and Application Seminar*

Let's look at the **PCB components**

- **Cooper traces**
  - Purpose: to connect to two or more points on board
  - Problem: *Trace Inductance and Capacitance.*
    - The shape of these traces determine (one very important aspect of a PCB) – the *characteristic inductance, capacitance*, and ultimately the characteristic impedance. *Resistance* is generally ignored as most designs do not carry more than **mA**.
    - PCB inductance & capacitance calculator.

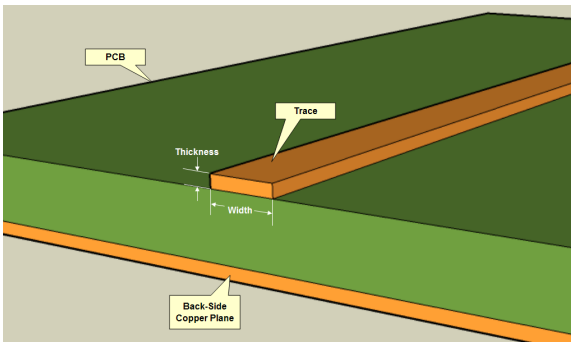


$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} Ln\left(\frac{5.98H}{.8W + T}\right)$$

$$C_0 = \frac{2.64 \cdot 10^{-11}(\varepsilon_r + 1.41)}{Ln\,[5.98\,H\ /(.8W\ + T)]}$$

$$t_{pd} = 3.34 \cdot 10^{9}\sqrt{.475\varepsilon_r + .67}$$

W is the trace width (cm), ***H*** is the trace height (cm), and ***T*** is the thickness of the copper trace (cm). $\boldsymbol{\varepsilon_r}$(permeability) for FR-4 is ~4.5. $\boldsymbol{t_{pd}}$ is propagation delay. CHECK WITH PCB MANUFACTURER TO DETERMINE THE MATERIAL.



- **Cooper planes**
  - Purpose: For ground planes and power planes
  - Problem: *Stray Capacitance* on signal traces.
  - Benefit: Large Bypass Capacitance & Minimal Inductance
    - Planes make an excellent high frequency capacitor, and can often be utilized for high frequency bypassing in complement with traditional capacitors.
    - *Solid plane* over *grid plane*, because solid plane minimizes inductance which is good for high speed signals (analog and digital). Also, solid plane is a good thermal conductor, can be a heat sink. But this plane can cause capacitance problems to sensitive nodes of the circuit.
  - Capacitance:

$$\mathrm{C(pF)} \approx \frac{0.0886\ \varepsilon_r\ A}{h}$$

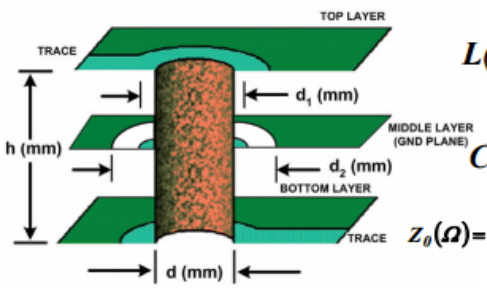
h is separation between planes (cm). ***A*** is area of common planes is length * width (cm^2).

- **Vias**
  - Purpose: to interconnect traces on different layers
  - Problems: Inductance & Capacitance
    - Generally we ignore these problems as the length of the vias are typically very small relative to the rest of the trace. But, ***if the signals are very high frequency (>100MHz)***, this can cause issues. The easiest way to fix is to simply not use the vias.
  - Inductance:

$$\mathrm{L(nH)} \approx \frac{h}{5}\left[1 + \ln\left(\frac{4h}{d}\right)\right]$$

  - Capacitance:

$$C(\text{pF}) \approx \frac{0.0555\ \varepsilon_r\ h\ d_1}{d_2 - d_1}$$



$$L(nH) \approx \frac{h}{5}\left[1 + ln\left(\frac{4h}{d}\right)\right]$$

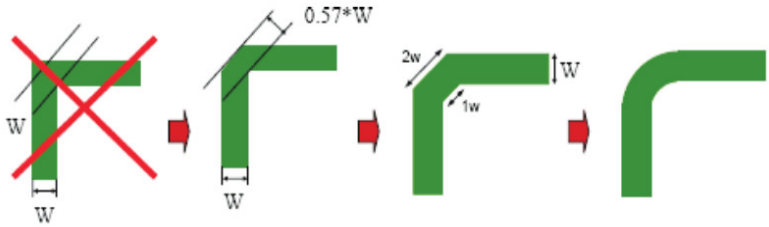
$$C(pF) \approx \frac{0.0555\ \varepsilon_r\ h\ d_1}{d_2 - d_1}$$

$$Z_0(\Omega) = 31.6\sqrt{\frac{L(nH)}{C(pF)}} \qquad T_p(ps/cm) = 31.6\sqrt{L(nH)C(pF)}$$

Some PCB design keys:

Traces and vias design

- Right angle in a trace causes more radiation! Capacitance increases in the region of the corner, and the characteristic impedance changes. This impedance change causes reflections**.**



- To minimize impedance change, the best routing is a **round bend**.
- Separate high-speed signals from low-speed signals, and digital from analog signals.
- To minimize crosstalk not only between two signals on one layer, but also between adjacent layers, route them with **90°** to each other.
- Good via placement to avoid/reduce large loop areas.
- Vias add inductance, capacitance, and reflection due to change in Z_0.

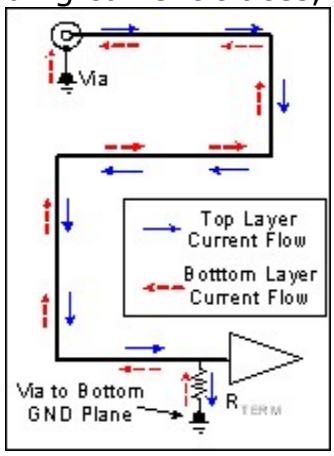
Return Currents and loop areas

- Current density is important when looking at return currents. For current to flow, there must be a return path, so the currents will find its way back to the source one way or another.

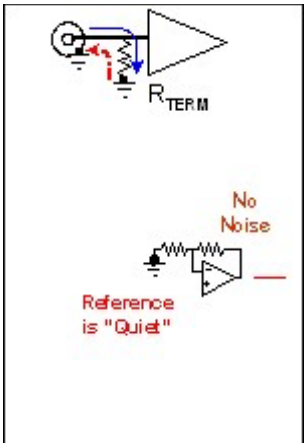
$$I(A/cm) = \frac{I_o}{\pi h}\frac{1}{1 + (\frac{D}{h})^2}$$

I_o is total signal current (A), ***h*** is height of the trace (cm), ***d*** is distance from the trace (cm).

- Must have a solid ground plane as return path for lowest impendence! High frequency current paths always follow the path of least impedance - Not Resistance.
- Avoid long winding current traces, large current loop area.



Bad: large current loop



Best: minimum current loop

Decoupling (Bypass) Capacitors

- 1 (decouple): to decouple one component in the circuit from another. Noise caused by other circuit elements is shunted through the capacitor, reducing the effect it has on the rest of the circuit.
- 2 (bypass): to suppress high-frequency noise in power supply signals. Acts like small local power supply. If the main power supply suddenly temporarily drops its voltage, this capacitor can supply.
- Decoupling/bypass capacitance must provide the high frequency components of the current

Trace length vs. signal wavelength

- If trace lengths are in range of signal's wavelength, we need to consider the effects of transmission lines (ie. Traces on board) – time delays, reflections, and crosstalk.
- Two structures for trace routing on PCB: *mircostrip* and *stripline*.

Signal speed and propagation delay

- We can calculate the time it takes for signal to travel through a trace (=propagation delay). Speed calculation on a *stripline* as function of the dielectric*:*

$$v = \frac{3\times10^8 m/s}{\sqrt{\epsilon_r}}$$

- It's more complicated for microstrip, because there's more than one surrounding dielectric – the subtract under trace, the air above trace, more medium if solder mask is there…

Characteristic impedance and Impedance matching

- One important property of transmission lines is the *characteristic impedance Z_0*.
- If there's impedance changes in signal's path (signal source → trace → vias →…) reflections will happen. **Reflection coefficient**= relationship between impedance of the transmission line and impedance of the source/sink.

$$\rho = \frac{R - Z_0}{R + Z_0}$$

  For open end $\rho = 1\ (R \to \infty)$, and short end $\rho = -1\ (R \to 0)$.
- Need **impendence matching**. We want ρ = 0 so no reflections –the impedance at the source has the same value as the characteristic impedance of the transmission line.
- Proper **termination** on the receiver of signal is needed to avoid reflections.

Power Planes and Ground Planes

- Complete ground plane in high-speed design is essential. A complete power plane is also recommended. If several regulated voltages are there, best solution is for every voltage to have its own layer and its own ground plane.
- But this would result in a huge number of layers just for ground and supply voltages. Alternative may be two split the ground planes and the power planes to avoid noise coupling (usually between digital part and sensitive analog part).

Differential signals (not sure if our signals count as one)

- Make sure trace lengths are equal, propagation delay times equal, in order for EM fields to cancel each other. Route them as close as possible to make sure radiation effects them equally)

More PCB Considerations During the Circuit Design:

- Highest frequency and fastest rise time in the system?
- Electrical specifications at the inputs and outputs of the sinks and sources?
- Are there sensitive signals to route –think about controlled impedance, termination, propagation delay on a trace (clock distribution, buses…)?
- Is a microstrip adequate for the sensitive signals, or need to use stripline?
- How many different supply voltages? Does each supply voltage need its own power plane, or is it possible to split them?

- Create a diagram with the functional groups of the system – for example, transmitter path, receiver path, analog signals, digital signals, and so forth.
- Interconnections between at least two independent functional groups? Think about the return current and crosstalk to other traces.
- Clarify the minimum width, separation and height of a trace with the PCB manufacturer -- Minimum distance between two layers? What about the minimum drill and the requirements of vias? Is it possible to use blind vias and buried vias?

Equipped with this information, a designer can do a lot of basic design

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Reference guides:

1. **What Is High Speed PCB Design? An Introduction For the Complete Beginner** by Eagle Academy
2. **TI's High Speed PCB Layout Techniques** (Useful tricks and calculations to consider when designing)
3. More from TI: **High-Speed Layout Guidelines** (More things and calculations to take into considerations)
