LABORATORY 7

PHYSICS 117 Winter 2017

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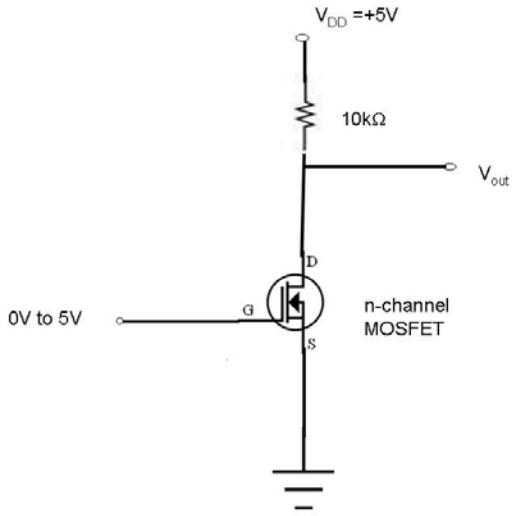
HEADS-UP: In part (a) you will be using two positive voltages. Make sure you wire up your power supply correctly.

MOSFET logic inverters

a) MOSFET switches are the basis of the CMOS digital electronics we will be using. Build the logic inverter shown below. Because the circuit has an n-channel MOSFET (in our lab IRL-510), it is called an "NMOS" inverter. A common standard is that a +5V output level is called 1 (true) and and 0V output level is called 0 (false). Plot the input vs. output voltage. HINT: having two DVM's for this measurement will make it easier. Why couldn't you just hook the drain directly to the +5V?



b) Without disassembling your NMOS inverter, build a PMOS inverter somewhere else on your breadboard using a p-channel MOSFET (in our lab IRF-9Z20PBF). Note you will have to rearrange this circuit. Hint: Remember the difference between V_{GS} and V_{SG} in class notes. Try to figure out the correct circuit without asking your TA.

c) Estimate and measure the output impedance of the NMOS inverter you built. Is it the same for 1 (true) and 0 (false)?

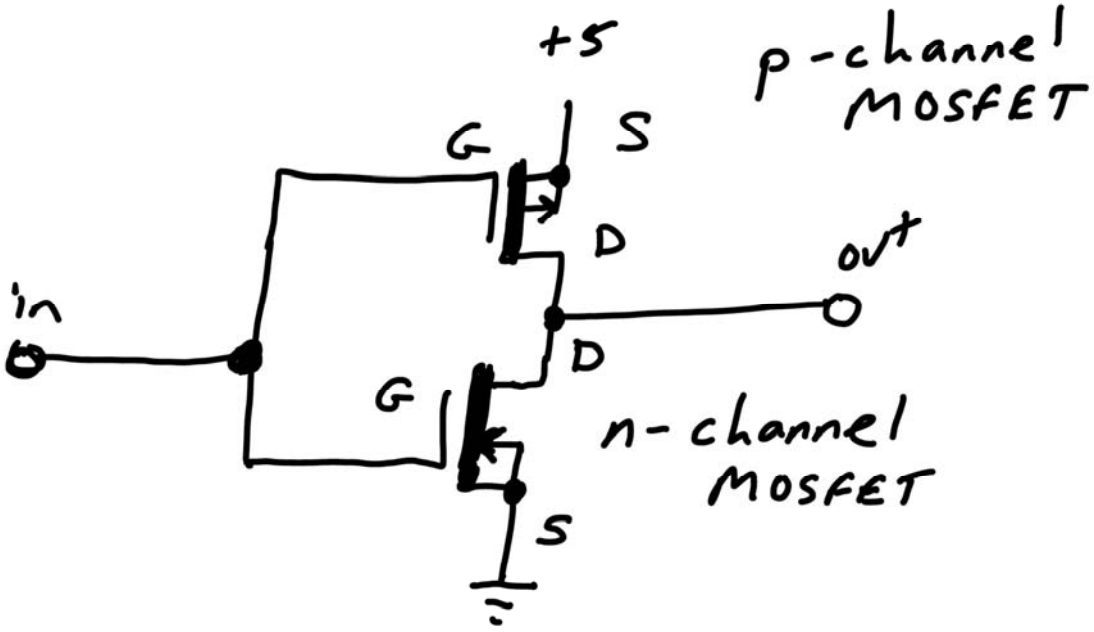
d) Set the amplitude and offset of your function generator to produce a square wave oscillating between 0 and 5V. (Remember the display will be wrong unless you set it to "high Z".) Now put this signal into the input of one of your inverters using the function generator starting at a low frequency, say 100Hz square wave and verify your circuit is inverting. How long (time) does it take your circuit to react (0 to 1? 1 to 0?) By watching the input and output on the scope, increase the frequency of the square wave to

measure the highest "baud" (bitrate) at which this inverter circuit still works. Compare to the bitrate of what you expect goes on in your home modem, computer etc.

e) Measure the risetimes and falltimes (10-90%) for the NMOS and PMOS inverters. Explain why the risetimes and falltimes are different.

f) Homemade CMOS inverter

The high output impedance of the NMOS and PMOS inverters are a pain. As you saw, even if you are driving another MOSFET next in line, the high output impedances combined with stray capacitances reduce the maximum switching speed of your circuits (due to the RC time). Also one logic state is always drawing current which wastes power. This is solved by the CMOS circuit, where C stands for "**C**omplementary". Build the CMOS-based inverter shown below:



This is known as "active pull-up".

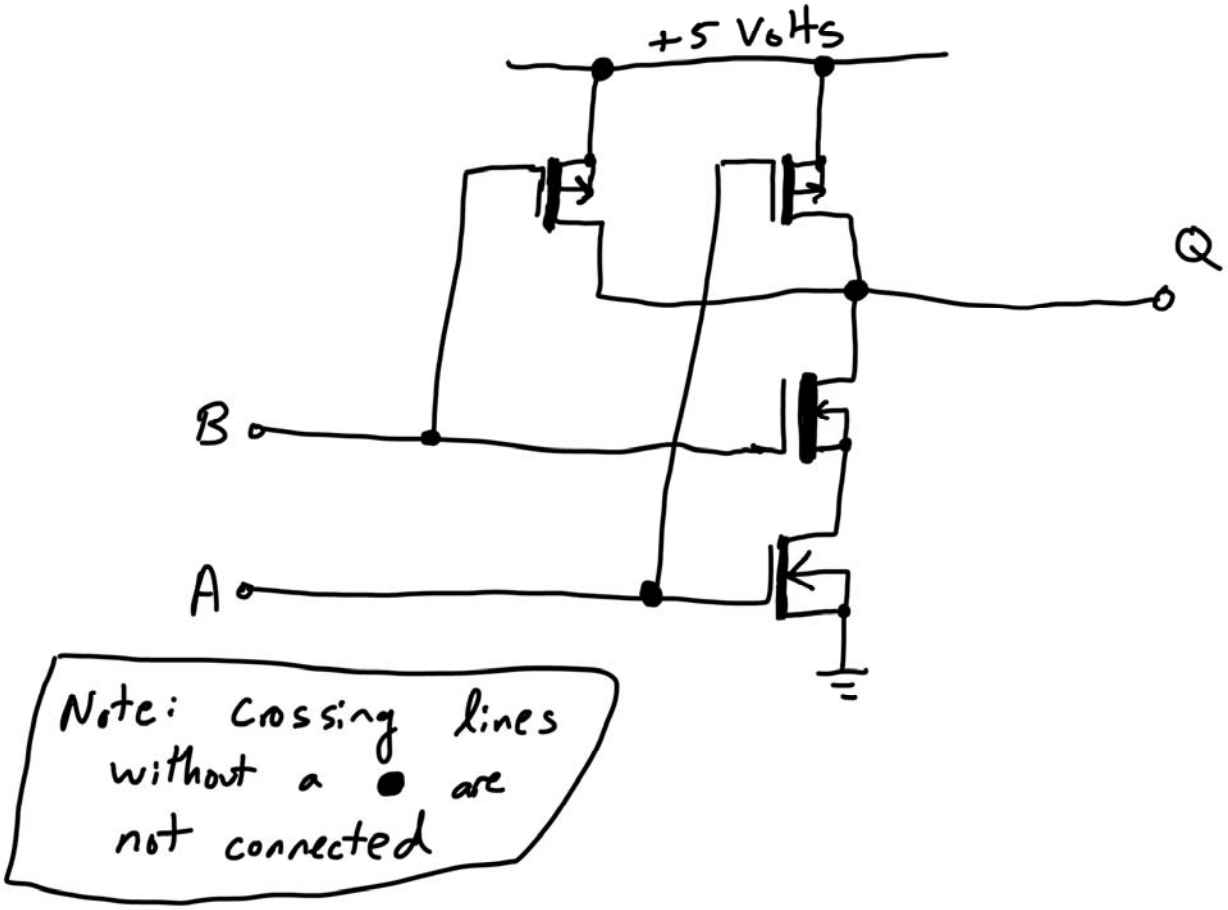
Measure the risetime and falltime of the CMOS inverter output and compare to what you got for the NMOS and PMOS inverters. Can you find the highest frequency at which this circuit still works using an input square wave?

Off-the-shelf CMOS inverter

g) Now use one of the CMOS inverters on a chip (74HCT04) located in the lab and compare its behavior to the one you built. Remember to put the unused inputs at 0 or 5V. Remember the chip needs to be powered. Because CMOS historically followed TTL, "V_{DD}" is still called V_{CC}" as if it had bipolar transistors inside. Measure the range of input voltages that correspond to 0 and 1 logic levels. (Now that you have your scope hooked up looking at square waves it is probably faster and easier to do it with your current setup rather than going back to the two DVM method from before.)

homemade NAND

h) Build your own NAND gate using CMOS logic (combined NMOS and PMOS) as shown below:



Measure the "truth table" and confirm that is a NAND. Explain in words why this circuit behaves as a NAND.

i) Commercial NAND: Wire up a NAND on a chip (74HCT00) and show it works the same way. HINT: You will need to look up its datasheet. Does it work better (faster)?

j) DeMorgan's Theorem: Use a NAND gate and Inverters to make an OR gate. HINT: You should look up "DeMorgan's Theorem" (Amazingly this was proved in the 1800's.)