In Rush Current Controller Circuit

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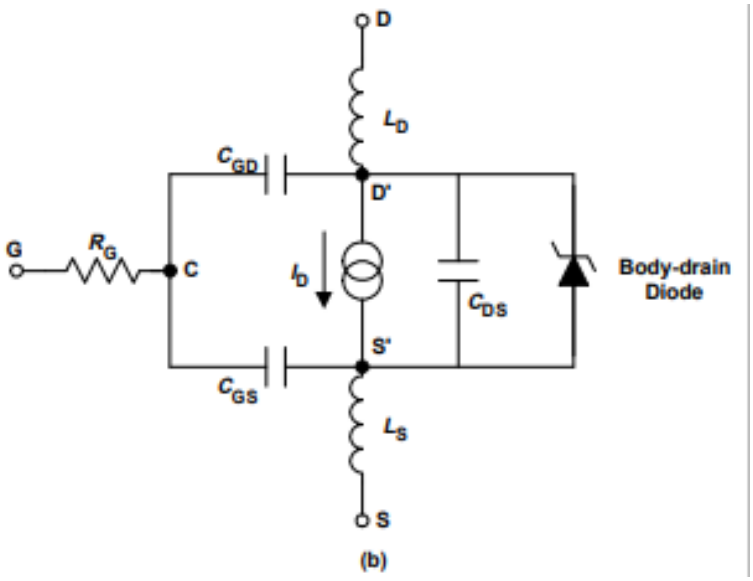
Assignment 2

1 Theory

Due to very low ESR(equivalent series resistance) of capacitor when it is supplied with a voltage, there is very high current in the circuit(ideally infinite). This surge of current can be harmful for the circuits. To limit this surge we add a MOSFET in series to the capacitor which is having dynamic resistance, so its resistance decreases from high resistance to low resistance as its turned on. So this high resistance at the starting limits the surge of current.

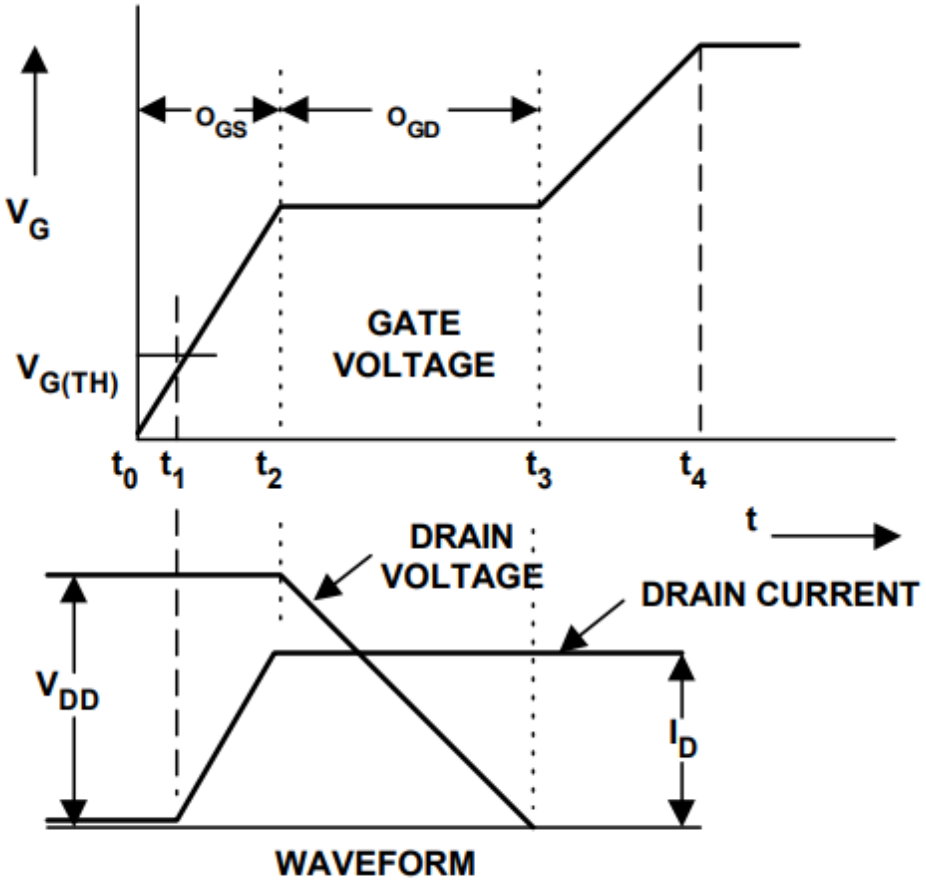
1.1 NMOS as a switch

When MOSFET is used as a switch its basic function is to control drain current by the gate voltage.
The switching performance of a device is determined by the time required to establish voltage changes across capacitances. MOSFET have gate-source capacitance, gate-drain capacitance, drain-source capacitance.
Circuit below show the capacitances



In data sheet following are mentioned:
$C_{iss} = C_{GS} + C_{GD}$, C_{DS} shorted, input capacitance
$C_{rss} = C_{GD}$
$C_{oss} = C_{DS} + C_{GD}$
Turn on time($t_{d(on)}$) is the time taken to charge input capacitance of the device.

To understand how MOSFET is switched on look at the following figure



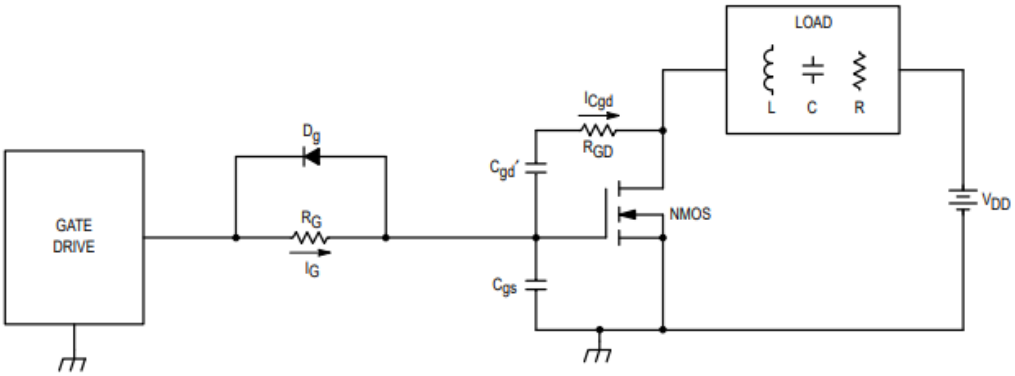
(b)

From t_0 to t_1 gate source is voltage is less than V_{th}, from t_1 gate source voltage is more than the threshold voltage so drain current rises proportionally and C_{GS} continues to charge till t_2. At t_2 C_{GS} is completely charged and drain current reaches predetermined current I_D and stays constant while drain voltage starts to falls. From t_2 C_{GD} starts to charge untill t_3. This minimum charge till t_3 that is $Q_{GS} + Q_{GD}$ is required amount of charge to turn on MOSFET.

Now designer can add Gate resistance or Capacitor parallel to parasitic capacitance so as to manipulate the time of Charging so as to achieve goals like inrush current control where we slowly charge the input capacitance so as to make transition from high resistance to low resistance so as to control initial high current.

2 Design

Following schematic is used as a reference for design



C'_{gd} is added in parallel to C_{GD} and its value is greater than C_{GD} so that C'_{gd} dominates and non-linear nature of C_{GD} is avoided.
Following design methodology is used:

1. Using following equation $i_c = C\frac{dV}{dt}$
   we can find time required to meet the inrush requirement
   $dt = C_{load}\frac{V_{DD}}{I_{inrush}}$

2. The constant $V_{plt}(V_{GS}$ between t_2 and$t_3)$ allows the input current to flow through the feedback capacitance C'_{gd} and its current is expressed as:
   $I_g = \frac{V_{GG}-V_{plt}}{R_G}$, V_{plt} can be found using
   $V_{plt} = V_{th} + I_{inrush}/g_{fmax}$
   or using datasheet.

3. Choose C'_{gd} based on following $C'_{gd} >> C_{iss}$, C_{iss} is given in data sheet.

4. Gate current required
   $I_{gd} = C'_{gd}\frac{dV_{DS}}{dt}$

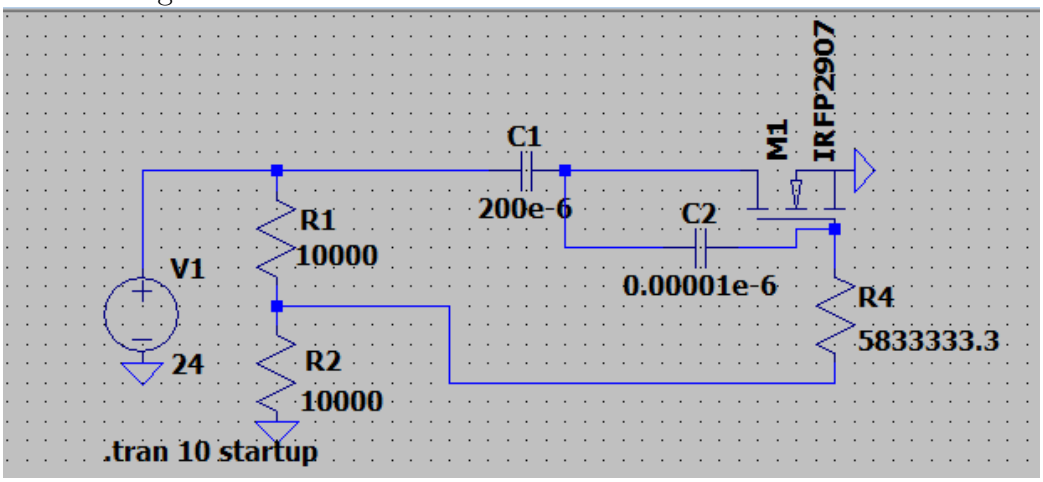
5. $I_g = \frac{V_{GG}-V_{plt}}{R_G}$ $I_{gd} = I_g I_{gd} = C'_{gd}\frac{dV_{DS}}{dt}$ Rate of change gate-drain voltage is $\frac{dV_{GD}}{dt} = \frac{I_g}{C'_{gd}} = \frac{V_{GG}-v_{plt}}{R_G C_{gd'}}$ Therefore $R_G = \frac{V_{GG}-V_{plt}}{I_g d}$

6. Choose $R_{GD} : R_G >> R_{GD}$

3 Implementation and Results

I have used IRFP2907 nmos because it is having high $Q_G = 410nC$ that is charge required to turn mosfet on, so high Q_G provide better control time to switch mosfet on. Its also have low $R_{DS} = 4.5m\Omega$ which means it do not affect circuit once switched on.

Circuit Diagram

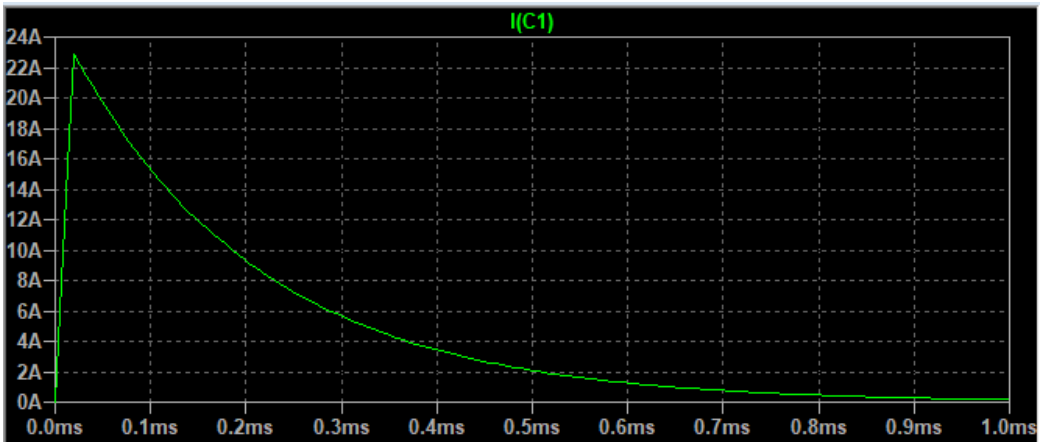


Load capacitance is of $200\mu F$ with ESR of 1Ω R_{GD} is modelled as ESR of $C'_{gd} = 0.00001\mu F$ capacitor, off course it can be added externally. $V_{GG} = 12V$ given from source of 24 V using resistive voltage divider.

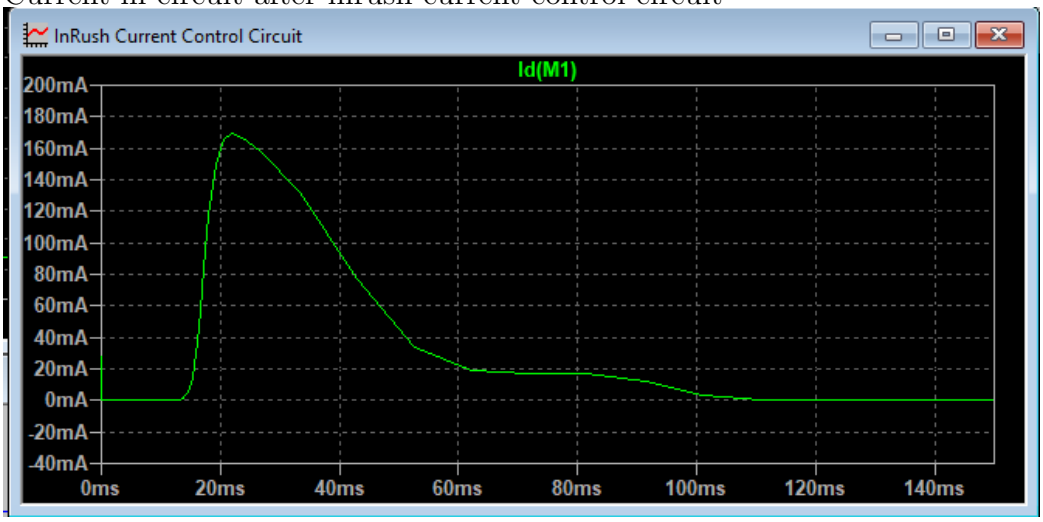
$V_{plt} = 5V$

$R_G = 5833333.3\Omega$ can be found using equation given in Design section. In practical implementation we will need to approximate this R_G with available resistances.

Current without inrush current control.

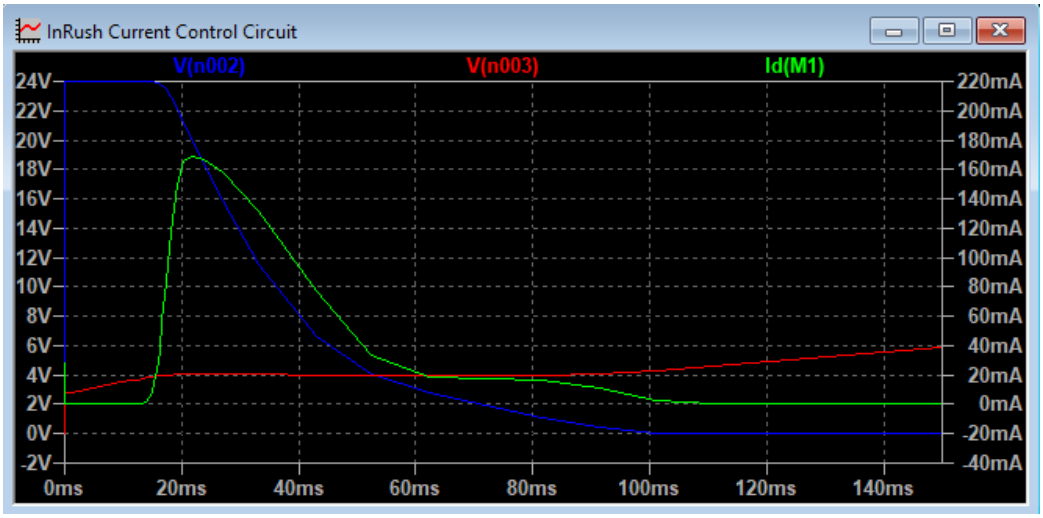


Current in circuit after inrush current control circuit



So at the cost of delay in the circuit initial current is reduced from 24A to 180 mA.

Circuit below show voltage $V_{DS} - Blue$ and $V_{GS} - Red$



These are as expected as explained in section 1.1

4 References

- Motorola AN1542
- Power MOSFET Basics