EE 671 VLSI DESIGN

Course Project - II

MACs for 2D Image Filtering (Convolution)

Group No: 23

Project report submitted by:

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Description:

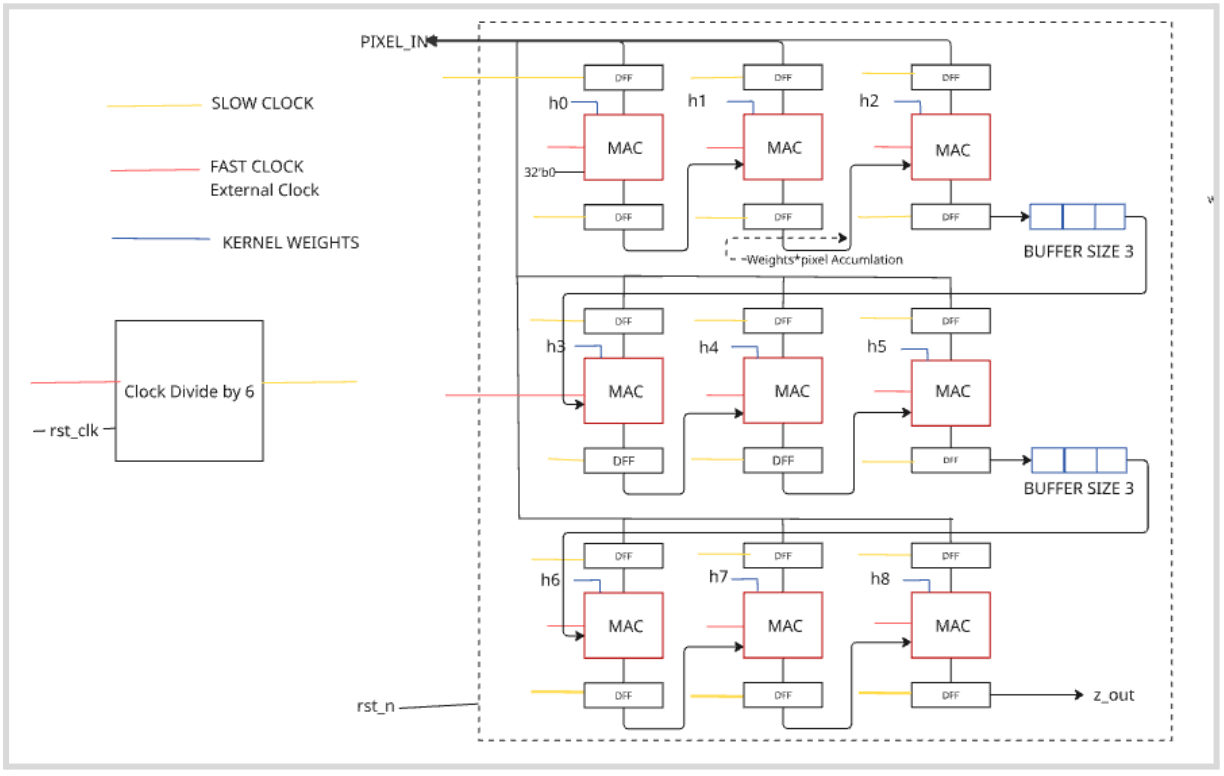
MACs for 2D Image Processing

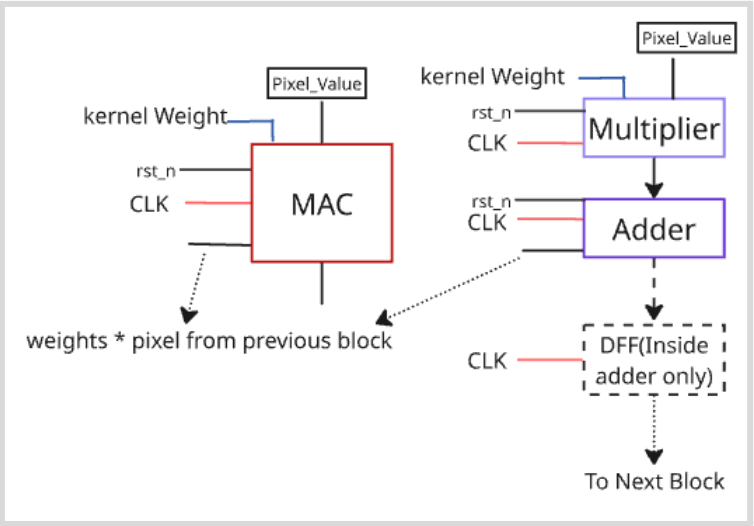
Specification:
Input: Pixel_in(Input pixel value) size 8 bits, clk - 100 MHz, rst_n, rst_clk
Output: z_out of size 32 bits, slow clock for control of input flow
Kernel size: 3 x 3

Note: Input image width should be 6.

In the project, MAC units are implemented and used to form a Kernel for the convolution operation on an image.

Architecture of Kernel :





Adder is a 32-bit Kogge Stone adder.

Multiplier:
We implemented an 8-bit × 8-bit pipelined multiplier to reduce the combinational delay between the stages of the multiplier for operation at a higher frequency.
Let's take two 8-bit numbers A and B. We decompose A×B as:

$$(A_{high} << 4 + A_{low}) (B_{high} << 4 + B_{low})$$

We computed these four partial products and then shifted them properly to align their values corresponding to the places in the final multiplication.

Pipeline Stages:
Design has three pipeline stages:

1st Stage: Break the input into a 4-bit combination, do the product, and load it into the register.

P1= (A3A2A1A0)*(B3B2B1B0)
P2=(A7A6A5A4)*(B3B2B1B0)
P3=(A3A2A1A0)*(B7B6B5B4)
P4=(A7A6A5A4)*(B7B6B5B4)
All 8 bits.

2nd Stage: Sum of P2 and P3. Shifted the P1 and P4 products.

P2+P3 = S1(9bits) and shift it 4 bits left. After the shift, there will be a total of 13 bits.
Add eight zero bits before P1. After the addition of zero bits, P1 will be 16 bits.
Shift P4 eight bits towards the left. After the shift, it will also become 16 bits.
Shift to get the magnitude of the P1, P2, P3, and P4.

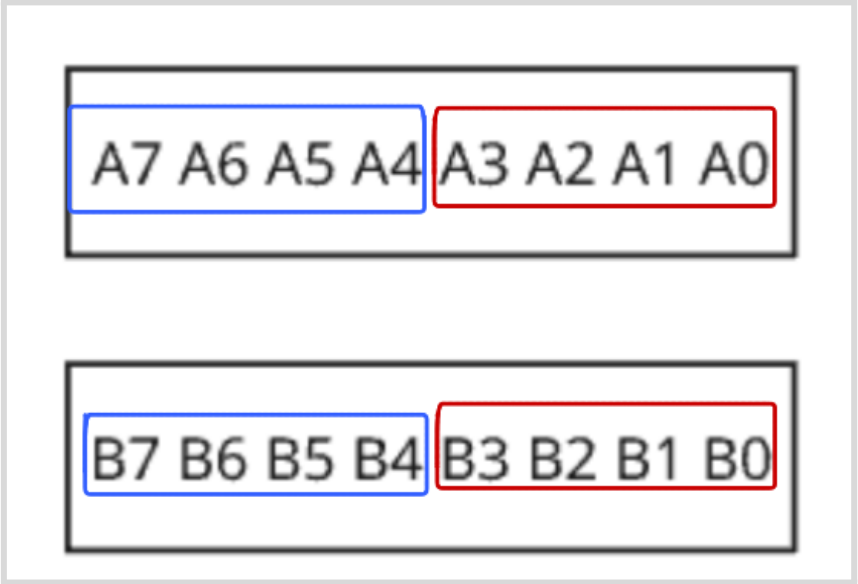
3rd Stage: Add as below to get the final product
Product = (8b'0P1)+(3b'0S14b'0)+(P48b'0)

Example:

11010011*10100110 =211*166=35026 (1000100011010010)
P1= 0011*0110=00010010 (3*6=18)
P2=1101*0110=01001110 (13*6=78)
P3=0011*1010=00011110 (3*10=30)
P4=1101*1010=10000010 (13*10=130)

S1= P2 +P3 =01001110+00011110= 01101100 (78+30=108) in 9-bits=001101100

Product = (8b'0P1)+ (3b'0S14b'0)+(P48b'0)
= 0000000000010010(18) + 0000011011000000(1728) + 1000001000000000(33280) = 1000100011010010(35206)



Working:

- Initially, we kept the rst_n and rst_clk low to initialize everything in the circuit to 0.
- After that, rst_clk followed by rst_n is set high after a few clock periods. Now the system starts to function.
- At the positive clock edge of the slow clock, which has 6 times the clock period of the fast clock, that is our external clock, the input pixel is sampled by DFF(D-Flip Flop) along with the propagation of weight*(previous pixel) from one block to another for addition with (current pixel)*weight.

Further explanation:

- At the first rising (positive) edge of the slow clock, pixel[0] is sampled.
- This pixel[0] then goes to the multiplier running on the fast clock.
- After 3 fast-clock cycles from the time the input appears, the multiplier outputs pixel[0] * h0.
- This product is then sampled by the adder, which adds it to 0 (since this is the first MAC unit and accumulation starts from 0).
- This result is sampled by DFF at the next positive edge of the slow clock.
- At this same slow-clock edge, pixel[1] is sampled by the second MAC unit.
- At this point, the second MAC has both the previous result pixel[0]*h0 and the new pixel pixel[1].
- At the next positive edge of the slow clock, pixel[0]*h0 + pixel[1]*h1 is propagated to the third MAC.
- The third MAC then generates and forwards pixel[0]*h0 + pixel[1]*h1 + pixel[2]*h2 to the buffer.
- The buffer is required because the upcoming pixels (pixel[3], pixel[4], pixel[5]) do not belong to the current convolution window and must not be accumulated with the current partial sum.
- Therefore, the accumulated value is held for 3 slow-clock cycles until the next valid window starts with pixels pixel[6], pixel[7], and pixel[8].
- The 15th z_out value represents the final convolution result corresponding to the given kernel and the image window.

In our case, Kernel weights are stored as follows:

2	1	2
1	2	1
2	1	2

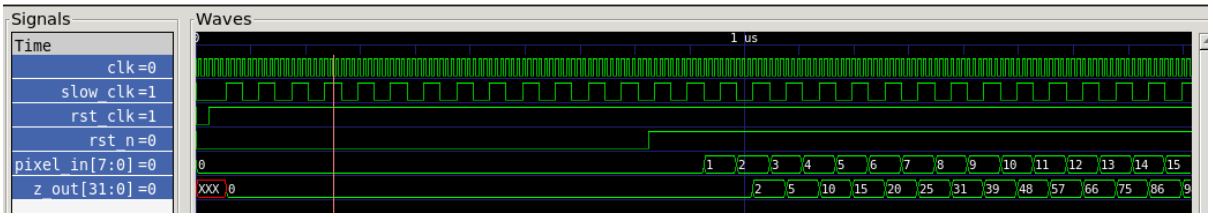
And the image from the test bench is being input as follows:

1	2	3	4	5	6
7	8	9	10	11	12
13	14	15	16	17	18
19	20	21	22	23	24
25	26	27	28	29	30
31	32	33	34	35	36

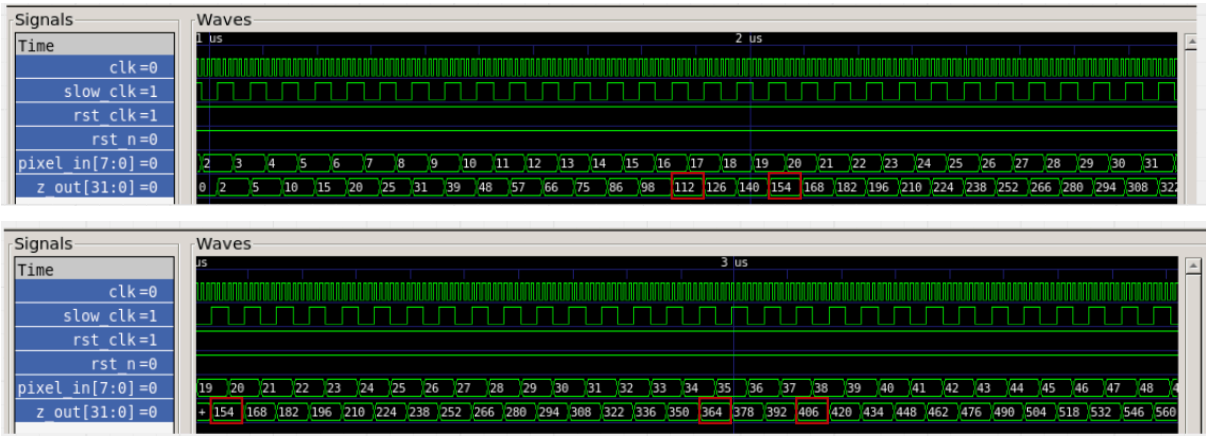
So first actual result of convolution between image and kernel in z_out will be the 15th z_out value, and the second result will be the 18th value of z_out, and then again, since the kernel changes to another set of rows again, the result will be at the 15th value from the last convoluted value, and then again at the 18th.
Expected results at 15th and 18th z_out value are
At 15th : (2 + 2 + 6 + 7 + 16 + 9 + 26 + 14 + 30) = 112
At 18th : (8 + 5 + 12 + 10 + 22 + 12 + 32 + 17 + 36) = 154
These values are highlighted on the simulation screenshots provided below.
Similarly, at the next 15th and 18th values from the last correct z_out will be 364 and 406, respectively.

Pre-Synthesis Simulation

Initial Setup

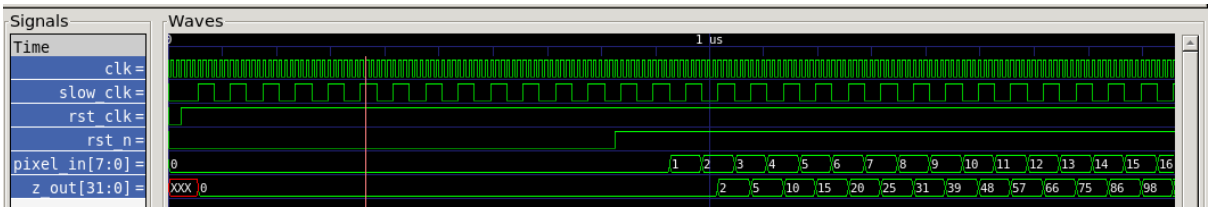


Convolution highlighted Result

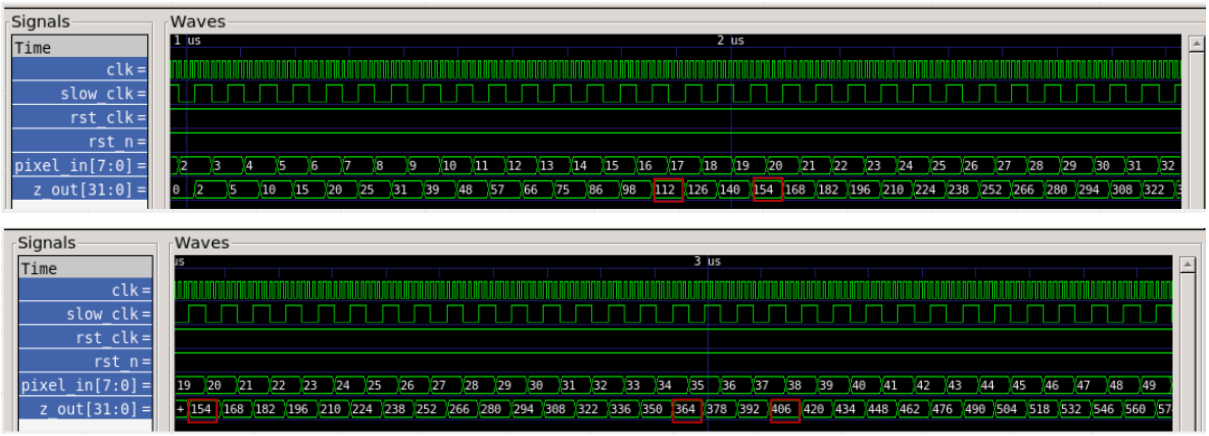


Post Synthesis Simulation

Initial Setup

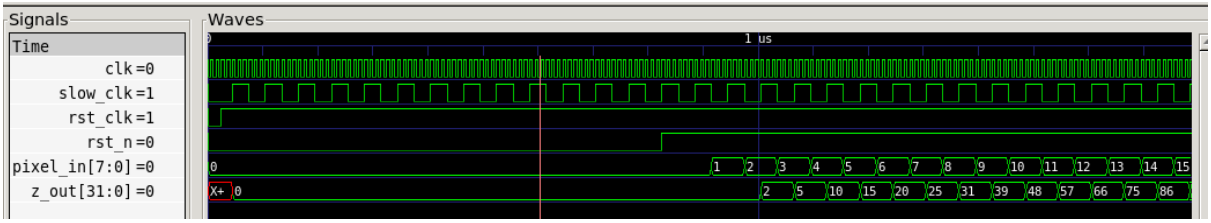


Convolution highlighted Result



Post Physical Design Simulation

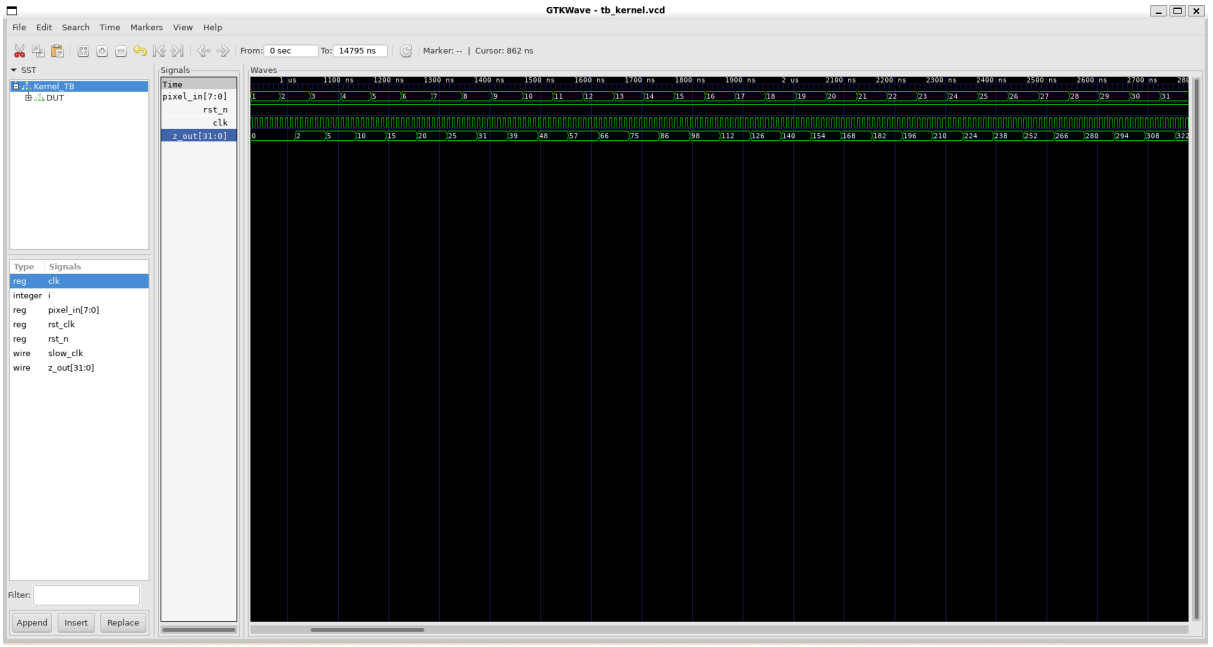
Initial setup



Result Highlighted Screenshot

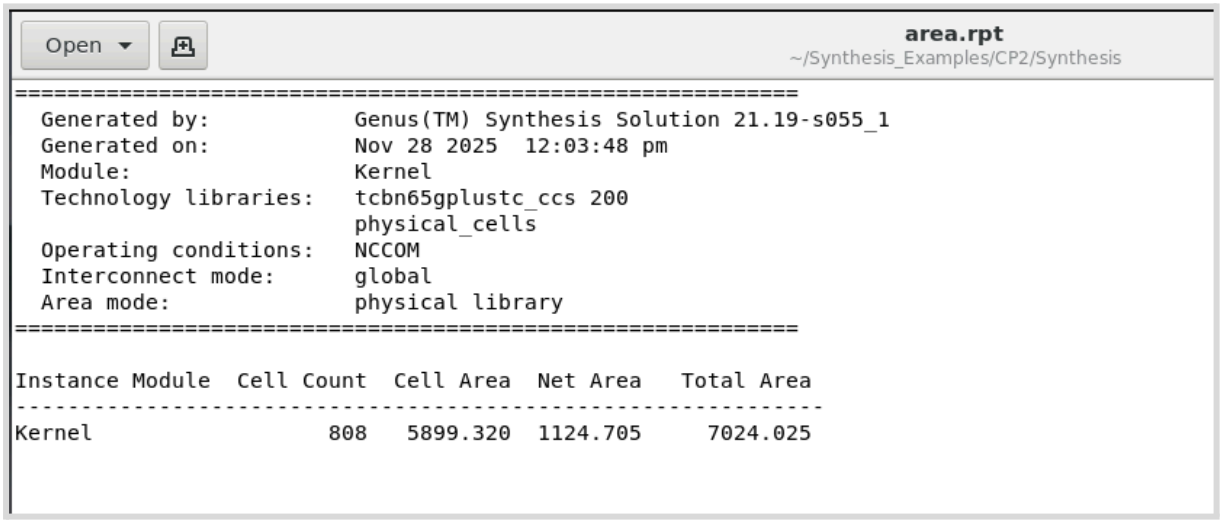
Note: Here, screen screenshots of gtkwave are the same as above. So, for understanding purposes, refer above.

Screenshot of the gtkwave waveforms (pre-synthesis)



Screenshot of the various reports after synthesis

Area report




```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.19-s055_1
  Generated on:           Nov 28 2025  12:03:48 pm
  Module:                 Kernel
  Technology libraries:   tcbn65gplustc_ccs 200
                          physical_cells
  Operating conditions:   NCCOM
  Interconnect mode:      global
  Area mode:              physical library
============================================================

Instance Module  Cell Count  Cell Area  Net Area   Total Area
------------------------------------------------------------
Kernel                 808   5899.320  1124.705     7024.025
```

Timing report

Open

timing.rpt
~/Synthesis_Examples/CP2/Synthesis

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.19-s055_1
  Generated on:           Nov 28 2025  12:03:48 pm
  Module:                 Kernel
  Technology libraries:   tcbn65gplustc_ccs 200
                          physical_cells
  Operating conditions:   NCCOM
  Interconnect mode:      global
  Area mode:              physical library
============================================================

              Pin                          Type     Fanout Load Slew Delay Arrival
                                                          (fF) (ps)  (ps)   (ps)
-------------------------------------------------------------------------------------
(clock clk)                                launch                                0 R
M8_original_u_adder_b_reg_reg[0]/CP                                 0    +0       0 R
M8_original_u_adder_b_reg_reg[0]/Q         DFCNQD1       1  4.5   34   +93      93 R
g3920__1617/B                                                             +0      93
g3920__1617/CO                             HA1D0         1  2.8   40   +53     146 R
g3827__9945/CI                                                            +0     146
g3827__9945/CO                             FA1D0         1  2.8   41   +64     210 R
g3781__5115/CI                                                            +0     210
g3781__5115/CO                             FA1D0         1  2.8   41   +64     273 R
g3757__5122/CI                                                            +0     273
g3757__5122/CO                             FA1D0         1  2.8   41   +64     337 R
g3728__6783/CI                                                            +0     337
g3728__6783/CO                             FA1D0         1  2.8   41   +64     401 R
g3706__5107/CI                                                            +0     401
g3706__5107/CO                             FA1D0         1  2.8   41   +64     465 R
g3682__7410/CI                                                            +0     465
g3682__7410/CO                             FA1D0         1  2.8   41   +64     529 R
g3661__9945/CI                                                            +0     529
g3661__9945/CO                             FA1D0         1  4.5   58   +74     603 R
g3651__4733/B                                                             +0     603
g3651__4733/CO                             HA1D0         1  4.5   58   +67     670 R
g3641__5115/B                                                             +0     670
g3641__5115/CO                             HA1D0         1  4.5   58   +67     737 R
g3632__7098/B                                                             +0     737
g3632__7098/CO                             HA1D0         1  4.5   58   +67     804 R
g3620__1705/B                                                             +0     804
g3620__1705/CO                             HA1D0         1  4.5   58   +67     870 R

g3610__1617/B                                                             +0     870
g3610__1617/CO                             HA1D0         1  4.5   58   +67     937 R
g3603__6783/B                                                             +0     937
g3603__6783/CO                             HA1D0         1  4.5   58   +67    1004 R
g3596__8428/B                                                             +0    1004
g3596__8428/S                              HA1D0         1  2.7   38   +70    1074 R
M8_original_u_adder_sum_reg[14]/D   <<<    DFCNQD1                     +0    1074
M8_original_u_adder_sum_reg[14]/CP         setup                        0   +24    1098 R
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock clk)                                capture                           10000 R
-------------------------------------------------------------------------------------
Cost Group   : 'clk' (path_group 'clk')
Timing slack :    8902ps
Start-point  : M8_original_u_adder_b_reg_reg[0]/CP
End-point    : M8_original_u_adder_sum_reg[14]/D
```

Music

Power report

Open

power.rpt
~/Synthesis_Examples/CP2/Synthesis

```
Instance: /Kernel
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ------------------------------------------------------------------------
       memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
     register     2.40884e-05  5.40610e-04  8.58522e-06  5.73283e-04  91.72%
        latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        logic     4.87989e-06  1.13296e-05  4.66415e-06  2.08736e-05   3.34%
         bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        clock     0.00000e+00  0.00000e+00  3.08700e-05  3.08700e-05   4.94%
          pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
           pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------
    Subtotal     2.89683e-05  5.51939e-04  4.41194e-05  6.25027e-04 100.00%
  Percentage           4.63%       88.31%        7.06%      100.00% 100.00%
  ------------------------------------------------------------------------
```

Gates report

Open

gates.rpt
~/Synthesis_Examples/CP2/Synthesis

```
  Generated by:           Genus(TM) Synthesis Solution 21.19-s055_1
  Generated on:           Nov 28 2025  12:03:48 pm
  Module:                 Kernel
  Technology libraries:   tcbn65gplustc_ccs 200
                          physical_cells
  Operating conditions:   NCCOM
  Interconnect mode:      global
  Area mode:              physical library
==========================================================


  Gate    Instances    Area          Library
-----------------------------------------------------
AN3XD1            1     2.520    tcbn65gplustc_ccs
AO22D0           11    31.680    tcbn65gplustc_ccs
CKXOR2D1         11    39.600    tcbn65gplustc_ccs
DFCND1            1     8.640    tcbn65gplustc_ccs
DFCNQD1         270  2138.400    tcbn65gplustc_ccs
DFKCNQD1        414  2980.800    tcbn65gplustc_ccs
EDFCND1           2    22.320    tcbn65gplustc_ccs
FA1D0            44   396.000    tcbn65gplustc_ccs
HA1D0            41   236.160    tcbn65gplustc_ccs
INR2XD0           1     2.160    tcbn65gplustc_ccs
NR2XD0            1     1.440    tcbn65gplustc_ccs
XOR2D1           11    39.600    tcbn65gplustc_ccs
-----------------------------------------------------
total           808  5899.320


     Type      Instances   Area   Area %
------------------------------------------
sequential           687 5150.160   87.3
logic                121  749.160   12.7
physical_cells         0    0.000    0.0
------------------------------------------
total                808 5899.320  100.0
```

Plain

Summary report

Open

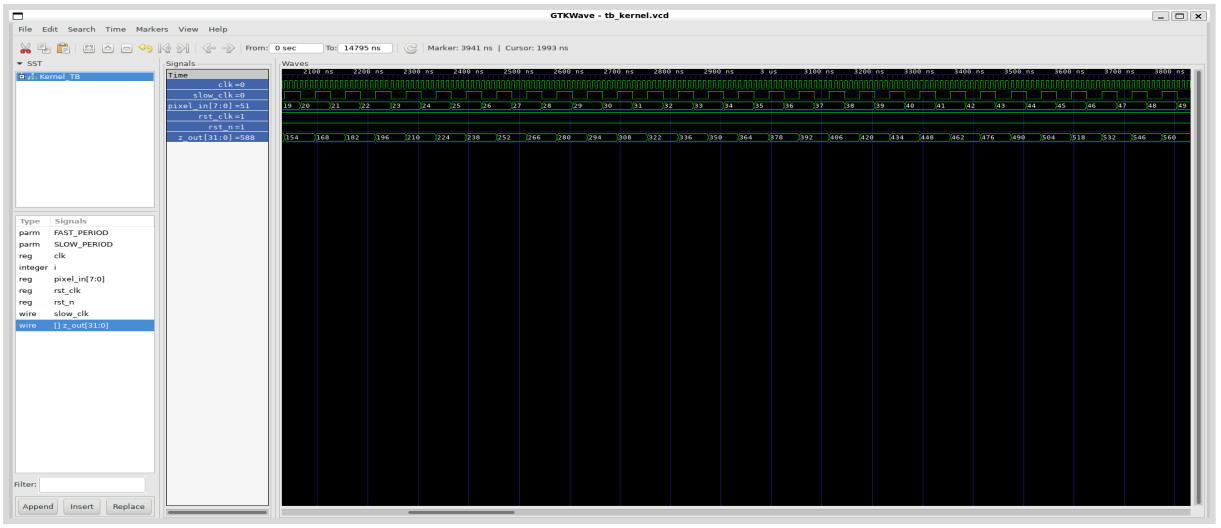
summary.rpt
~/Synthesis_Examples/CP2/Synthesis

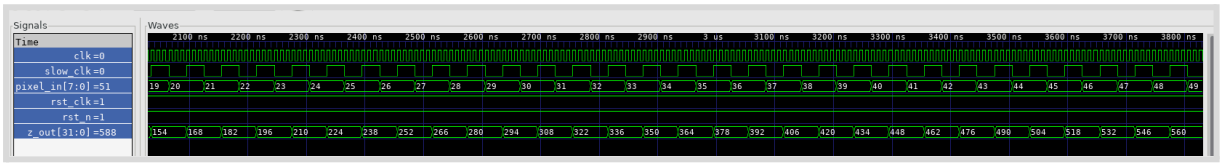
```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.19-s055_1
  Generated on:           Nov 28 2025  12:03:48 pm
  Module:                 Kernel
  Technology libraries:   tcbn65gplustc_ccs 200
                          physical_cells
  Operating conditions:   NCCOM
  Interconnect mode:      global
  Area mode:              physical library
============================================================

        Timing
        ------

 Slack               Endpoint             Cost Group
------------------------------------------------------------
+8902ps M8_original_u_adder_sum_reg[14]/D clk


        Area
        ----

Instance Module  Cell Count  Cell Area  Net Area   Total Area
-------------------------------------------------------------
Kernel                  808   5899.320  1124.705     7024.025

        Design Rule Check
        -----------------

Max_transition design rule: no violations.

Max_capacitance design rule: no violations.
```

The following table is based on the above gate.rpt file:

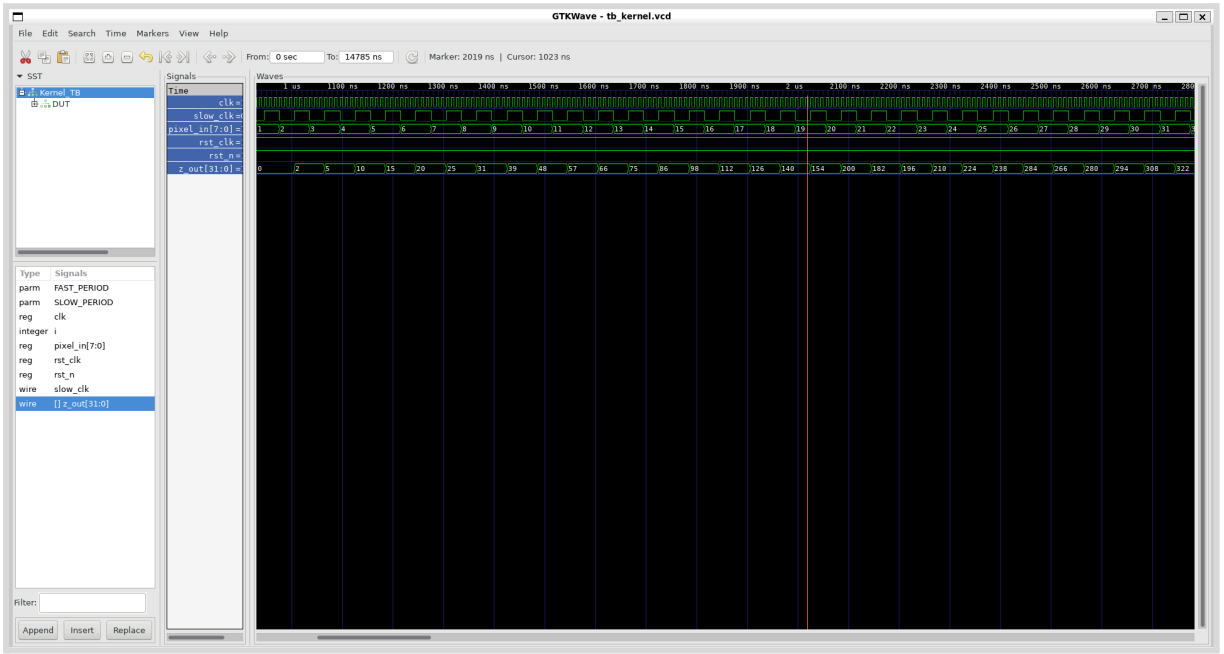
Number of combinational cells	121
Number of sequential cells (Flip-flops)	687
Total number of cells	808

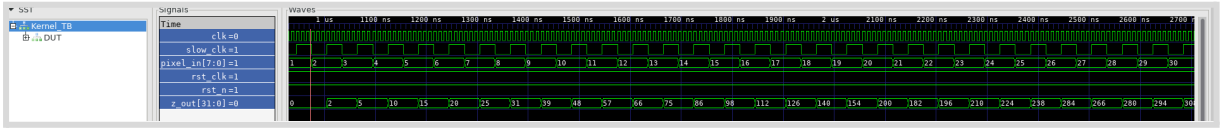
Screenshot of the gtkwave waveforms (post-synthesis)





Physical Design
Post Route gtkwave





Post route reports:

Area report:

Open ▾ area.rpt
~/PnR_Example/9.Kernel/physical_design

Hinst Name	Module Name	Inst Count	Total Area
Kernel		850	6001.920

Hold report:

Kernel_postRoute_hold.summary - /home/running_courses/EE671/EE671_24/PnR_Example/9.Kernel/timingReports/

File Edit Search Preferences Shell Macro Windows

```
#####################################################################
#  Generated by:      Cadence Innovus 21.12-s106_1
#  OS:                Linux x86_64(Host ID vlsi73.ee.iitb.ac.in)
#  Generated on:      Fri Nov 28 11:10:24 2025
#  Design:            Kernel
#  Command:           timeDesign -postRoute -hold
#####################################################################

------------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.004  |  0.004  |  0.012  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   730   |   289   |   441   |
+--------------------+---------+---------+---------+

Density: 100.000%
------------------------------------------------------------------
```

Timing report:

Kernel_postRoute.summary - /home/running_courses/EE671/EE671_24/PnR_Example/9.Kernel/timingReports/

File Edit Search Preferences Shell Macro Windows

```
#####################################################################
#  Generated by:      Cadence Innovus 21.12-s106_1
#  OS:                Linux x86_64(Host ID vlsi73.ee.iitb.ac.in)
#  Generated on:      Fri Nov 28 11:10:21 2025
#  Design:            Kernel
#  Command:           timeDesign -postRoute
#####################################################################

------------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  8.422  |  8.422  |  9.294  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   730   |   289   |   441   |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+-------------------+
|                |              Real             |       Total       |
|    DRVs        +---------------+---------------+-------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+---------------+---------------+-------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+---------------+---------------+-------------------+

Density: 100.000%
------------------------------------------------------------------
```

Power Report

power.rpt - /home/running_courses/EE671/EE671_24/PnR_Example/9.Kernel/physical_design/

File Edit Search Preferences Shell Macro Windows Help

```
 1 *----------------------------------------------------------------------------------------
 2 *       Innovus 21.12-s106_1 (64bit) 12/08/2021 18:19 (Linux 3.10.0-693.el7.x86_64)
 3 *
 4 *
 5 *       Date & Time:    2025-Nov-28 11:10:25 (2025-Nov-28 05:40:25 GMT)
 6 *
 7 *----------------------------------------------------------------------------------------
 8 *
 9 *       Design: Kernel
10 *
11 *       Liberty Libraries used:
12 *             BEST_CASE:
  /vlsi/pdk/course_pdk_2025/tsmc_gp_65_stdio/tcbn65gplus_200a/TSMCHOME/digital/Front_End/timing_power_noise/CCS/tcbn65gplus_200a/tcbn65gplusbc_ccs.lib
13 *
14 *       Power Domain used:
15 *             Rail:        VDD      Voltage:      1.1
16 *
17 *       Power View : BEST_CASE
18 *
19 *       User-Defined Activity : N.A.
20 *
21 *       Activity File: N.A.
22 *
23 *       Hierarchical Global Activity: N.A.
24 *
25 *       Global Activity: N.A.
26 *
27 *       Sequential Element Activity: 0.200000
28 *
29 *       Primary Input Activity: 0.200000
30 *
31 *       Default icg ratio: N.A.
32 *
33 *       Global Comb ClockGate Ratio: N.A.
34 *
35 *       Power Units = 1mW
36 *
37 *       Time Units = 1e-09 secs
38 *
39 *       report_power -outfile physical_design/power.rpt
40 *
41 ----------------------------------------------------------------------------------------
42
43
44 Total Power
45 ----------------------------------------------------------------------------------------
46 Total Internal Power:        0.86662250            72.5712%
```

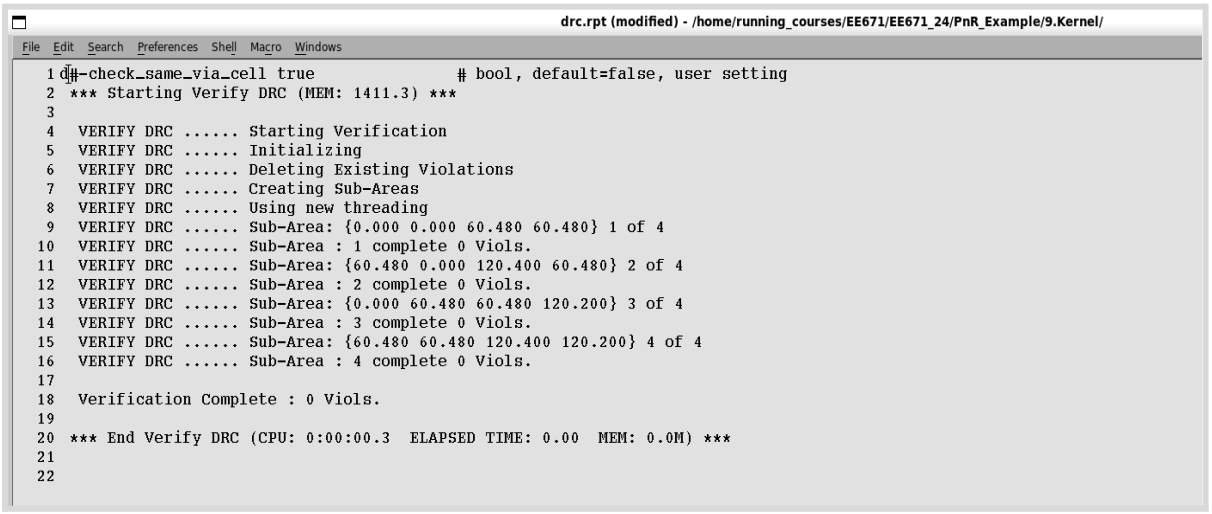
power.rpt - /home/running_courses/EE671/EE671_24/PnR_Example/9.Kernel/physical_design/

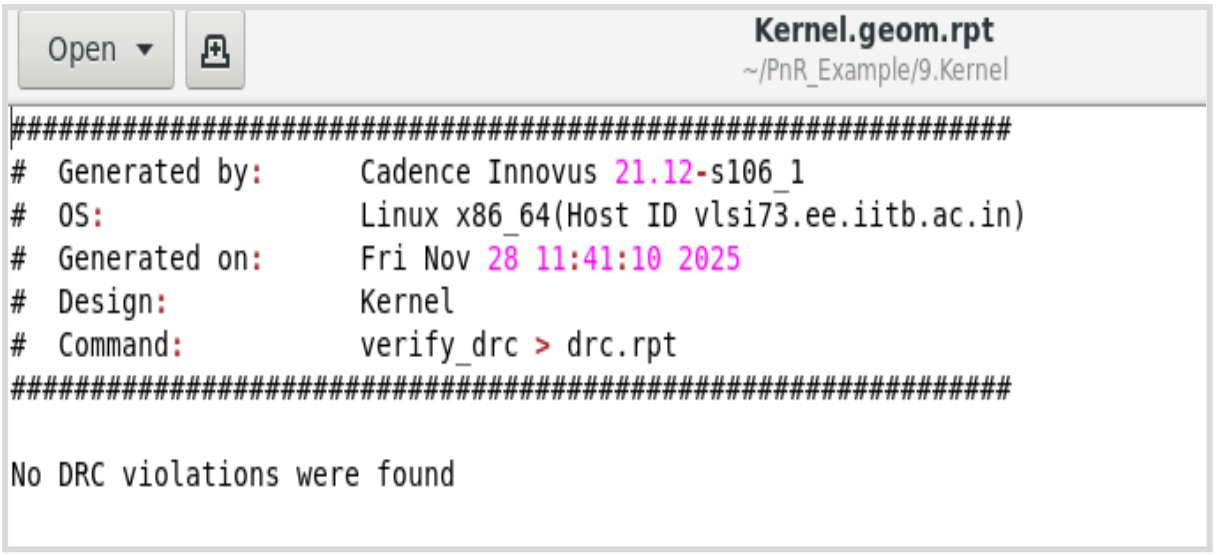
File Edit Search Preferences Shell Macro Windows Help

```
43
44 Total Power
45 ----------------------------------------------------------------------------------------
46 Total Internal Power:        0.86662250            72.5712%
47 Total Switching Power:       0.10563899             8.8462%
48 Total Leakage Power:         0.22190761            18.5826%
49 Total Power:                 1.19416911
50 ----------------------------------------------------------------------------------------
51
52
53 Group                           Internal   Switching     Leakage       Total  Percentage
54                                 Power      Power         Power         Power  (%)
55 ----------------------------------------------------------------------------------------
56 Sequential                        0.8077     0.01411      0.1156      0.9374        78.5
57 Macro                                  0          0           0           0           0
58 IO                                     0          0    7.44e-05    7.44e-05     0.00623
59 Physical-Only                          0          0     0.07719     0.07719       6.464
60 Combinational                    0.03323     0.02668     0.02604     0.08595       7.198
61 Clock (Combinational)             0.0257     0.06484    0.003022     0.09357       7.835
62 Clock (Sequential)                     0          0           0           0           0
63 ----------------------------------------------------------------------------------------
64 Total                             0.8666      0.1056      0.2219       1.194         100
65 ----------------------------------------------------------------------------------------
66
67
68 Rail                  Voltage   Internal   Switching     Leakage       Total  Percentage
69                                 Power      Power         Power         Power  (%)
70 ----------------------------------------------------------------------------------------
71 VDD                       1.1     0.8666      0.1056      0.2219       1.194         100
72
73
74 Clock                           Internal   Switching     Leakage       Total  Percentage
75                                 Power      Power         Power         Power  (%)
76 ----------------------------------------------------------------------------------------
77 clk                               0.0257     0.06484    0.003022     0.09357       7.835
78 ----------------------------------------------------------------------------------------
79 Total (excluding duplicates)      0.0257     0.06484    0.003022     0.09357       7.835
80 ----------------------------------------------------------------------------------------
81 Clock: clk
82 Clock Period: 0.010000 usec
83 Clock Toggle Rate:   200.0000 Mhz
84 Clock Static Probability:  0.5000
85
86
87
88 ----------------------------------------------------------------------------------------
89 *       Power Distribution Summary:
90 *               Highest Average Power:       CTS_ccl_a_buf_00001 (CKBD16):          0.01918
91 *               Highest Leakage Power:       CTS_ccl_a_buf_00005 (CKBD16):        0.0006045
92 *          Total Cap:      3.70842e-12 F
93 *          Total instances in design:  1365
94 *          Total instances in design with no power:     0
95 *          Total instances in design with no activity:     0
96 *          Total Fillers and Decap:   515
97 ----------------------------------------------------------------------------------------
98
99
```

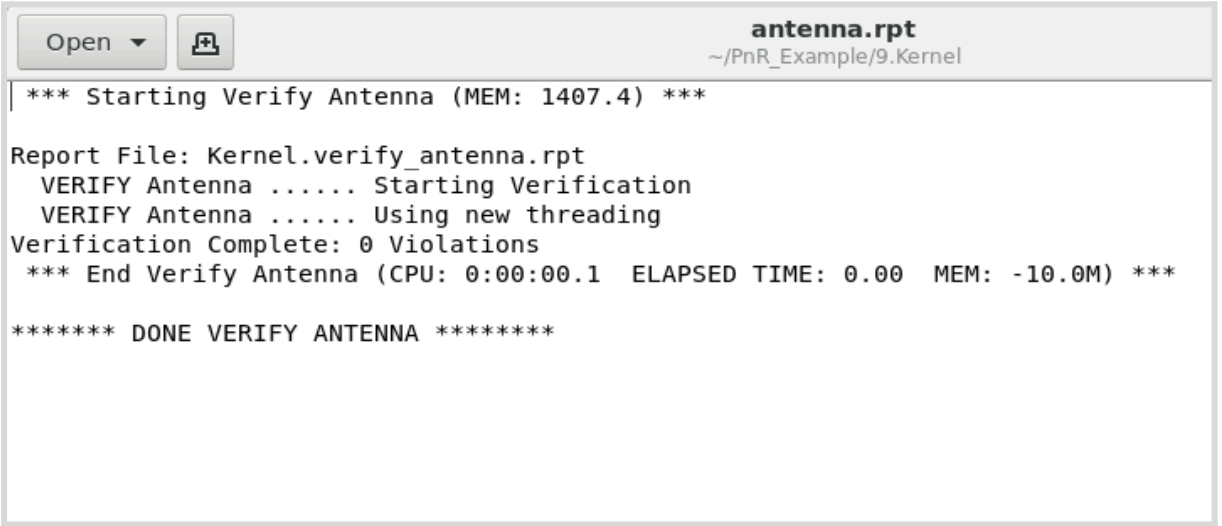
Physical Verification

DRC report:





Antenna report:



Open

Kernel.antenna.rpt
~/PnR_Example/9.Kernel

```
#####################################################################
#  Generated by:      Cadence Innovus 21.12-s106_1
#  OS:                Linux x86_64(Host ID vlsi73.ee.iitb.ac.in)
#  Generated on:      Fri Nov 28 11:36:10 2025
#  Design:            Kernel
#  Command:           saveModel -sdf -spef -dir Kernel_hier_data
#####################################################################

No Violations Found
```

Connectivity report:

connectivity.rpt - /home/running_courses/EE671/EE671_24/PnR_Example/9.Kernel/

File Edit Search Preferences Shell Macro Windows

```
1 VERIFY_CONNECTIVITY use new engine.
2
3 ******** Start: VERIFY CONNECTIVITY ********
4 Start Time: Fri Nov 28 11:42:17 2025
5
6 Design Name: Kernel
7 Database Units: 2000
8 Design Boundary: (0.0000, 0.0000) (120.4000, 120.2000)
9 Error Limit = 1000; Warning Limit = 50
10 Check all nets
11
12 Begin Summary
13   Found no problems or warnings.
14 End Summary
15
16 End Time: Fri Nov 28 11:42:17 2025
17 Time Elapsed: 0:00:00.0
18
19 ******** End: VERIFY CONNECTIVITY ********
20   Verification Complete : 0 Viols.  0 Wrngs.
21   (CPU Time: 0:00:00.1  MEM: 0.000M)
22
23
```

Open

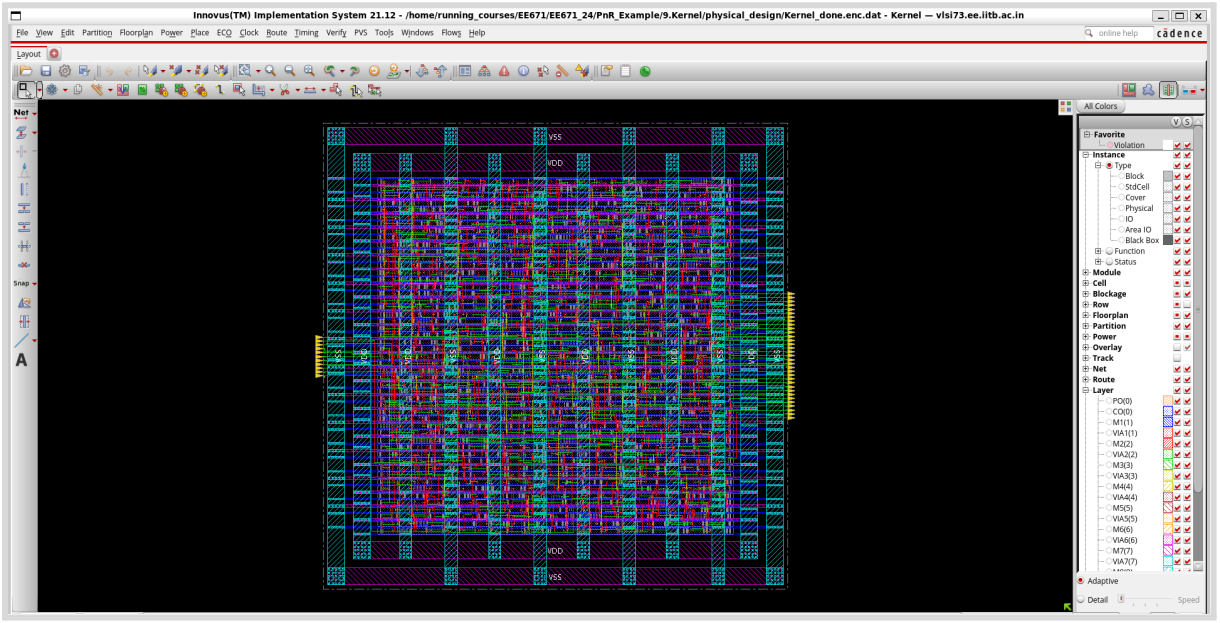
Kernel.conn.rpt
~/PnR_Example/9.Kernel

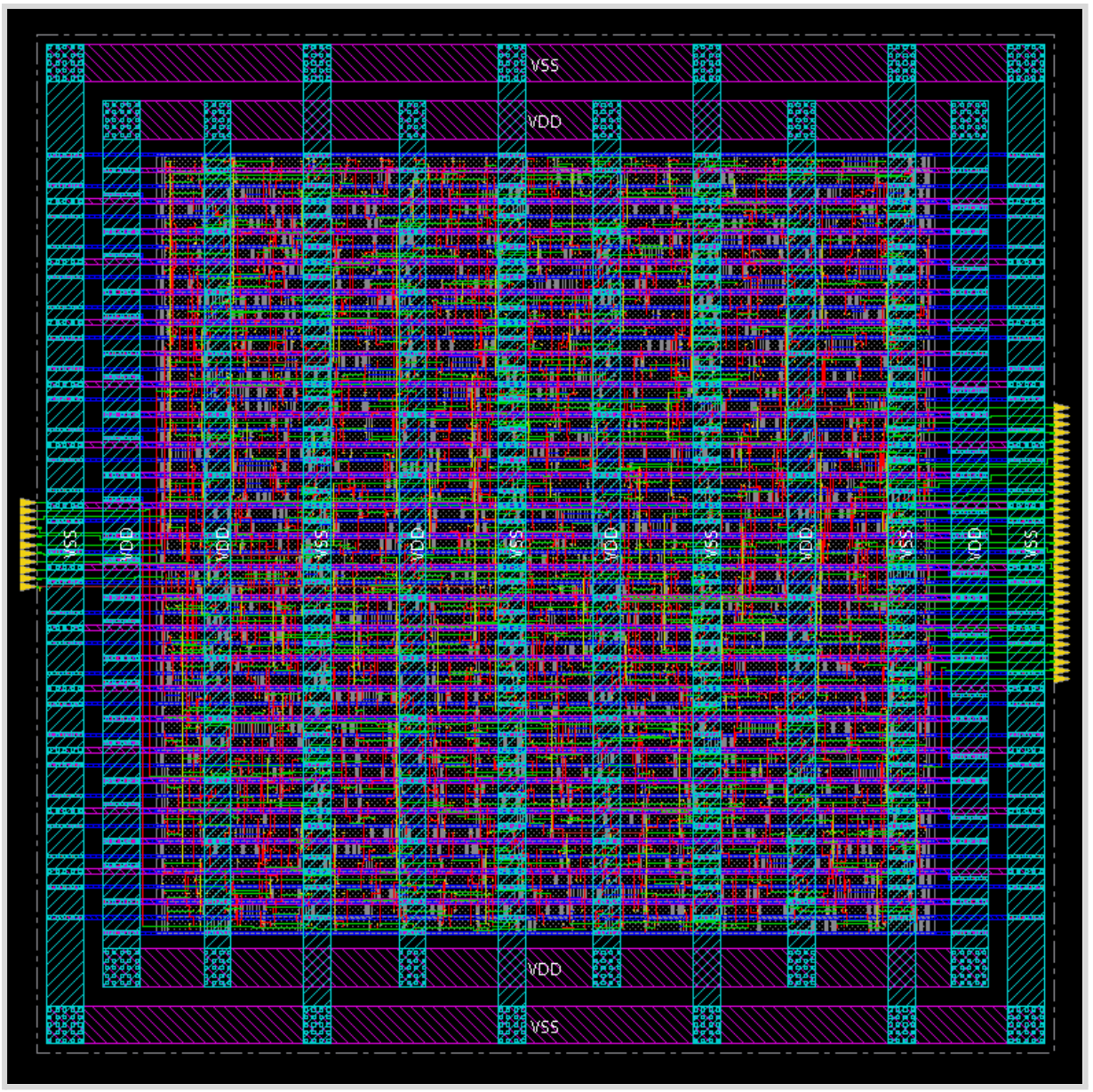
```
#####################################################################
#  Generated by:      Cadence Innovus 21.12-s106_1
#  OS:                Linux x86_64(Host ID vlsi73.ee.iitb.ac.in)
#  Generated on:      Fri Nov 28 11:42:17 2025
#  Design:            Kernel
#  Command:           verifyConnectivity > connectivity.rpt
#####################################################################
Verify Connectivity Report is created on Fri Nov 28 11:42:17 2025



Begin Summary
    Found no problems or warnings.
End Summary
```

Table containing post route timing, area, and power reports:

Clock Frequency (MHz)	100
Worst case setup slack [WNS in the report] (ns)	8.422
Worst case hold slack [WNS in the report] (ns)	0.004
Design area (μm^2)	6001.920
Power Consumption (Sequential Only) (μW)	937.4
Power Consumption (Combinational Only) (μW)	77.19
Total Power Consumption (Internal Only) (μW)	866.6225
Total Power Consumption (Switching Only) (μW)	105.6390
Total Power Consumption (Leakage Only) (μW)	221.9076
Total Power Consumption (μW)	1194.1691

Screenshot of the final Layout:




VSS
VDD
VSS
VDD
VDD
VSS
VDD
VSS
VDD
VSS
VDD
VSS
VDD
VSS
VDD
VSS

Contribution Table

Name and Roll No.	Contribution
Ankit Raj, 25M1269	Implemented the pipelined multiplier as well as did the part from verilog to synthesis of the module.
Ayush Singh, 25M1239	Implemented the part from Synthesis to physical design of the module. Log files and screenshots of the results.
Harsh Gupta, 25M1237	Implemented the complete datapath except for the multiplier block. This includes the full 32-bit Kogge Stone adder, the MAC and modified-MAC modules, the slow-clock divider, and the entire Kernel architecture.
Shubham, 25M1277	Implemented testbench for the Kernel module that includes clock generation, reset signals, pixel inputs, and waveform generation. Written report that includes description, working, waveform comparison, screenshots, and results obtained.