

Risultati test

Tests executed on FPGA **xc7k160tfbv484-2**

Index	Nome	Descrizione	Tipo (Syn o Impl)	Vitis Directives	LUT	FF	Latency(Avg- Max-Min)	Target Clock(ns)	Max Target Clock reachable (ns)
a	Reference	Test from ascon-hardware repo(VHDL post implementation)	impl	x	1459	666	x	10	fixed to 10
b	Standard Version	debloat of unusefull ports(our baseline)	syn	x	9213	3654	118-188-52	15	15
b			impl	x	4590	3438	x	10	8.5
c.1	Standard Version	Permutations.h directives	syn	INLINE recursive on P6, P8, P12	42969	5229	124-206-53	10	3
c.1			impl	""""	11361	4984	x	10	7.5
c.2			syn	""""	43265	12473	233-419-85	3	3
c.2			impl	""""	13252	10393	x	3	2.9
d	Standard Version	ROUND.h directives	syn	PIPELINE on ROR function	11492	3420	144-229-65	13	13
d			impl	""""	3701	3147	x	10	8.4
e	Pipelined permutations	Permutations are pipelined so P8->P6 and P12->P8	syn	x	9213	3420	118-188-52	15	15

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e			impl	x	4590	3438	x	10	8.5
f	Standard version	Round.h directives	syn	DATAFLOW on ROUND function	9908	7302	384-618-185	13.5	13.5
f			impl	""""	6352	7174	x	10	6.4
g.1	Standard version	Permutations.h directives	syn	DATAFLOW on P6, P8, P12	50401	18665	150-248-68	10	3
g.1			impl	""""	23375	21029	x	10	7.9
g.2	Standard version	Permutations.h directives	syn	DATAFLOW on P6, P8, P12	50823	22821	275-486-107	3	3
g.2			impl	""""	23375	21029	x	3	7.9
h.1	Standard version	Permutations.h directives	syn	PIPELINE on P6, P8, P12	43052	6671	127-205-55	10	3
h.1			impl	""""	11507	6399	x	10	7.4
h.2	Standard version	Permutations.h directives	syn	PIPELINE on P6, P8, P12	43723	19057	227-482-108	3	3
h.2			impl	""""	11507	6399	x	3	7.4
i.1	Standard version	Permutations.h directives	syn	PIPELINE and INLINE recursive on P6, P8, P12	43081	6219	127-197-53	10	3

Index	Nome	Descrizione	Tipo (Syn o Impl)	Vitis Directives	LUT	FF	Latency(Avg- Max-Min)	Target Clock(ns)	Max Target Clock reachable (ns)
i.1			impl	""	11407	5947	x	10	9
i.2	Standard version	Permutations.h directives	syn	PIPELINE and INLINE recursive on P6, P8, P12	43504	13903	235-415-86	3	3
i.2			impl	""	11407	5947	x	3	9