results.MD 17/5/2022

Risultati test

Tests executed on FPGA xc7k160tfbv484-2

Nome	Descrizione	Tipo (Syn o Impl)	Vitis Directives	LUT	FF	Latency(Avg- Max-Min)	Target Clock(ns)	Max Target Clock reachable (ns)
Reference	Test from ascon-hardware repo(VHDL post implementation)	impl	х	1459	666	х	10	fixed to 10
Standard Version	debloat of unusefull ports(our baseline)	syn	х	9213	3654	118-188-52	15	15
		impl	х	4590	3438	Х	10	8.5
Standard Version	Permutations.h directives	syn	INLINE recoursive on P6, P8, P12	42969	5229	124-206-53	10	3
		impl	11111	11361	4984	Х	10	7.5
		syn	11111	43265	12473	233-419-85	3	3
		impl	"""	13252	10393	Х	3	2.9
Standard Version	ROUND.h directives	syn	PIPELINE on ROR function	11492	3420	144-229-65	13	13
		impl	11111	3701	3147	Х	10	8.4
Pipelined permutations	Permutations are pipelined so P8->P6 and P12->P8	syn	х	9213	3420	118-188-52	15	15
	Reference Standard Version Standard Version Standard Version Pipelined	Reference Test from ascon-hardware repo(VHDL post implementation) Standard debloat of unusefull ports(our baseline) Standard Version Permutations.h directives Standard Version ROUND.h directives	Nome Descrizione (Syn o Impl) Test from ascon-hardware repo(VHDL post implementation) Standard debloat of unusefull ports(our baseline) Standard Version Permutations.h directives syn impl Standard Version Fermutations.h directives syn impl Standard Version Permutations are pipelined so syn Pipelined Permutations are pipelined so	Nome Descrizione (Syn o Impl) Vitis Directives Reference Test from ascon-hardware repo(VHDL post implementation) impl x Standard Version debloat of unusefull ports(our baseline) syn x Standard Version Permutations.h directives syn INLINE recoursive on P6, P8, P12 Impl """ syn """" Standard Version ROUND.h directives syn PIPELINE on ROR function Pipelined Permutations are pipelined so syn x	NomeDescrizione(Syn o Impl)Vitis DirectivesLUTReferenceTest from ascon-hardware repo(VHDL post implementation)implx1459Standard Versiondebloat of unusefull ports(our baseline)synx9213Standard VersionPermutations.h directivessynINLINE recoursive on P6, P8, P1242969Standard Versionsynimpl"""11361LUTsyn"""43265Standard Versionsyn"""43265Standard VersionROUND.h directivessynPIPELINE on ROR function11492Pipelined VersionPermutations are pipelined so permutationssynx9213	NomeDescrizione(Syn o Impl)Vitis DirectivesLUTFFReferenceTest from ascon-hardware repo(VHDL post implementation)implx1459666Standard Versiondebloat of unusefull ports(our baseline)synx92133654Standard VersionPermutations.h directivesimplx45903438Standard VersionPermutations.h directivessynINLINE recoursive on P6, P8, P125229Impl"""113614984Syn"""4326512473Standard VersionROUND.h directivessynPIPELINE on ROR function114923420Standard VersionROUND.h directivessynPIPELINE on ROR function37013147Pipelined Pipelined by P8->P6 and P12->P8synx92133420	Nome Descrizione (Syn o Impl) Vitis Directives Implementatives LUT FF Latency(Avg-Max-Min) Reference Test from ascon-hardware repo(VHDL post implementation) impl x 1459 666 x Standard Version debloat of unusefull ports(our baseline) syn x 9213 3654 118-188-52 Standard Version Permutations.h directives syn INLINE recoursive on P6, P8, P12 42969 5229 124-206-53 Standard Version Permutations.h directives syn """" 11361 4984 x Standard Version ROUND.h directives syn PIPELINE on ROR function 11492 3420 144-229-65 Version Permutations are pipelined so syn x 9213 3420 118-188-52	Nome Descrizione (Syn o Impl) Vitis Directives Inpl LUT FF Latency(Avg-Max-Min) Target Clock(ns) Reference Test from ascon-hardware repo(VHDL post implementation) impl x 1459 666 x 10 Standard Version debloat of unusefull ports(our baseline) syn x 4590 3438 x 10 Standard Version Permutations.h directives syn INLINE recoursive on P6, P8, P12 42969 5229 124-206-53 10 Standard Version syn """ 43265 12473 233-419-85 3 Syn """ 43265 12473 233-419-85 3 Standard Version ROUND.h directives syn PIPELINE on ROR function 11492 3420 144-229-65 13 Pipelined Permutations are pipelined so syn x 9213 3420 118-188-52 15

Index	Nome	Descrizione	Tipo (Syn o Impl)	Vitis Directives	LUT	FF	Latency(Avg- Max-Min)	Target Clock(ns)	Max Target Clock reachable (ns)
е			impl	х	4590	3438	Х	10	8.5
f	Standard version	Round.h directives	syn	DATAFLOW on ROUND function	9908	7302	384-618-185	13.5	13.5
f			impl	11111	6352	7174	Х	10	6.4
g.1	Standard version	Permutations.h directives	syn	DATAFLOW on P6, P8, P12	50401	18665	150-248-68	10	3
g.1			impl	11111	23375	21029	Х	10	7.9
g.2	Standard version	Permutations.h directives	syn	DATAFLOW on P6, P8, P12	50823	22821	275-486-107	3	3
g.2			impl	11111	23375	21029	Х	3	7.9
h.1	Standard version	Permutations.h directives	syn	PIPELINE on P6, P8, P12	43052	6671	127-205-55	10	3
h.1			impl	11111	11507	6399	Х	10	7.4
h.2	Standard version	Permutations.h directives	syn	PIPELINE on P6, P8, P12	43723	19057	227-482-108	3	3
h.2			impl	11111	11507	6399	Х	3	7.4
i.1	Standard version	Permutations.h directives	syn	PIPELINE and INLINE recoursive on P6, P8, P12	43081	6219	127-197-53	10	3

Index	Nome	Descrizione	Tipo (Syn o Impl)	Vitis Directives	LUT	FF	Latency(Avg- Max-Min)	Target Clock(ns)	Max Target Clock reachable (ns)
i.1			impl	11111	11407	5947	Х	10	9
i.2	Standard version	Permutations.h directives	syn	PIPELINE and INLINE recoursive on P6, P8, P12	43504	13903	235-415-86	3	3
i.2			impl	11111	11407	5947	Х	3	9