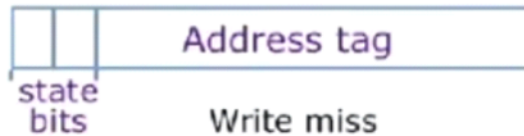


Cache State Transition Diagram

The MSI protocol

Each cache line has state bits



M: Modified

S: Shared

I: Invalid

