Enrollment No. _____

ADIT/GCET/MBIT
(CONSTITUENT INSTITUTION OF CVMU)
BE – SEMESTER – 6th INTERNAL EXAMINATION – FEB 2023-24

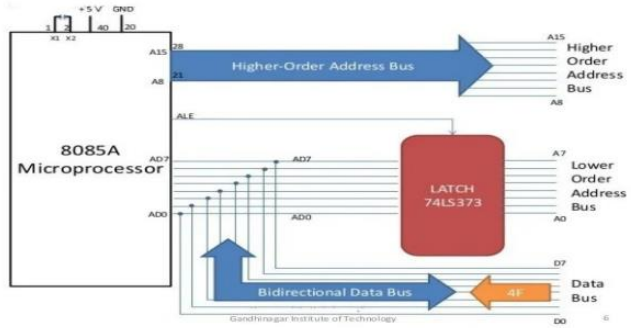
MICROPROCESSOR TECHNOLOGIES (102045610)

Date: 07/2/2024	Time: 10.30 am to 11.45am	Maximum Marks: 40

Instructions:

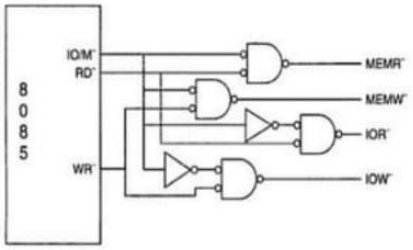
1. Figures on the right indicate full marks.
2. Make the suitable assumption if required, do specify the same.

Q. 1	**(A)**	**Answer the Following. (Each question carries one mark).**	**[08]**
	(i)	List the four operations commonly performed by the 8085 microprocessor. Microprocessor Initiated operations: Memory read, Memory writes, I/O read and I/O write Internal Data Operation Peripheral and externally initiated operations	
	(ii)	For each pin show whether it is an input line or an output line to microprocessor: ALE, HLDA ALE, HLDA: Output line (MP to Peripheral)	
	(iii)	How many T –states are required for LXI instruction? 10 T-states	
	(iv)	What is the use of READY pin of 8085? to delay the microprocessor until the slow responding peripheral is ready to send or accept the data.	
	(v)	Which flag is/are not affected by executing INR instruction. Carry flag	
	(vi)	Specify the crystal frequency required for the 8085-system having time period of one T-state is 3.72 μs. =2/3.72micr sec = 0.53763 MHz= 537.63 KHz	
	(vii)	Define the machine cycle and instruction cycle. Machine Cycle: The time required to complete one operation of accessing memory, I/O, or acknowledging an external request. • This cycle may consist of 3 to 6 T-states. Instruction Cycle: The time required to complete the execution of an instruction.	
	(viii)	List the different addressing modes of 8085. Register, Immediate, Direct and Indirect	
Q-2	**(A)**	Explain how address/data lines AD0-AD7 are de-multiplexed. Draw the logic diagram to generate control signals MEMW', MEMR', IOW' and IOR'. ALE signal is used to demultiplex the lower order address bus (AD0 – AD7). ALE is high Multiplex Add/Data Bus work as Address Bus ALE is low Multiplex Add/Data Bus work as Data Bus ----------(1)	**[05]**



----------(2)

Generation of Control signal



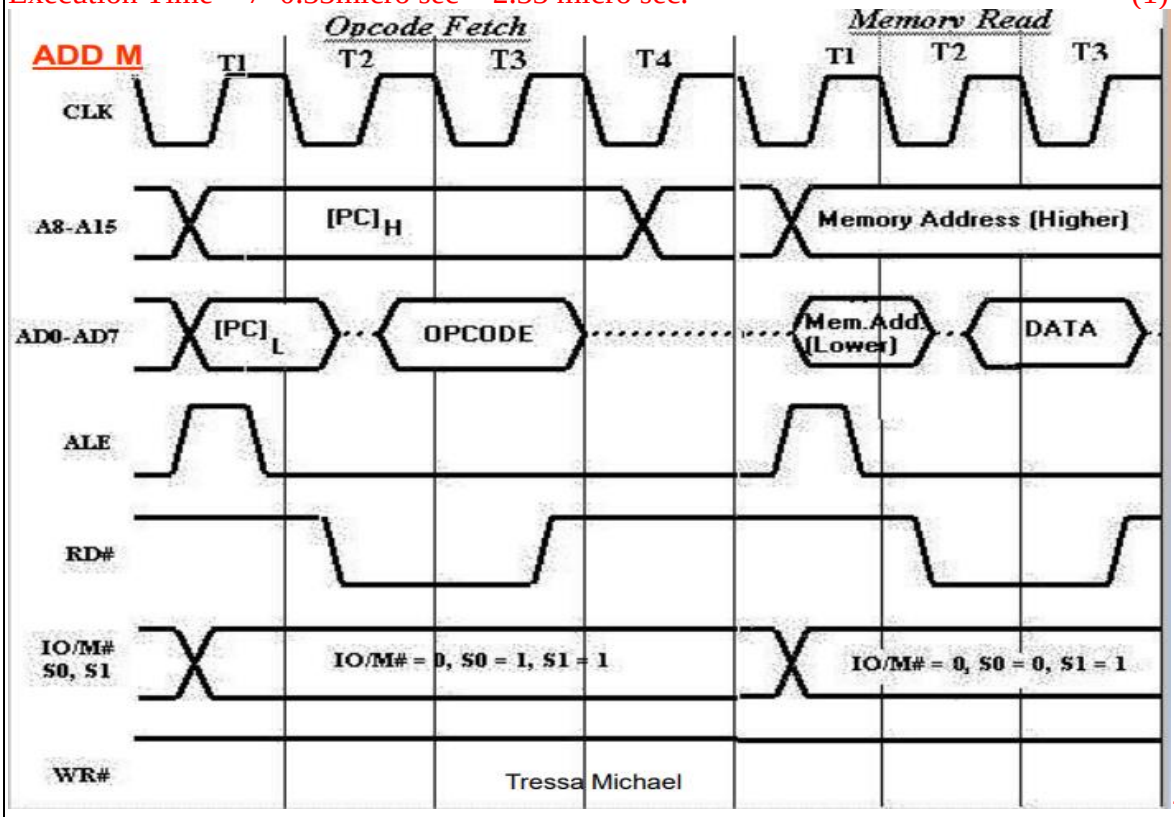
----------(2)

(B) Draw the timing diagram of an instruction ADD M written on memory location 2050H. Also calculate the execution time required for the same. (Hex code of ADD M is 86H and content in memory 2050H is 12H). **[05]**

Machine cycle: 2 (Opcode fetch, Memory write)

T-states : 4+3=7

Execution Time = 7*0.33micro sec = 2.33 micro sec. ----------(1)



-(4)

Q-3 (A) **1.** Explain the following instructions with number of machine cycle and T state. **[04]**

(i) CMC (ii) *INR* M

CMC: Complement Carry

Opcode	Operand	Bytes	M-Cycles	T-States	Hex Co
CMC	None	1	1	4	3F

Description The Carry flag is complemented.

Flags The Carry flag is modified, no other flags are affected.

INR: Increment Contents of Register/Memory by 1

Opcode	Operand	Bytes	M-Cycles	T-States
INR	Reg.	1	1	4
	Mem.	1	3	10

Reg.	Hex
B	04
C	0C
D	14
E	1C
H	24
L	2C
M	34
A	3C

Description The contents of the designated register/memory are incremented by 1 and the results are stored in the same place. If the operand is a memory location, it is specified by the contents of HL register pair.

2.. Define the instruction XCHG with example and show the content of register/memory locations before and after execution of instruction. **[02]**

XCHG: Exchange H and L with D and E

Opcode	Operand	Bytes	M-Cycles	T-States	Hex Code
XCHG	None	1	1	4	EB

Description The contents of register H are exchanged with the contents of register D, and the contents of register L are exchanged with the contents of register E.

Flags No flags are affected.

(B) Identify the bytes from the following set that will be displayed at memory location 3000H, assuming one byte is loaded into accumulator at a time. Data(H): 58, 32, 7A, 87, F2, D7 **[04]**

```
MVI A, Data        Loop: SUB A
MVI b,64H                STA 3000H
MVI C, C8H               HLT
JC Loop
CMP C
JNC Loop
STA 3000H
HLT
```

The data bytes display on 3000H memory location are: 00, 00, 7A, 87, 00, 00

(C) An array of 10 data bytes is stored from memory location 2000H onwards. Write an ALP for 8085 to find the maximum value from the given array and store that on 3000H. **[06]**

```
MVI A, 00H
MVI B, 00H          ; NO TO BE COMPARED IS STORED IN REGISTER B
                    ; AS WE WANT TO FIND OUT MAXIMUM NUMBER WE
                          ; WOULD COMPARE WITH 00H
    MVI C, 0AH            ; INITIALIZE COUNTER FOR LOOP
    LXI H, 2000H          ; ARRAY POINTER

ABC: MOV A, M  ; LOAD A BY THE CONTENT OF MEMORY LOCATION
                          ;POINTED BY HL REGISTER PAIR
    CMP B
    JC PQR
    MOV B, A
```

```
PQR: INX H          ; INCREMENT HL REGISTER PAIR
     DCR C          ; DECREMENT REGISTER C
     JNZ ABC        ; CONDITION USED TO COME OUT OF THE LOOP

     MOV A, B
     STA 3000H

     HLT            ; HALT THE PROGRAM
```

INPUT ARRAY:	OUTPUT ARRAY:
2000H: 01H	3000H: 0AH
2001H: 02H	
2002H: 03H	
2003H: 04H	
2004H: 05H	
2005H: 06H	
2006H: 07H	
2007H: 08H	
2008H: 09H	
2009H: 0AH	

OR

(C) An array of 10 data bytes is stored from memory location 2000H. Write an assembly language program for 8085 to reverse a given array on same location without using another array. **[06]**

```
MVI H, 00H          ; TEMP. REGISTER
    MVI L, 05H      ; COUNTER
    LXI B, 2000     ; POINTER TO FORWARD ARRAY
    LXI D, 2009     ; POINTER TO REVERSE ARRAY

ABC: LDAX B
     MOV H, A
     LDAX D
     STAX B
     MOV A, H
     STAX D

     INX B          ; INCREMENT FORWARD ARRAY
     DCX D          ; DECREMENT REVERSE ARRAY
     DCR L          ; DECREMENT COUNTER
     JNZ ABC        ; CONDITION TO COME OUT OF THE LOOP

     HLT            ; HALT THE PROGRAM
```

LOGIC TO REVERSE THE ARRAY WITHOUT USING ANOTHER ARRAY

INPUT ARRAY:	OUTPUT ARRAY:
2000H: 01H	2000H: 0AH
2001H: 02H	2001H: 09H
2002H: 03H	2002H: 08H
2003H: 04H	2003H: 07H
2004H: 05H	2004H: 06H
2005H: 06H	2005H: 05H
2006H: 07H	2004H: 04H
2007H: 08H	2003H: 03H
2008H: 09H	2002H: 02H
2009H: 0AH	2001H: 01H

Q-4	**(A)**	Design a memory interfacing circuit to meet following specification: 1. Use 74LS138 decoder. 2. 2732 (4K X 8) EPROM- address range should begin at 0000H, and additional 4K memory space should reserve for future expansion. 3. 6116(2K X 8) CMOS R/W-next to EPROM.	**[06]**
		OR	
	(A)	Design and draw the complete circuit for interfacing memories with the 8085 microprocessor which contains an EPROM (2K x 8) starting from 0000*h* and a RAM (2K x 8) staring from 7000*h*. Use a suitable decoder for selecting the chips.	**[06]**

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