S32K142EVB-Q100

CUSTOMER EVB

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Revisions									
Rev	Description	Designer	Date	Approved					
X1	Draft	J.Sanchez							
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3 Different test points used in design:

IFV:

 $\begin{array}{lll} \text{TPVx} & \text{-} & \text{Through Hole Pad} \\ \text{small} & \end{array}$

1____ TPH

TPHx - Through Hile Pad Large (for standard 0.1" header). Also used on IO Matrix (IOMx)

₫-| TP

TPX - Surface Mount Wire Loop

Notes:

- All components and board processes are to be ROHS compliant
- All connectors and headers are denoted Jx/Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2.
- 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.

User notes are given throughtout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS



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