

DISEÑO CON HARDWARE RECONFIGURABLE

Hortensia Mecha López

Departamento de Arquitectura de Computadores y Automática

Universidad Complutense de Madrid

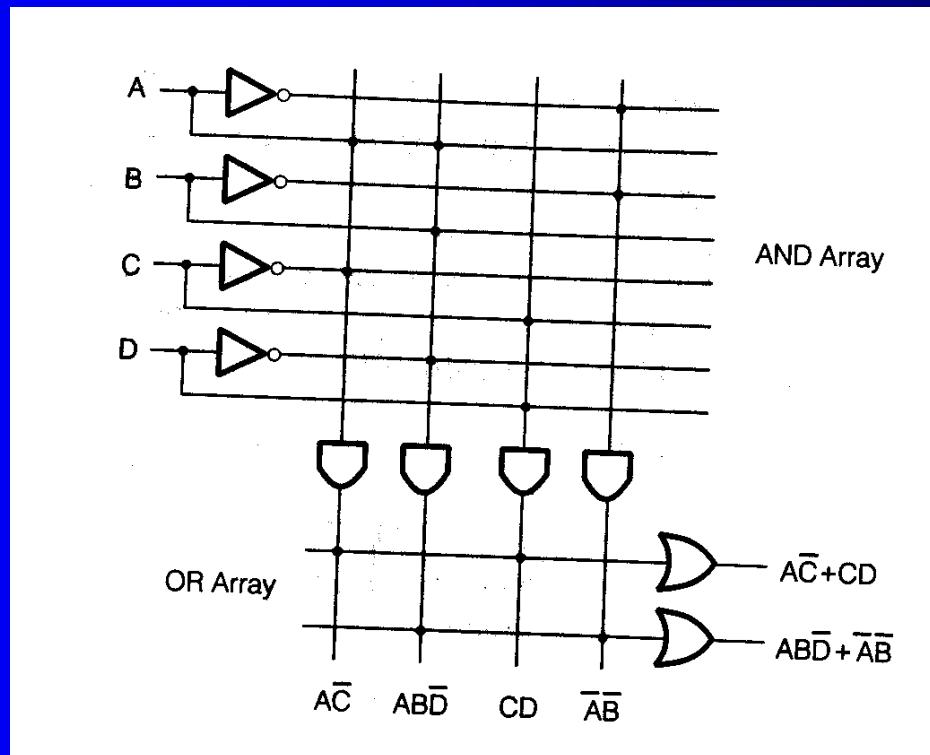
DISEÑO CON HARDWARE RECONFIGURABLE

- Hardware reconfigurable
- Flujo de diseño sobre FPGAs
- Arquitectura FPGAs Xilinx
- Placa de trabajo
- Prácticas

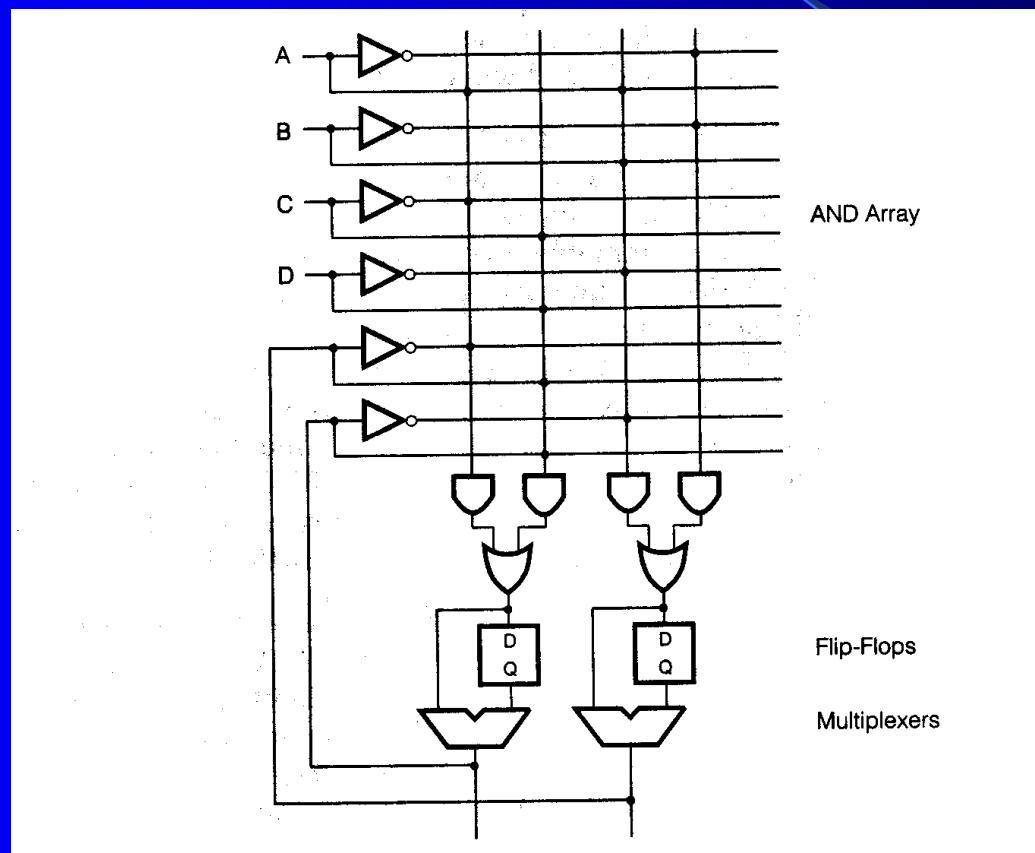
Hardware reconfigurable

Arrays Precableados

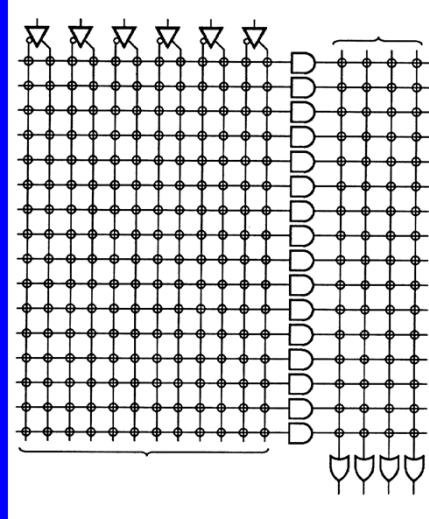
- Circuitos prefabricados con funcionalidad programable: PLA, PROM, PAL, CPLD, FPGA



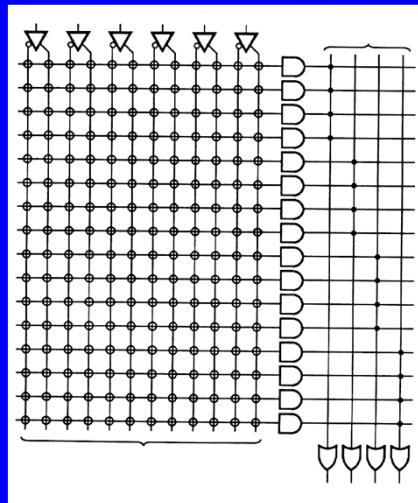
Hardware reconfigurable



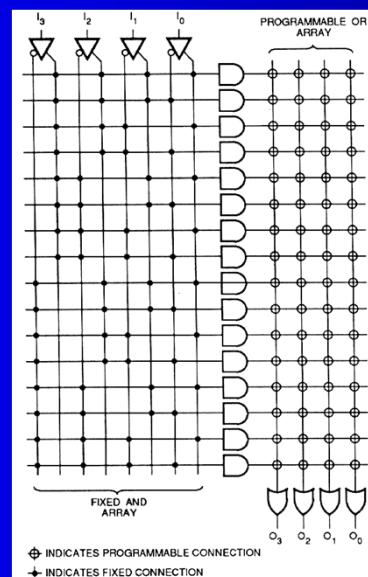
Hardware reconfigurable



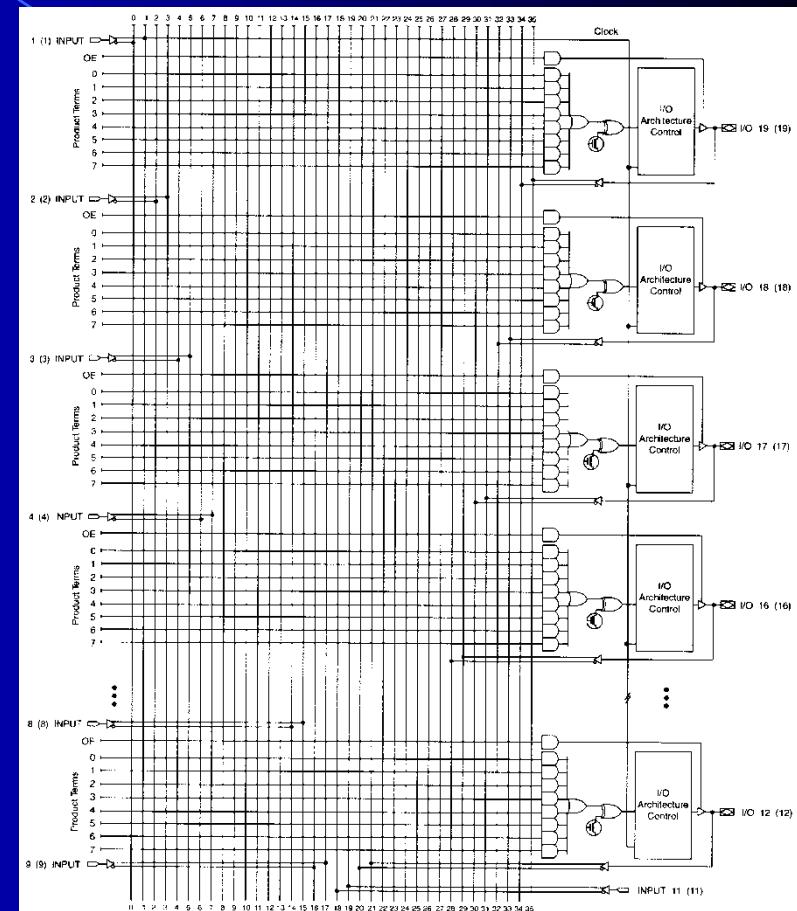
PLA



PAL



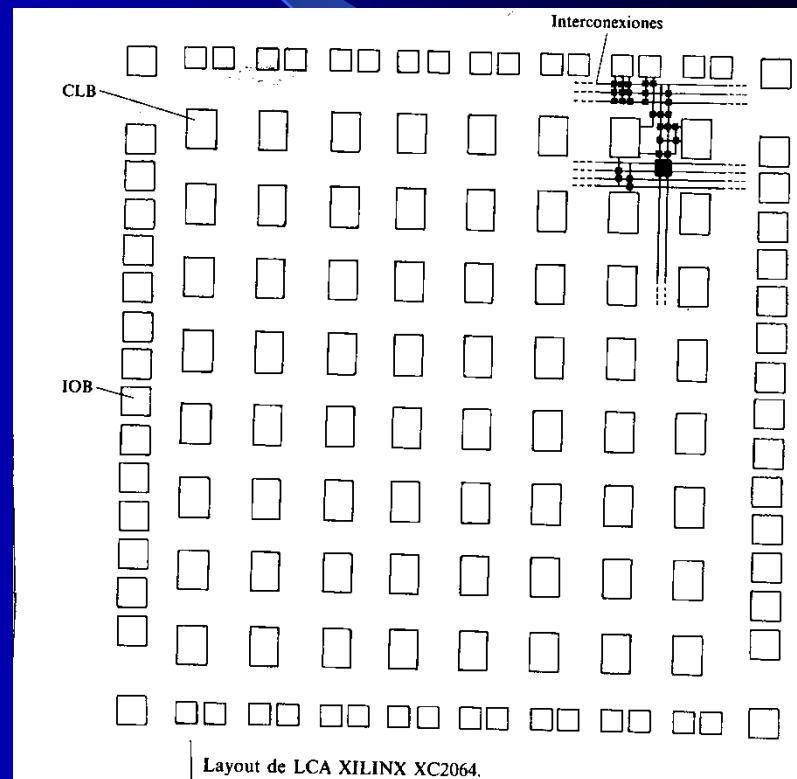
PROM



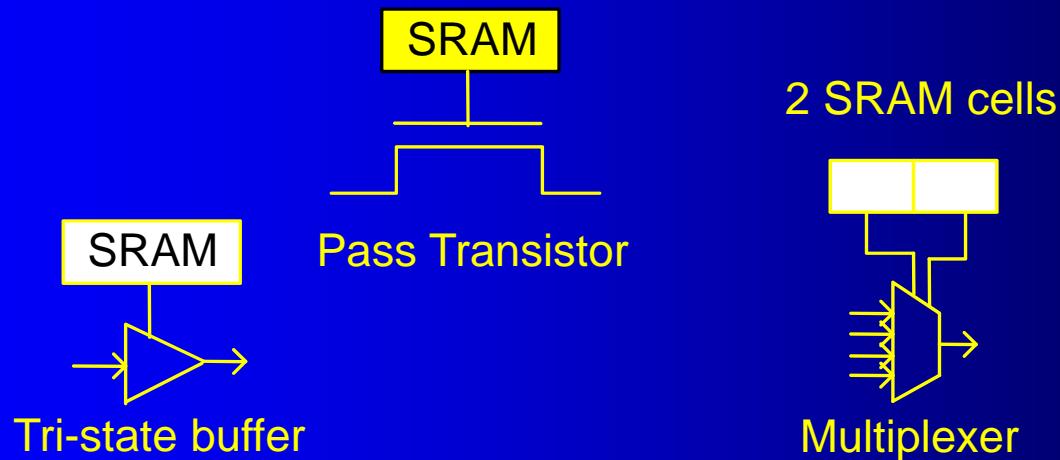
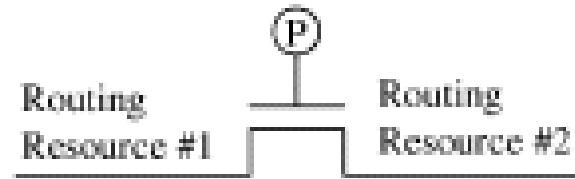
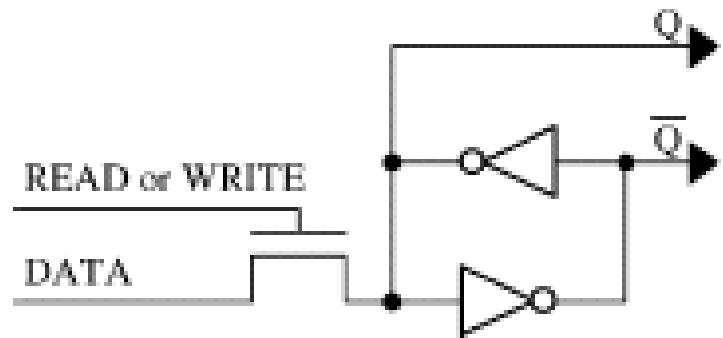
CPLD

Hardware reconfigurable

- **FPGA:**
 - Un array de celdas regularmente dispuestas sobre el silicio cuya funcionalidad es programable, denominados CLB.
 - Una colección de celdas de entrada/salida dispuestas perimetralmente cuyas características son programables, denominados IOB
 - Una colección de bloques de interconexión, que bajo programación permiten conectar CLBs e IOBs entre sí.

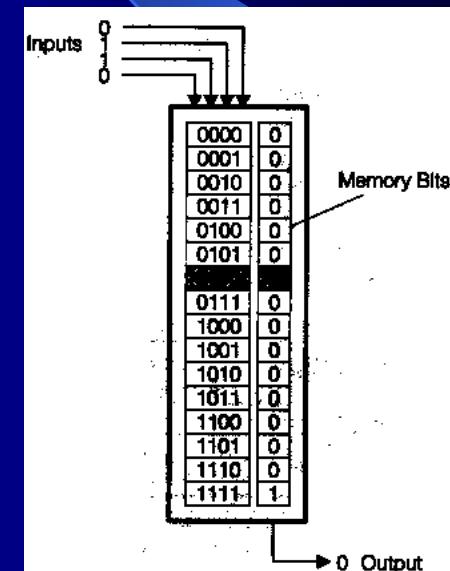
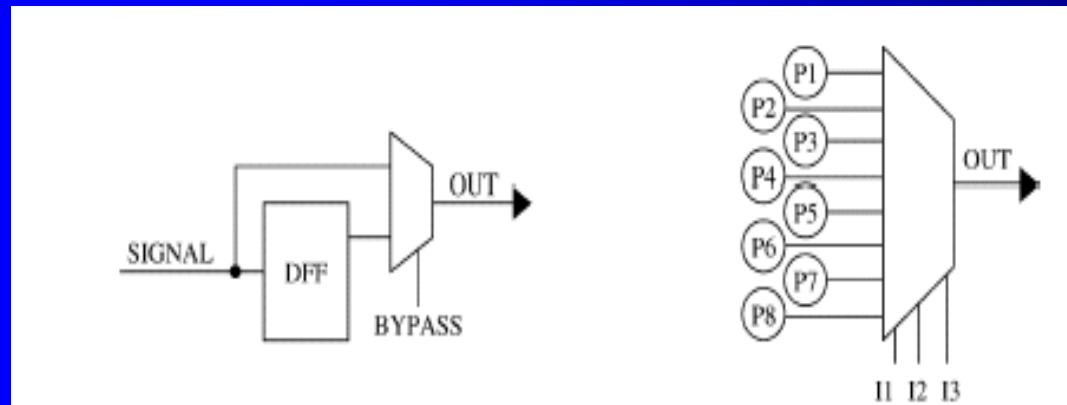


Hardware reconfigurable

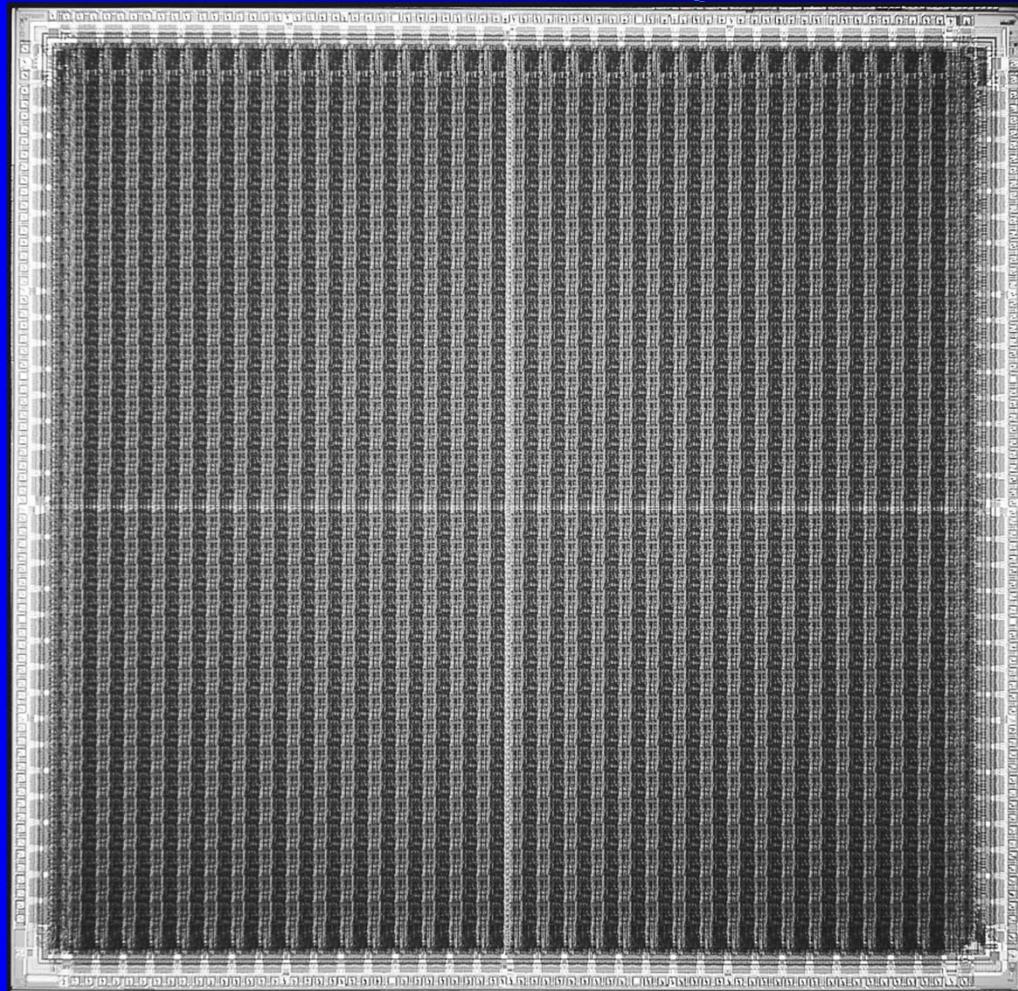


Hardware reconfigurable

- Los elementos de control o configuración sirven para:
 - 1.- Controlar los multiplexores
 - 2.- Implementar LUTs (Look Up Table)
 - 3.- Configurar el interconexiónado



Hardware reconfigurable



Xilinx XC4025

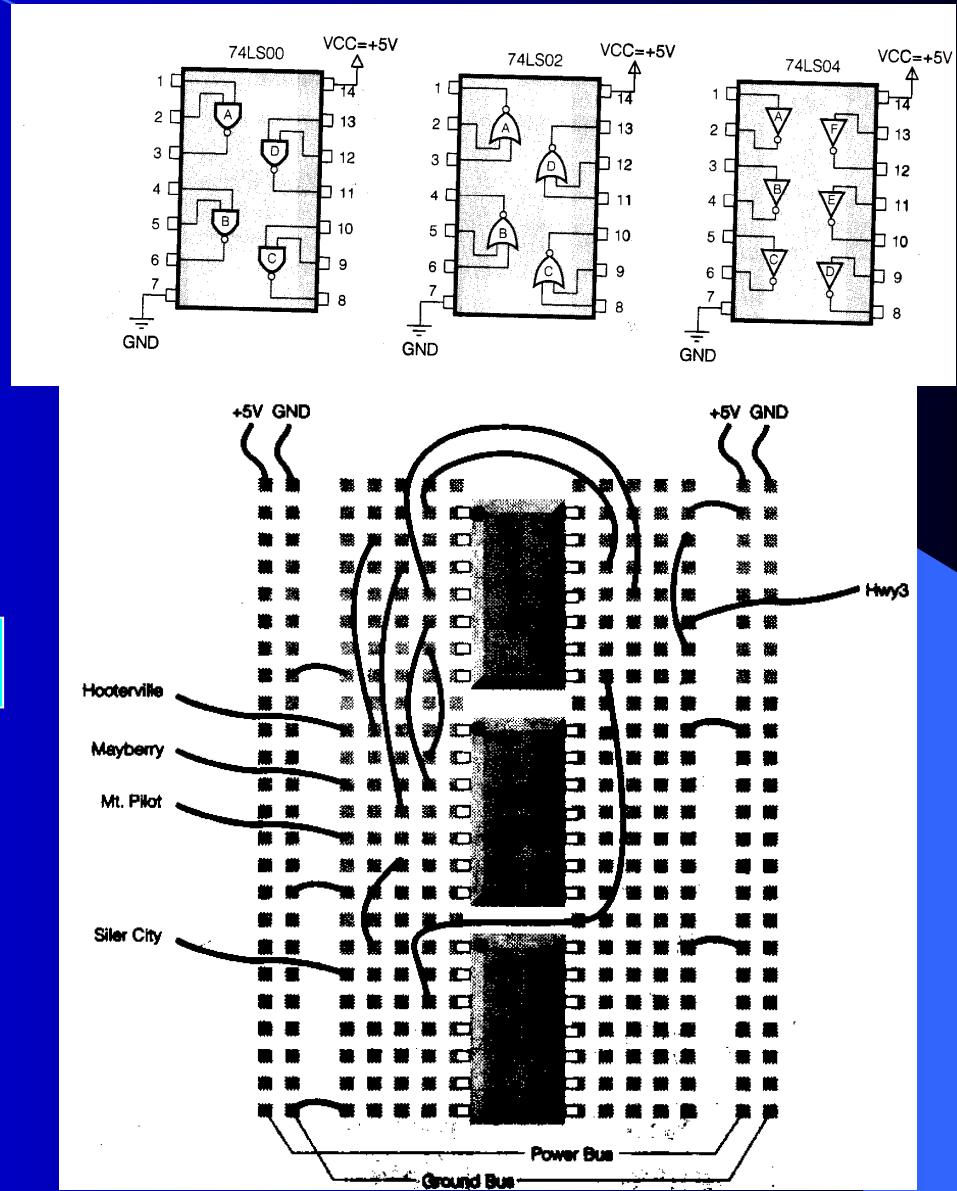
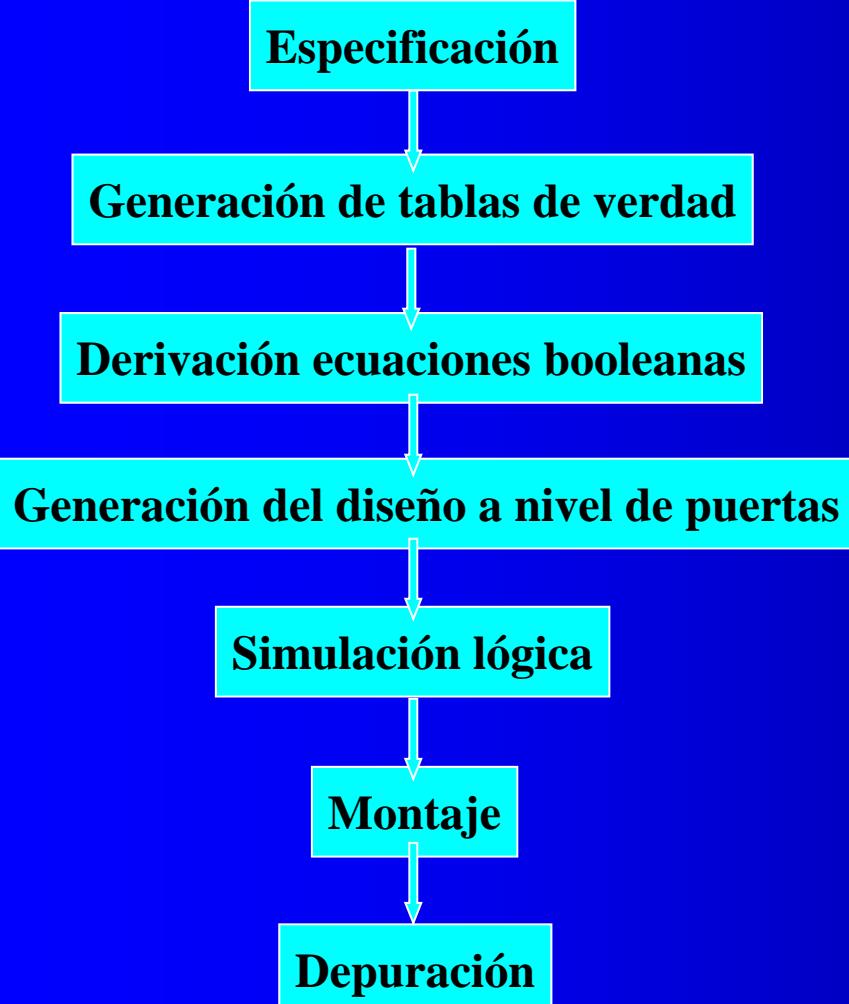
Hardware Reconfigurable

- **Metodología de diseño** para FPGA:
 - Los diseños no se fabrican, sino que se realizan programando adecuadamente los CLBs, IOBs y bloques de interconexión.
 - Cada bloque almacena su configuración (programa) en una SRAM, EPROM o en antifusibles. Dependiendo del método de almacenaje, el diseño volcado sobre la FPGA será o no volátil.
 - Funcionalmente las celdas son complejas y su grado de complejidad se denomina granularidad:
 - **Granularidad fina** (FPGAs): cualquier función de conmutación de 4~6 variables y varios FFs.
 - **Granularidad gruesa** (FIPSOCS, sistemas reconfigurables): ALUs y varios registros.
- **Características:**
 - El diseño físico y la fabricación es independiente del diseño particular.
 - Diseños complejos pueden no caber en una FPGA.

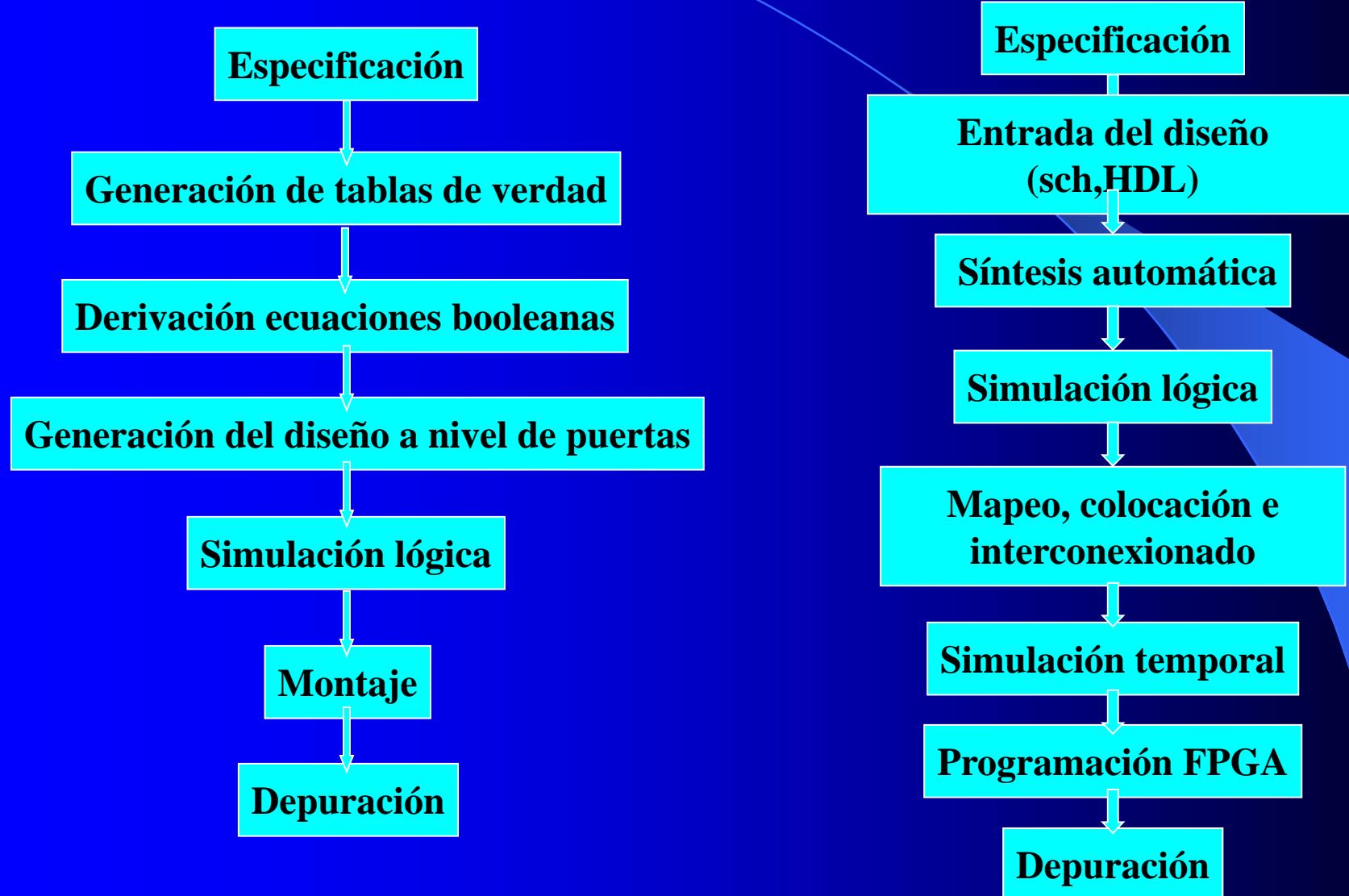
DISEÑO CON HARDWARE RECONFIGURABLE

- Hardware Reconfigurable
- **Flujo de diseño sobre FPGAs**
- Arquitectura FPGAs Xilinx
- Placa de trabajo
- Prácticas

Flujo de diseño

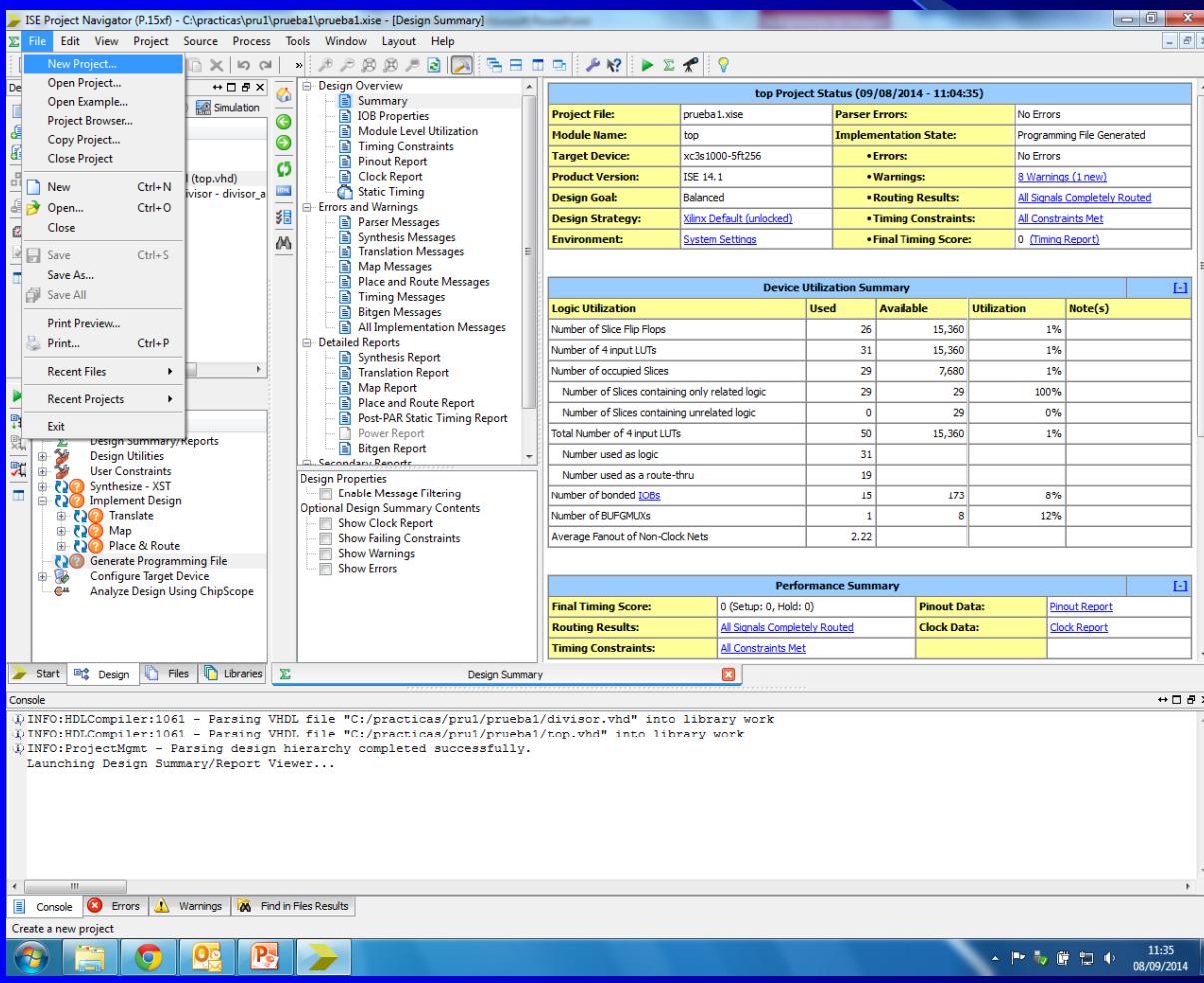


Flujo de diseño

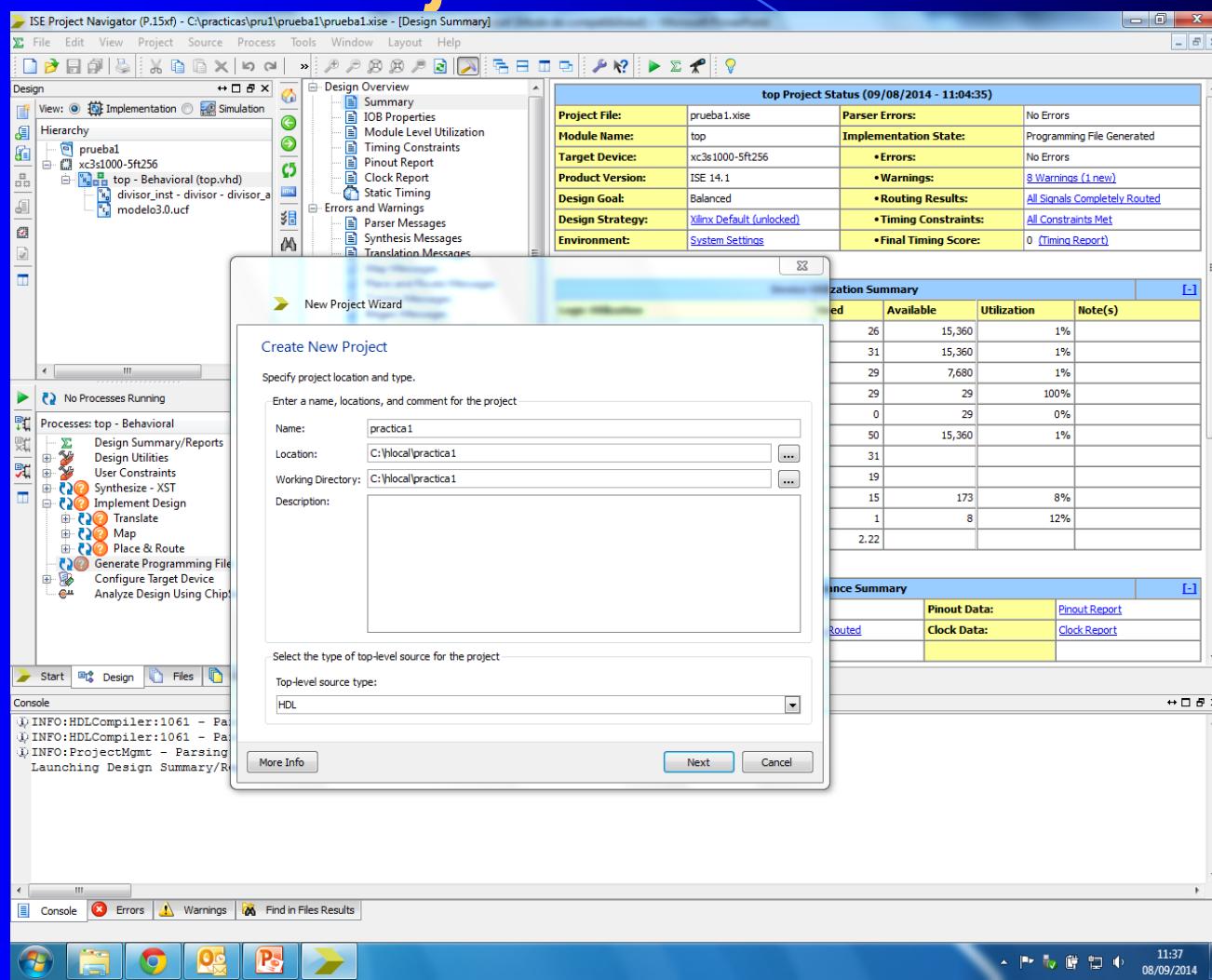


Flujo de diseño

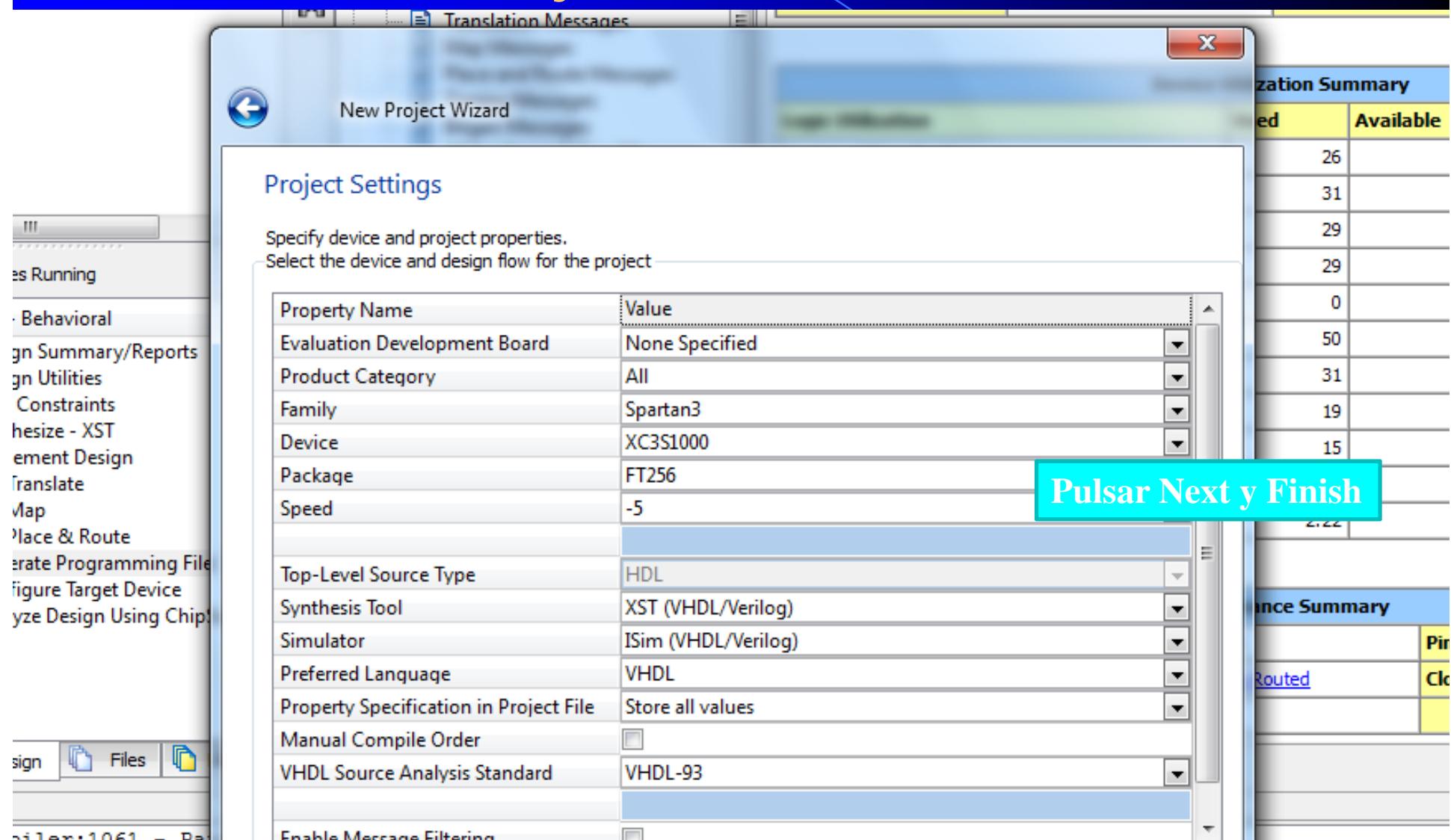
Xilinx ISE



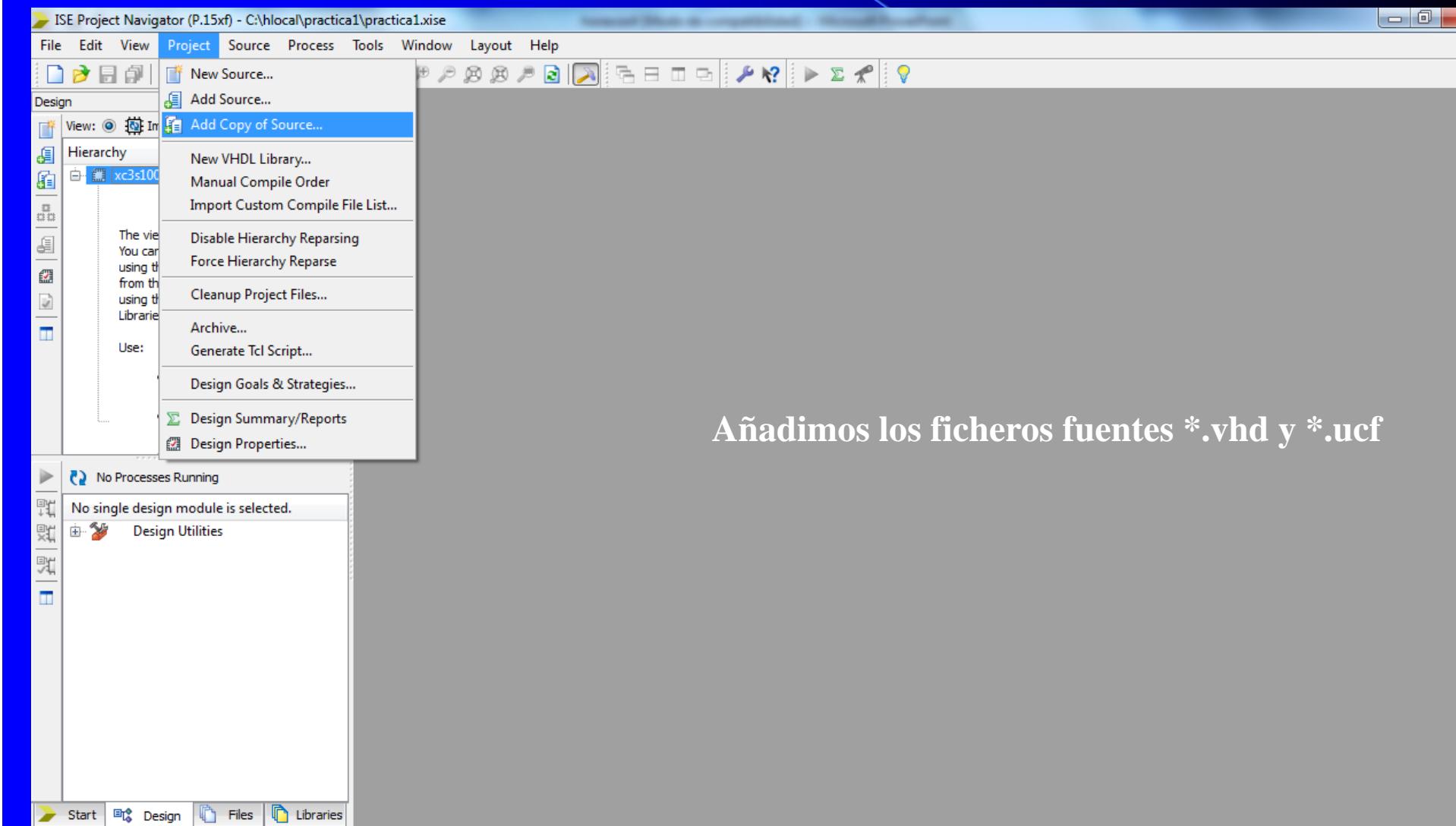
Flujo de diseño



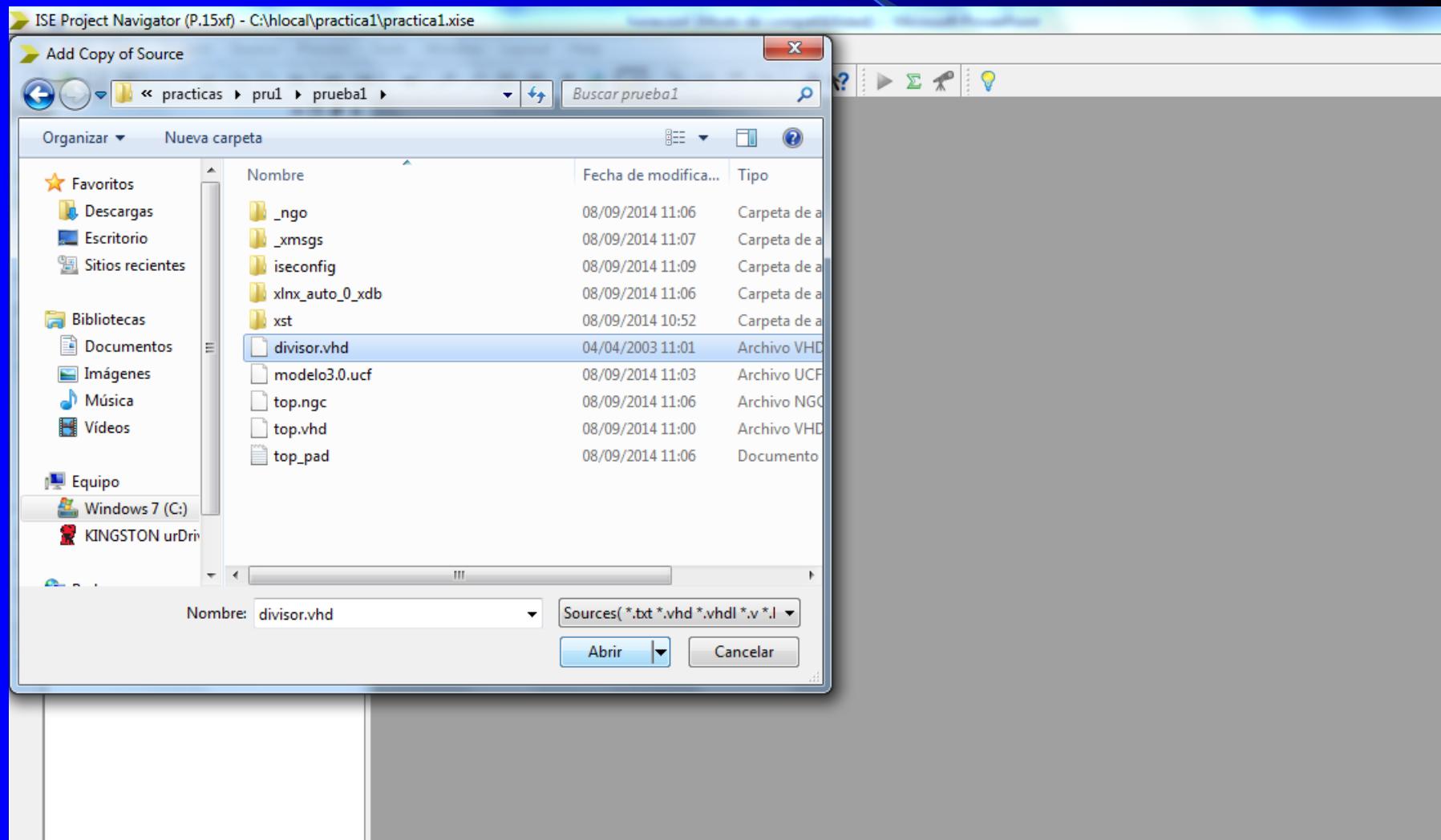
Flujo de diseño



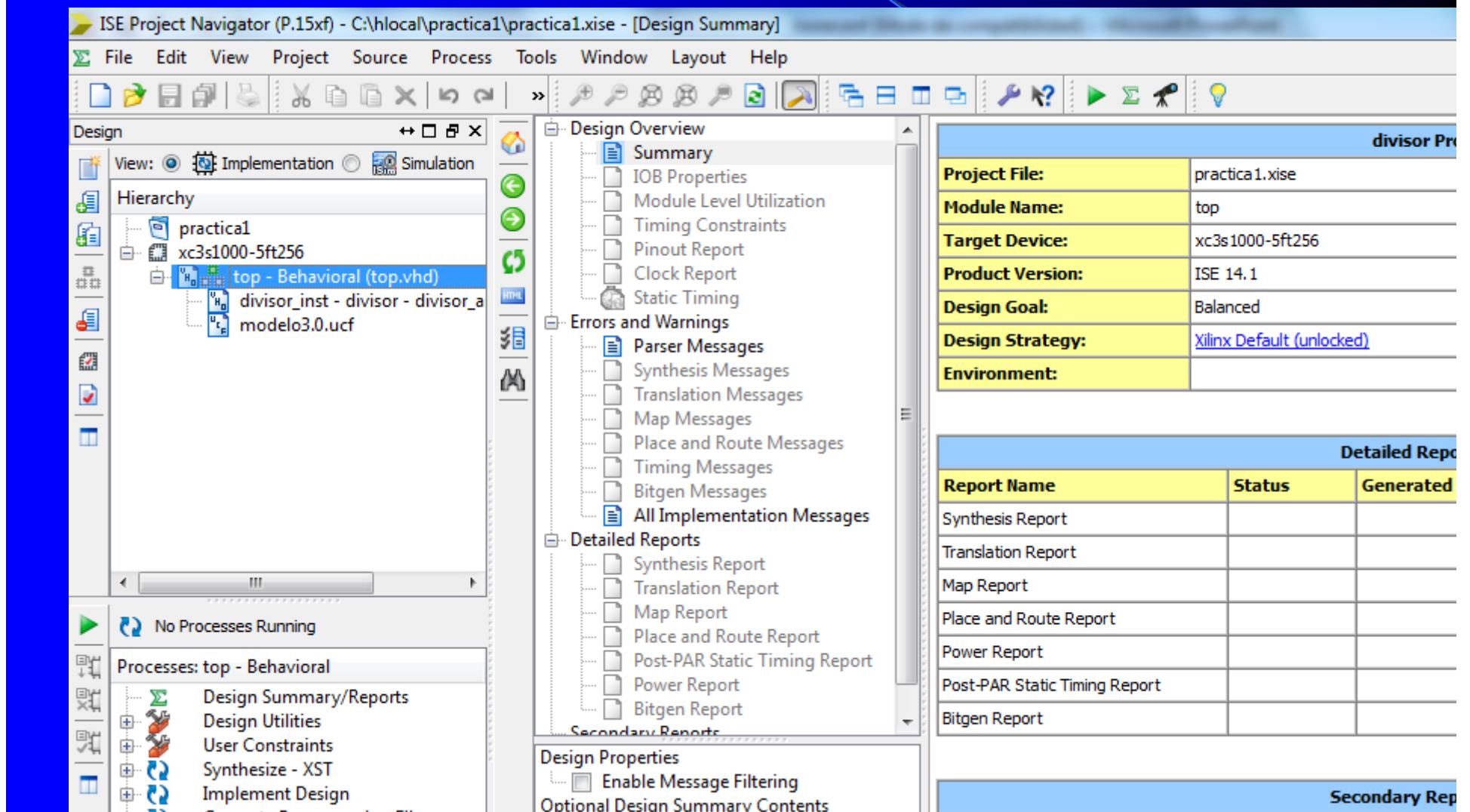
Flujo de diseño



Flujo de diseño



Flujo de diseño



Flujo de diseño

The screenshot shows the Xilinx ISE Project Navigator interface. The project is named "practica1" and the top module is "top - Behavioral (top.vhd)". The "Design" view is selected, showing the hierarchy of files: practical1, xc3s1000-5ft256, top - Behavioral (top.vhd), divisor_inst - divisor - divisor_a, and modelo3.0.ucf. The "Design Overview" pane lists various reports like Summary, IOB Properties, Module Level Utilization, Timing Constraints, Pinout Report, Clock Report, and Static Timing. The "Errors and Warnings" pane lists Parser Messages, Synthesis Messages, Translation Messages, Map Messages, Place and Route Messages, Timing Messages, Bitgen Messages, and All Implementation Messages. The "Detailed Reports" pane lists Synthesis Report, Translation Report, Map Report, Place and Route Report, Post-PAR Static Timing Report, Power Report, Post-PAR Static Timing Report, and Bitgen Report. The "Secondary Reports" pane lists Design Properties, Optional Design Summary Contents, and a list of reports: Clock Report, Failing Constraints, Warnings, and Error. A context menu is open over the "Generate Programming File" option, showing options like Run, ReRun, Rerun All, Stop, View Text Report, Force Process Up-to-Date, and Implement Top Module. The "Project Status" section shows the project file is practica1.xise, module name is top, target device is xc3s1000-5ft256, product version is ISE 14.1, design goal is Balanced, design strategy is Xilinx Default (unlocked), and environment is Xilinx Default (unlocked). The "Detailed Reports" section shows a table with columns: Report Name, Status, Generated, Errors, and Warnings. The "Secondary Reports" section shows a table with columns: Report Name, Status, and Generated. The date generated is 09/08/2014 - 11:47:44.

ISE Project Navigator (P.15xf) - C:\hlocal\practical\practica1.xise - [Design Summary]

File Edit View Project Source Process Tools Window Layout Help

Design Overview

- Summary
- IOB Properties
- Module Level Utilization
- Timing Constraints
- Pinout Report
- Clock Report
- Static Timing

Errors and Warnings

- Parser Messages
- Synthesis Messages
- Translation Messages
- Map Messages
- Place and Route Messages
- Timing Messages
- Bitgen Messages
- All Implementation Messages

Detailed Reports

- Synthesis Report
- Translation Report
- Map Report
- Place and Route Report
- Post-PAR Static Timing Report
- Power Report
- Post-PAR Static Timing Report
- Bitgen Report

Secondary Reports

- Design Properties
- Optional Design Summary Contents
- Enable Message Filtering
- Clock Report
- Failing Constraints
- Warnings
- Error

Project Status

Project File:	practica1.xise	Parser Errors:
Module Name:	top	Implementation State:
Target Device:	xc3s1000-5ft256	• Errors:
Product Version:	ISE 14.1	• Warnings:
Design Goal:	Balanced	• Routing Results:
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:
Environment:		• Final Timing Score:

Detailed Reports

Report Name	Status	Generated	Errors	Warnings
Synthesis Report				
Translation Report				
Map Report				
Place and Route Report				
Power Report				
Post-PAR Static Timing Report				
Bitgen Report				

Secondary Reports

Report Name	Status	Generated

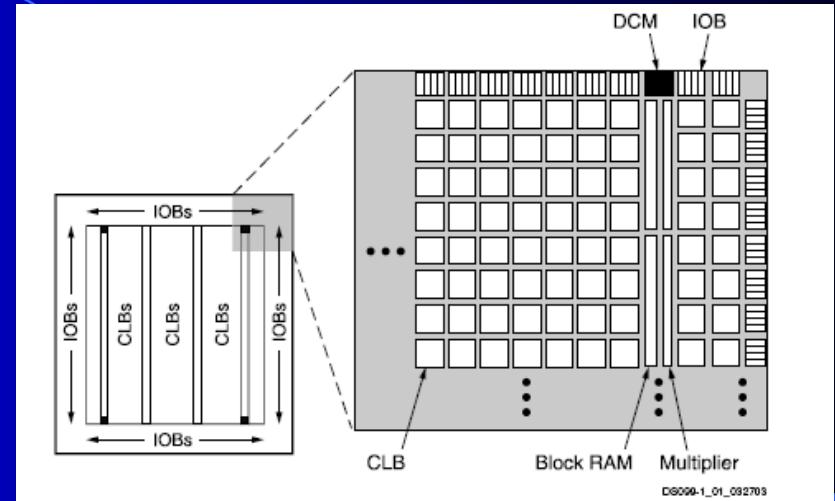
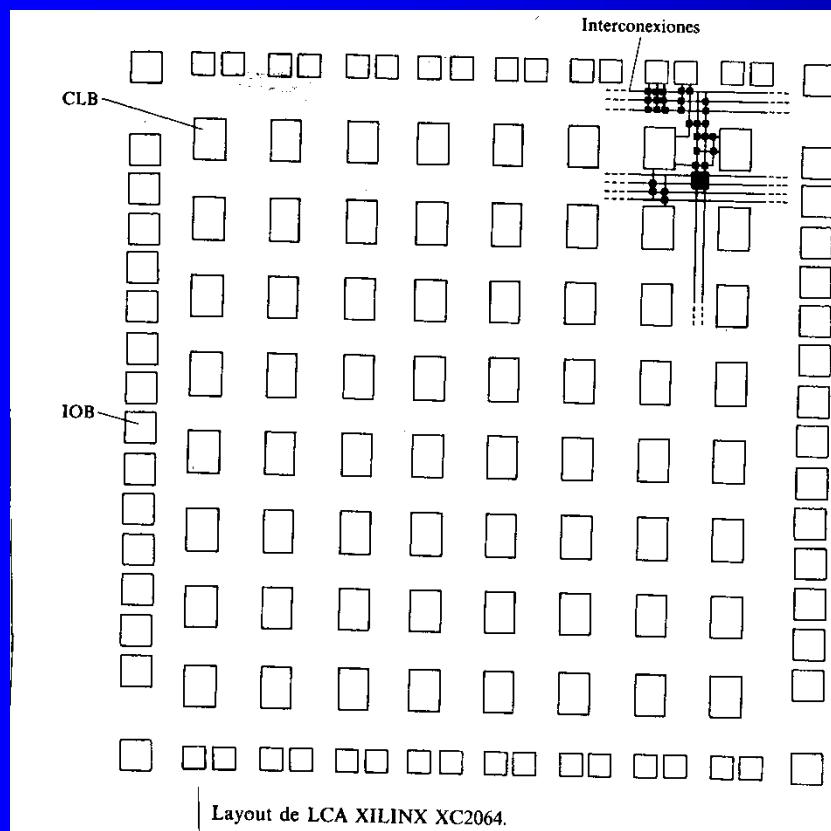
Date Generated: 09/08/2014 - 11:47:44

Para generar el *.bit se pulsa Generate Programming File
El *.bit queda en el directorio de nuestra práctica

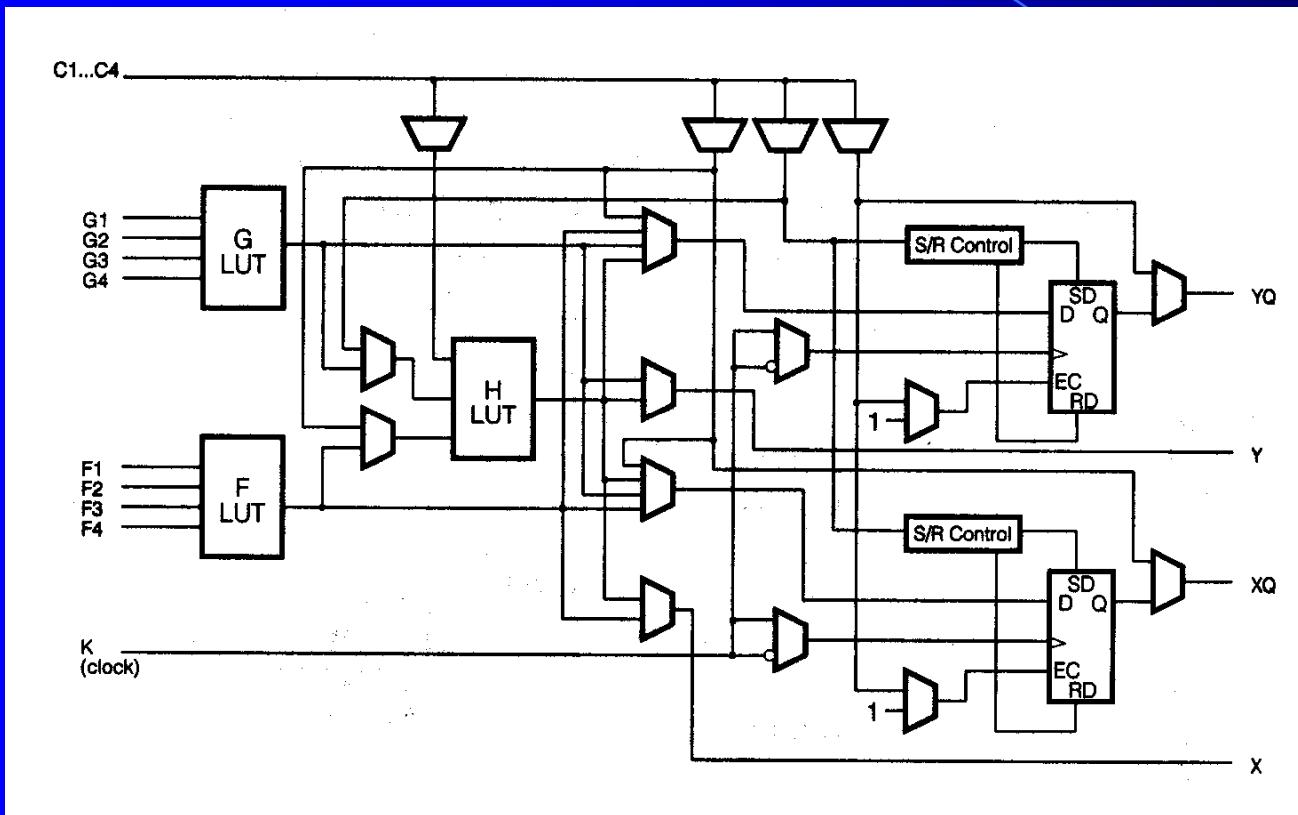
DISEÑO CON HARDWARE RECONFIGURABLE

- Hardware Reconfigurable
- Flujo de diseño sobre FPGAs
- Arquitectura FPGAs Xilinx
- Placa de trabajo
- Prácticas

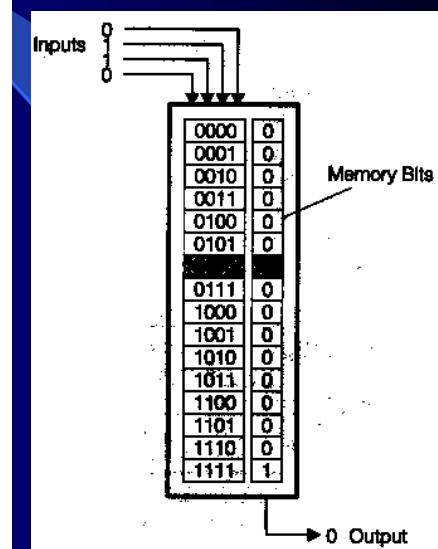
Arquitectura FPGAs Xilinx



Arquitectura FPGAs Xilinx

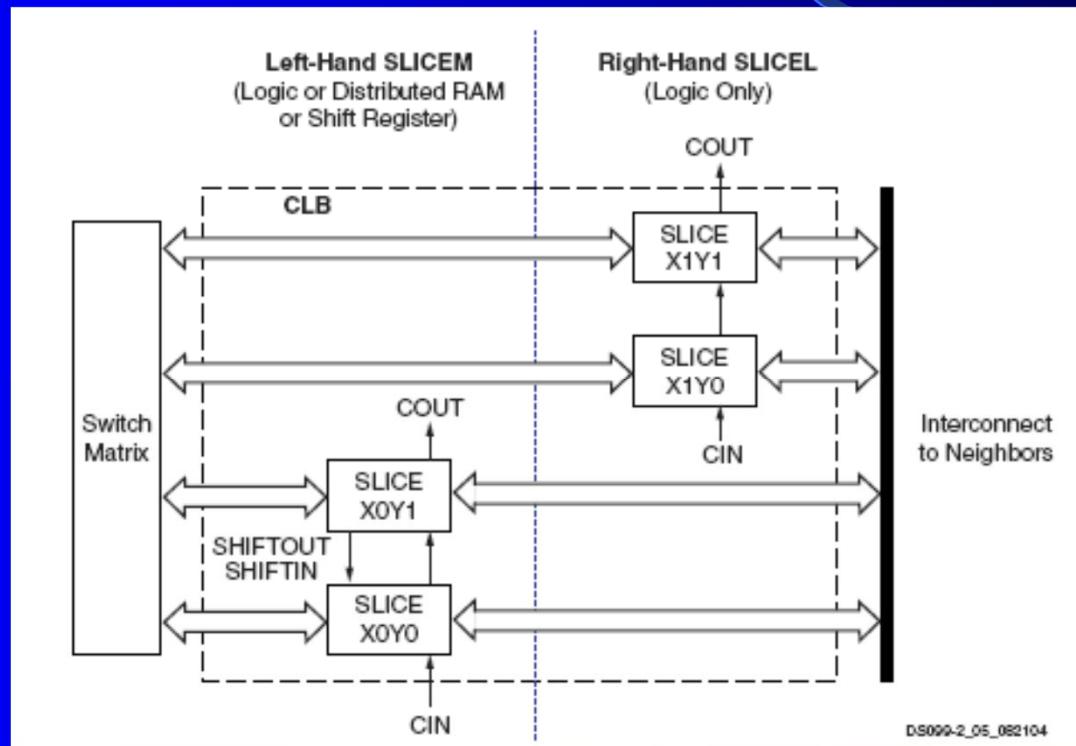


Estructura de un CLB



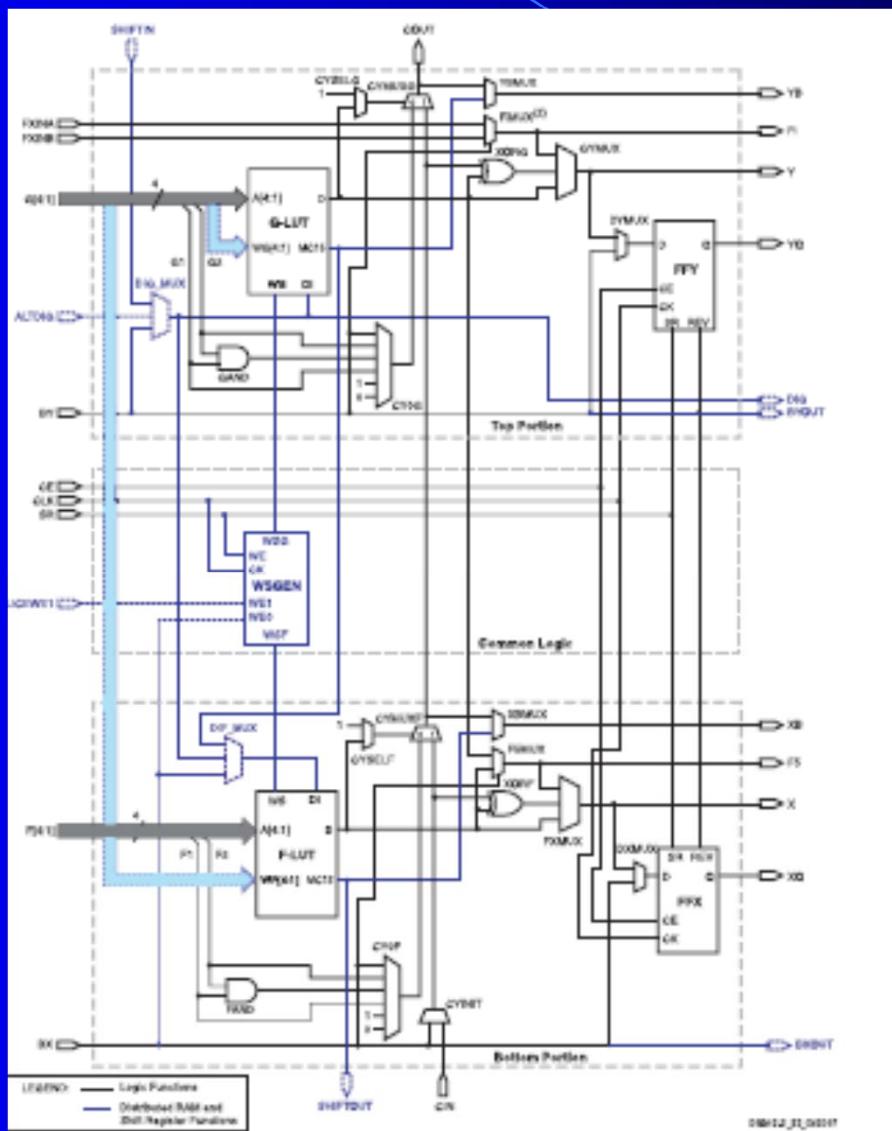
Estructura de una LUT
Look Up Table

Arquitectura FPGAs Xilinx

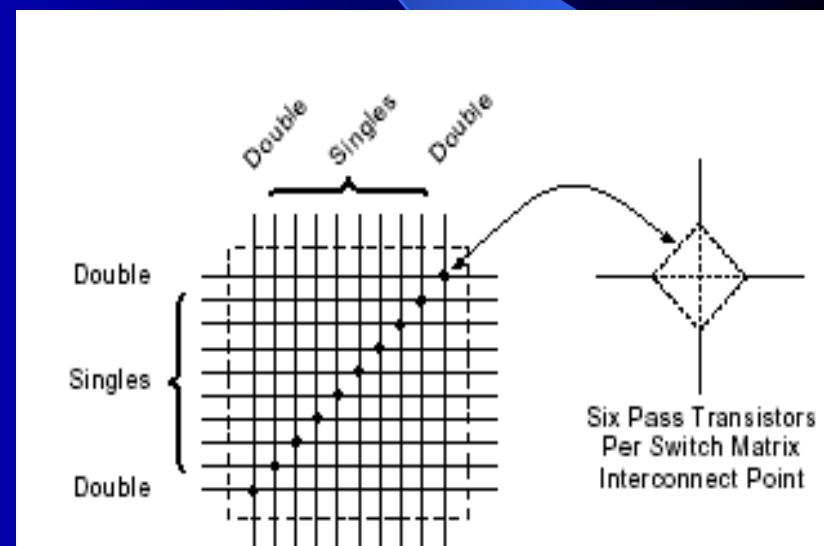
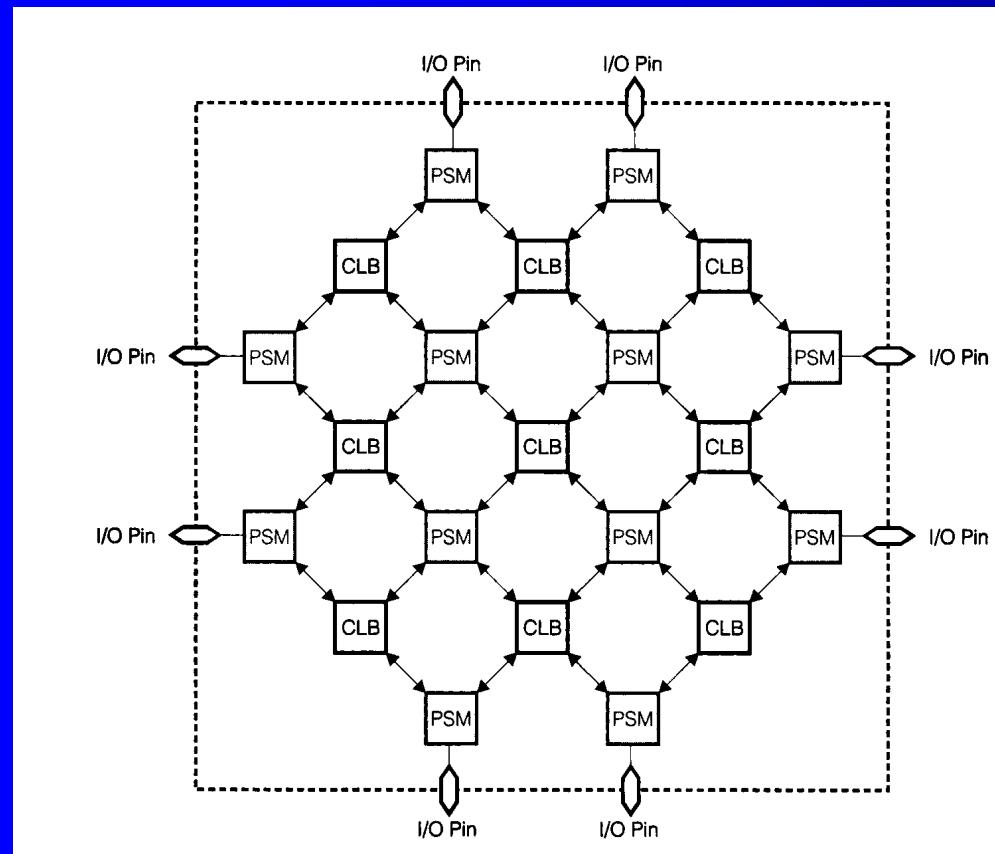


CLB de una Spartan 3

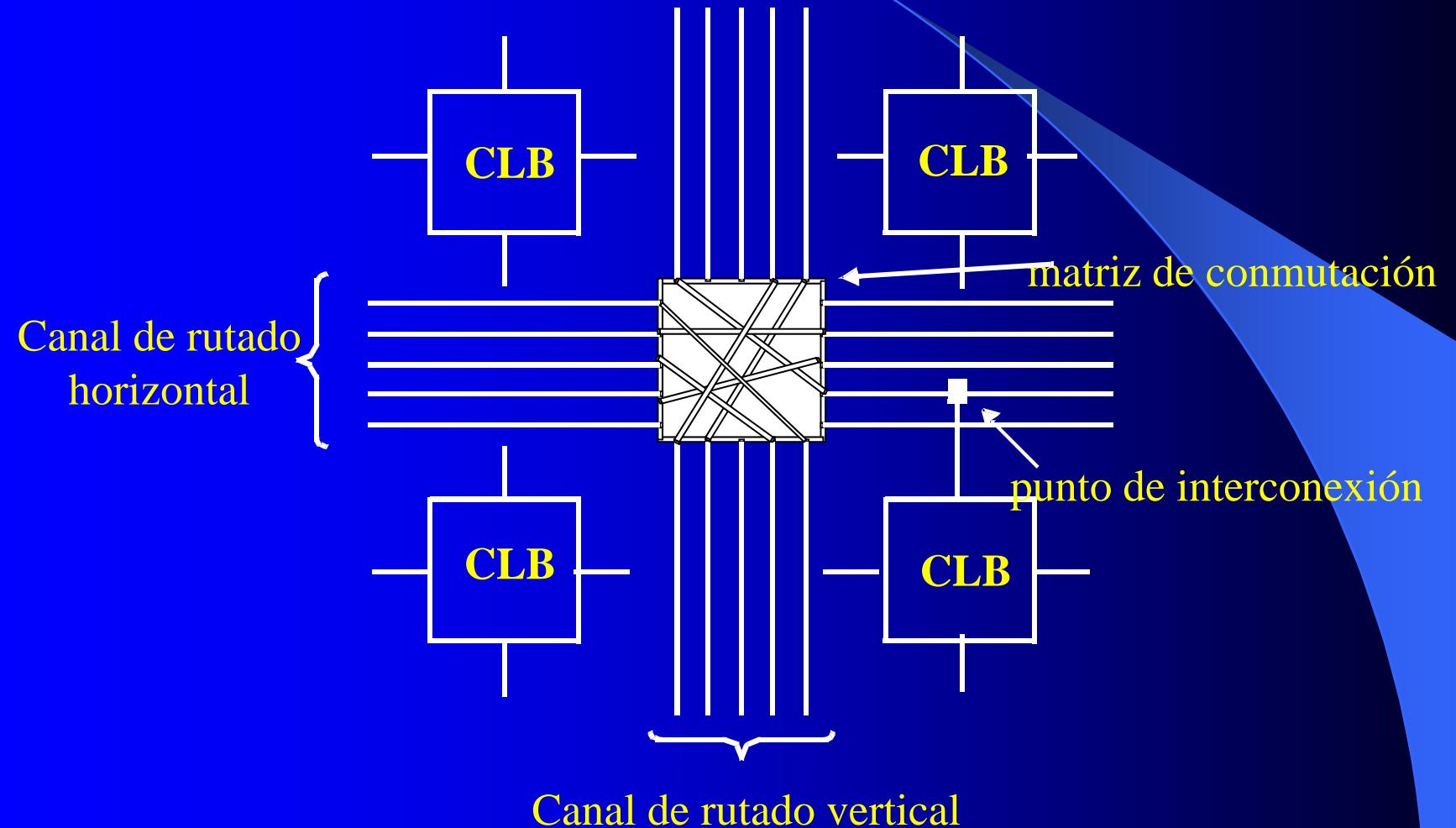
Arquitectura FPGAs Xilinx



Arquitectura de las FPGAs

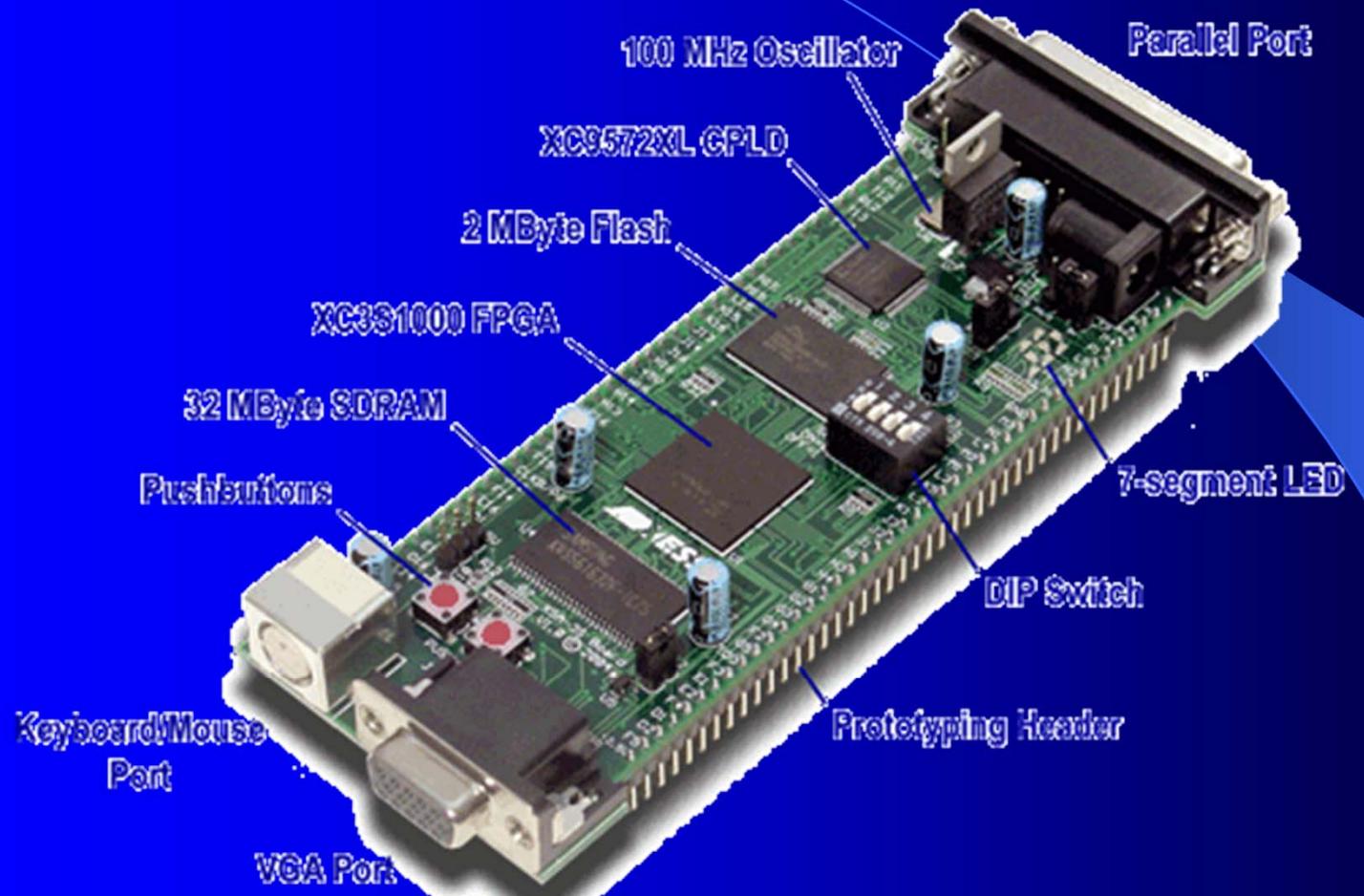


Arquitectura FPGAs Xilinx

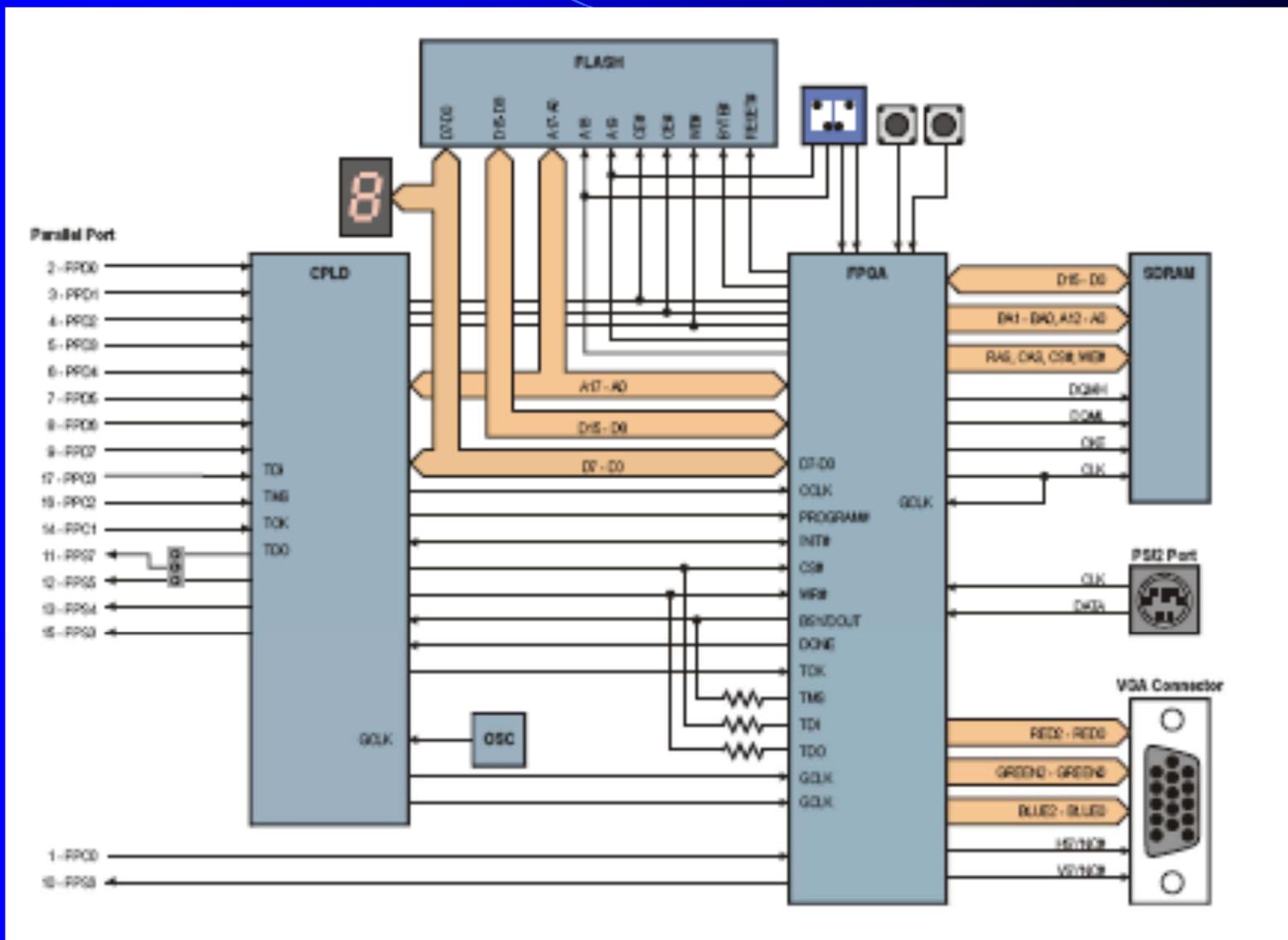


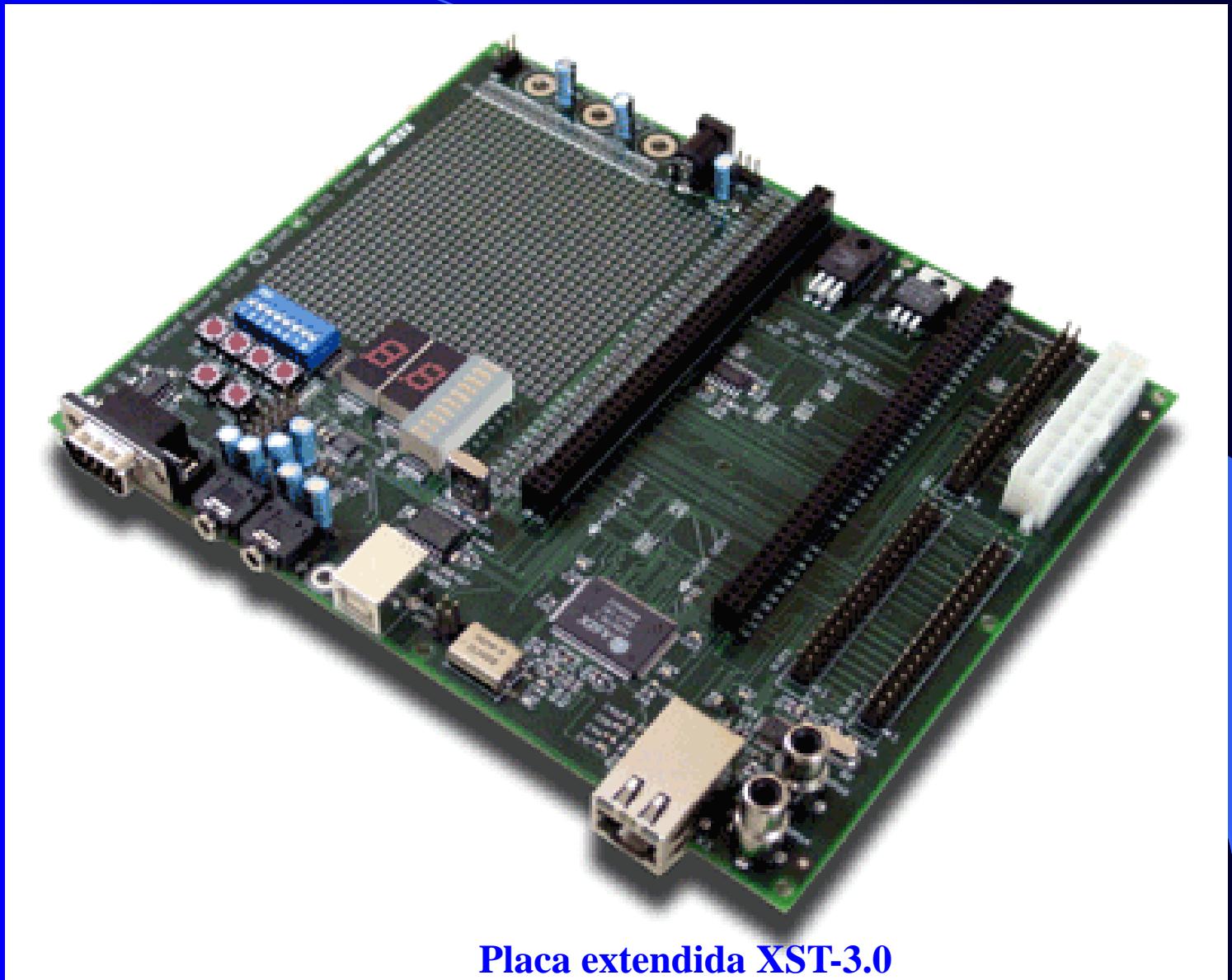
DISEÑO CON HARDWARE RECONFIGURABLE

- Hardware Reconfigurable
- Flujo de diseño sobre FPGAs
- Arquitectura FPGAs Xilinx
- **Placa de trabajo**
- Prácticas

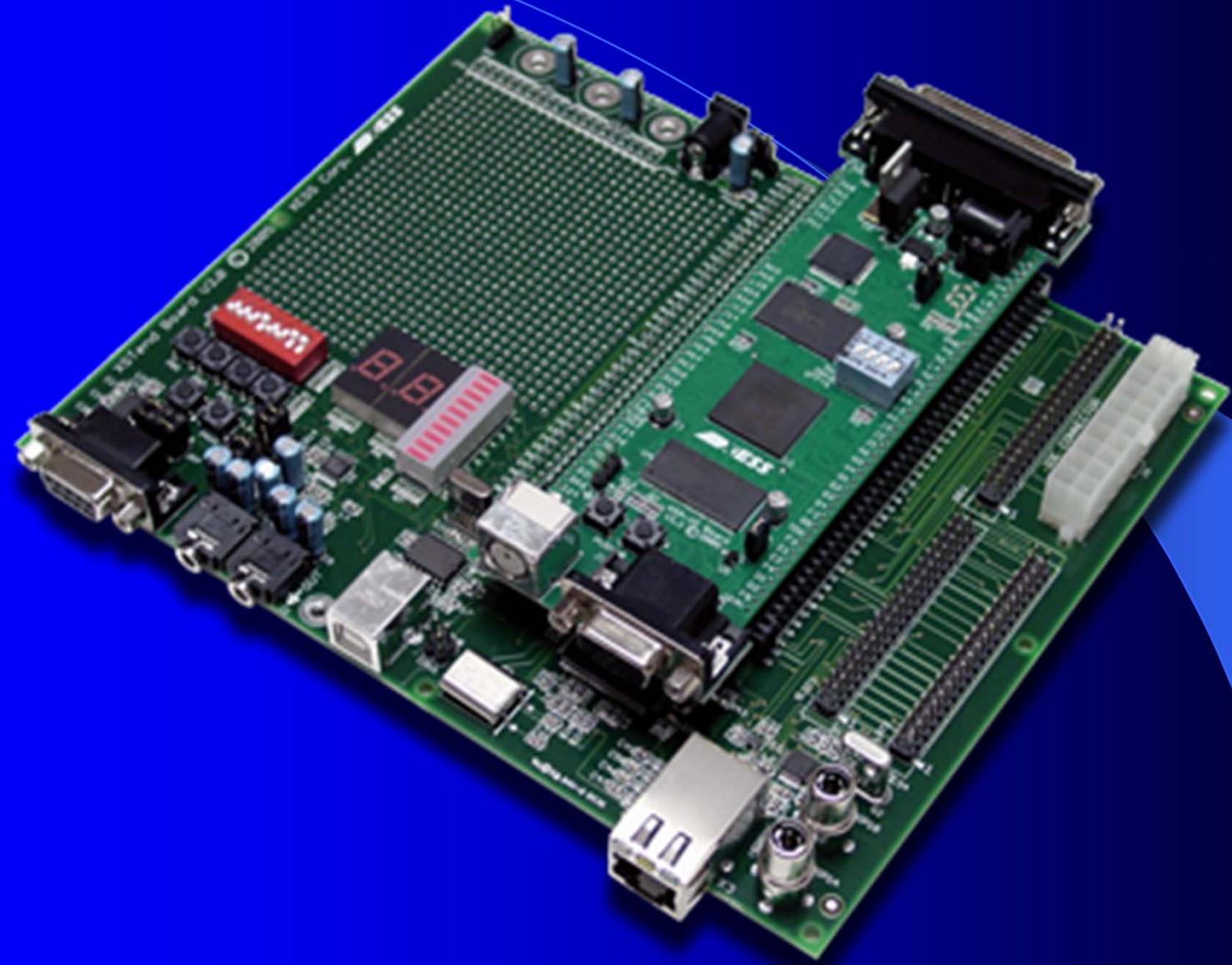


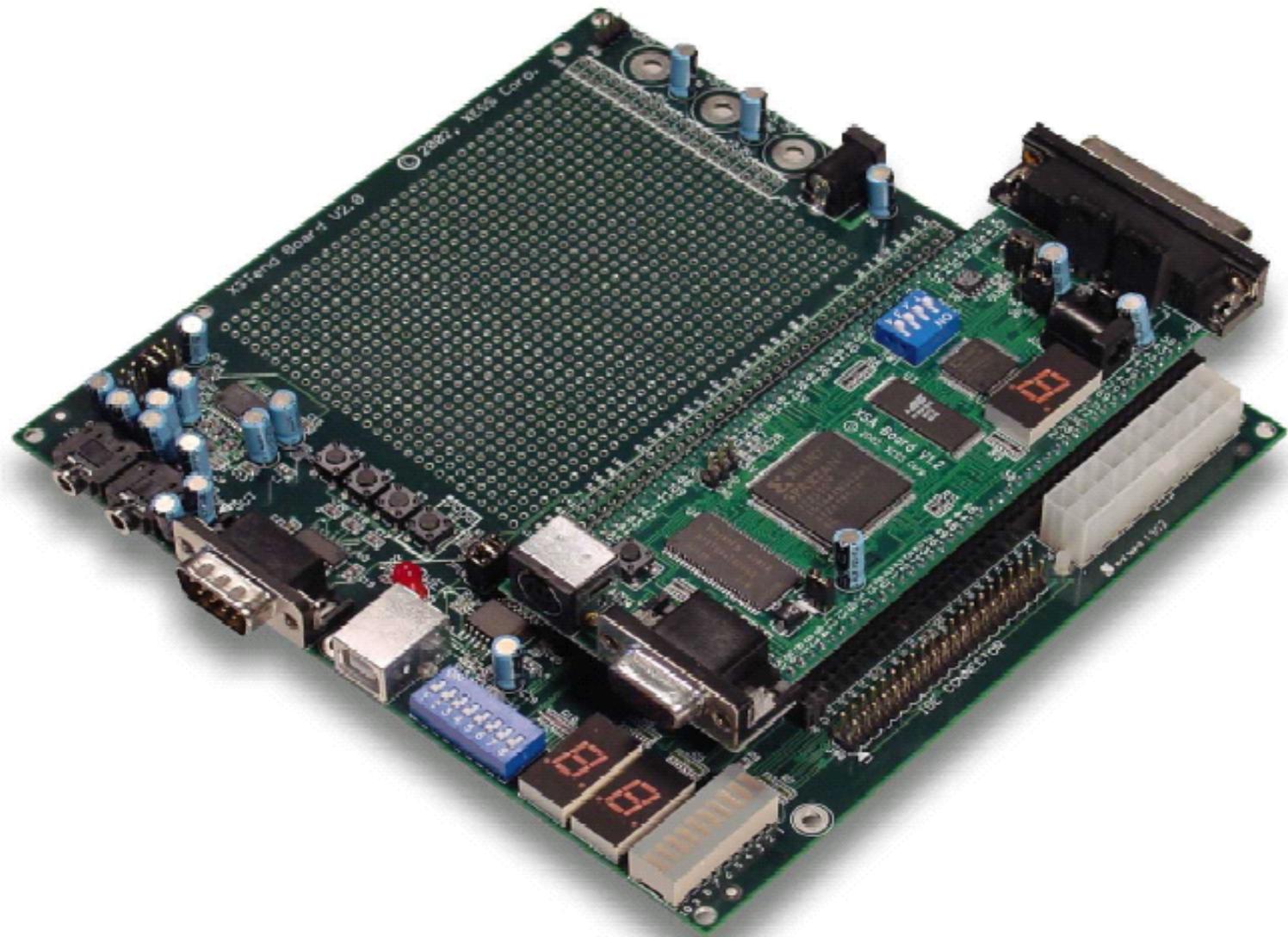
Placa base XSA-3S



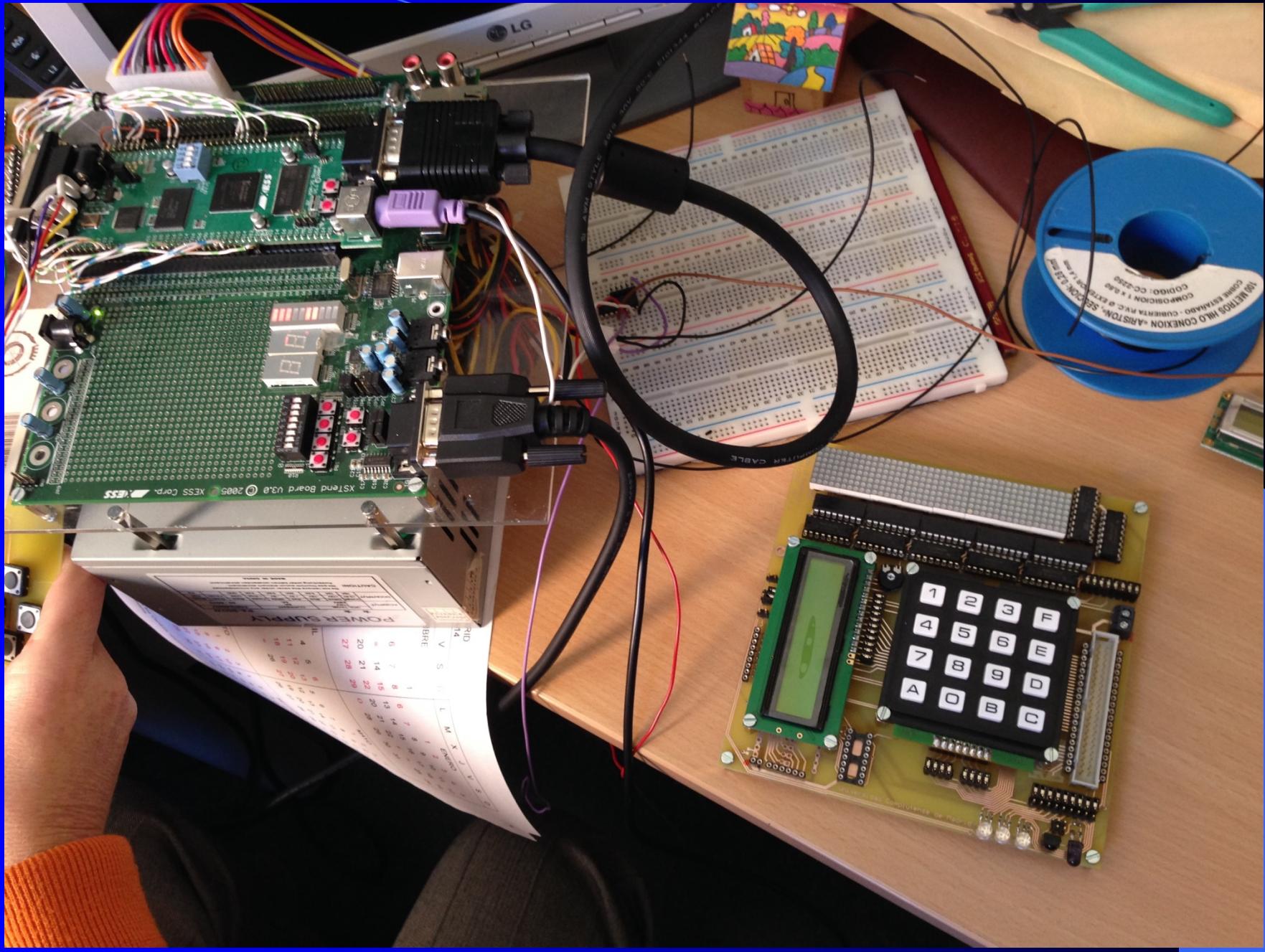


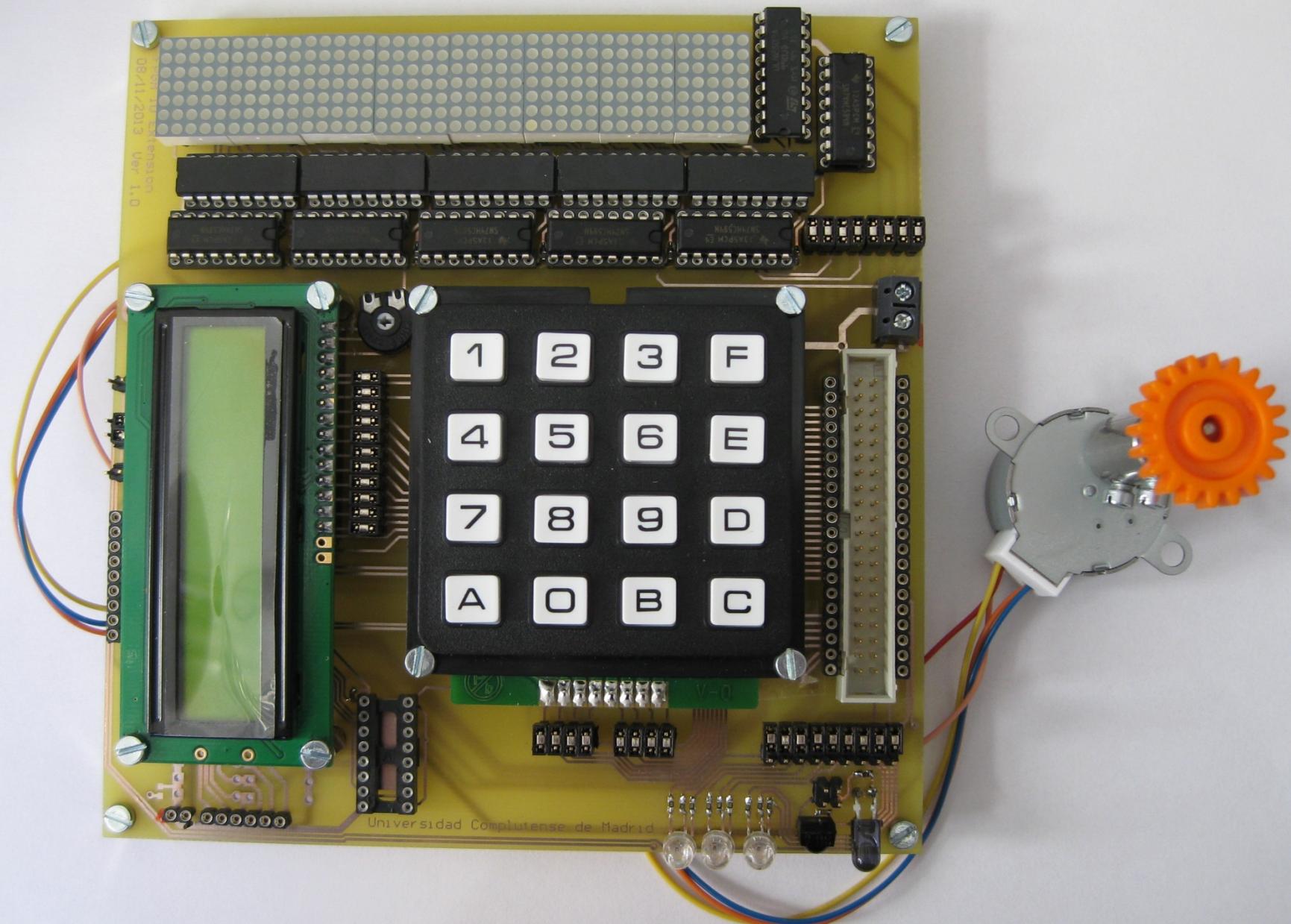
Placa extendida XST-3.0





Placa base XSA-3S, placa de extensión XST-3.0





DISEÑO CON HARDWARE RECONFIGURABLE

- Hardware reconfigurable
- Flujo de diseño sobre FPGAs
- Arquitectura FPGAs Xilinx
- Placa de trabajo
- **Prácticas**

Prácticas

Práctica 1 . Juego (FPGAs de Xilinx).

- 1.- El usuario mete 3 números
- 2.- Hay dos premios
 - Mayor: si los 3 son iguales
 - Menor: si hay dos iguales