Lab 2 - Combinational Design

- Primary Objectives:
  - Design and simulate a circuit consisting of 4 inputs; A, B, C & D, and two outputs, P (for pair) & T (for trio).
  - The outputs should follow the behavior of:
    - P should be true (1) if and only if two input pins are true, otherwise P should be false (0)
    - T should be true if and only if three input pins are true, otherwise T should be false (0)
    - Neither outputs should be true for any other input conditions ie 4 inputs are true
- Objective #1: Circuit Design
  - Table #1: Truth table for intended circuit functionality
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A	B	C	D	P(pair)	T(trio)
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	0	1
1	0	0	0	0	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	0	0

- Note:
  - From the truth table we can see that there are 6 input combinations that result in the output P being True
  - We can also see that there are 4 input conditions that result in the output T being True
- Design:
  - P output
    - The circuit that activates the Pair output will consist of 6 AND gates:
      - AB | AC | AD | BC | BD | CD
    - Each AND gate with then be routed into 1 of 6 input terminals on a XOR gate
    - The XOR gate will then terminate to the P output
      - The XOR gate will ensure that only *one* AND gate (and therefore only two inputs) is true, in order to turn the P output True
  - T output
    - The circuit that activates the Trio output will consist of 4 AND gates, which are terminated from the AND gates from the P circuit
      - AB + AC = ABC | AB + AD = ABD | BC + BD = BCD | AC + CD = ACD
    - Each AND gate will then be terminated into 1 of 4 input terminals on a XOR gate, which outputs to the T output
      - This ensures that only one AND gate (and therefore two P circuit AND gates -> therefore 3 input devices) is responsible for triggering the T output, when 3 inputs are true
- Boolean Expression for Circuit Design:
  - Pair output: P = ((ABC'D') ⊕ (AB'CD') ⊕ (AB'C'D) ⊕ (A'BCD') ⊕ (A'BC'D) ⊕ (A'B'CD)) = **((AB) ⊕ (AC) ⊕ (AD) ⊕ (BC) ⊕ (BD) ⊕ (CD))**
  - Trio output: T = ((ABCD') ⊕ (ABC'D) ⊕ (AB'CD) ⊕ (A'BCD)) = **((ABC) ⊕ (ABD) ⊕ (ACD) ⊕ (BCD))**
- Figure #1: Circuit Design
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