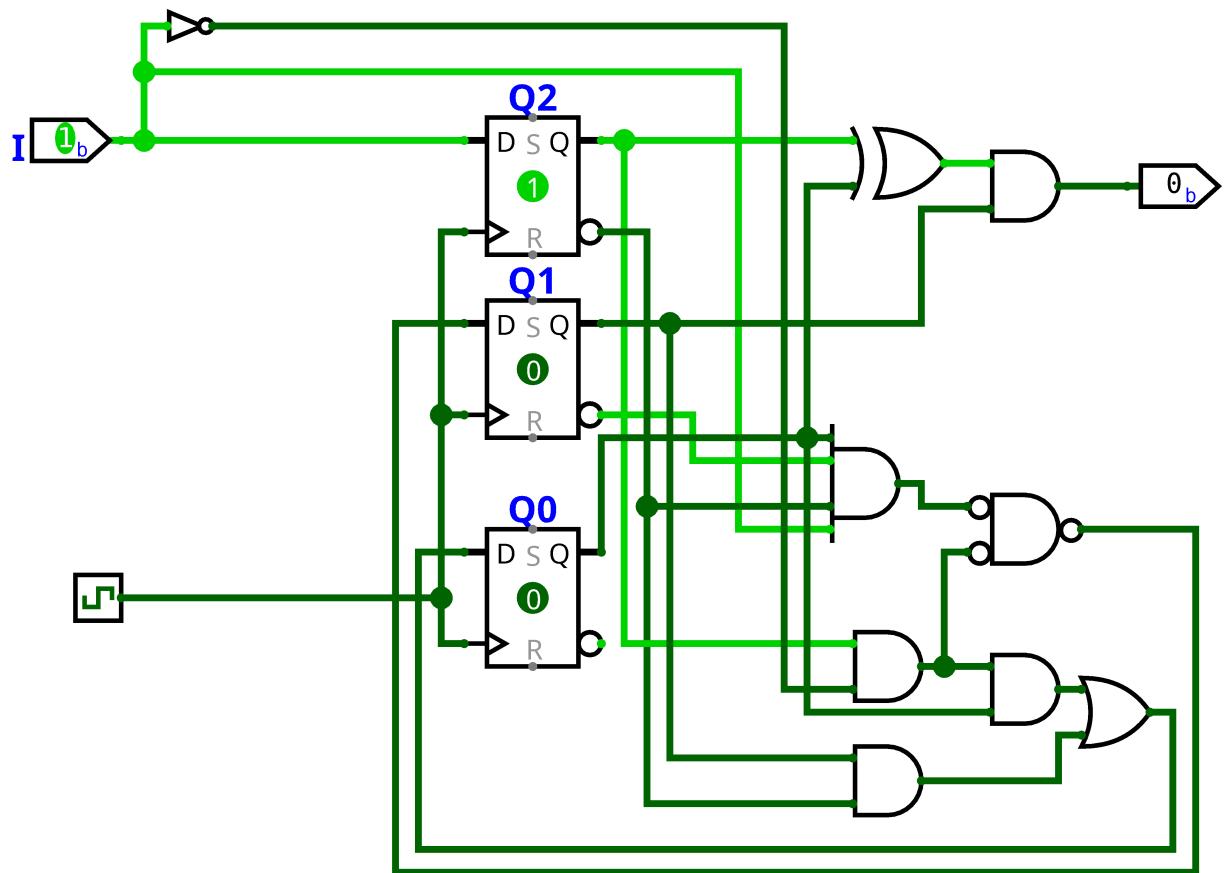


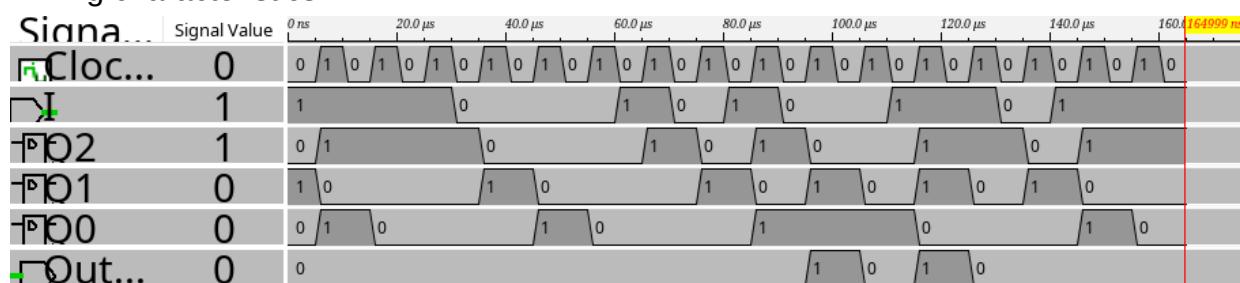
Lab 7 - More Sequential Circuit Analysis & Design

- Objective:
 - Design and simulate a sequential logic circuit using flip-flops
 - Analyze the logic diagram of a sequence detector and determine:
 - Mealy or Moore device
 - What is the code sequence
 - What are the timing characteristics
 - Design & implement a sequence detector that detects two sequences
 - UNLOCK should be asserted for whenever the last four inputs are either:
 - 1101
 - 1010
 - Include:
 - State diagram
 - State table
 - Boolean equations
 - Labeled logic diagram
 - Design the circuit as both a Moore and Mealy device
 - Analyze advantages/disadvantages of each device:
 - Hardware requirements
 - Memory
 - Timing
 - Security
 - Ease of design
 - Figure #1 Circuit Diagram Analysis

- Circuit Diagram:

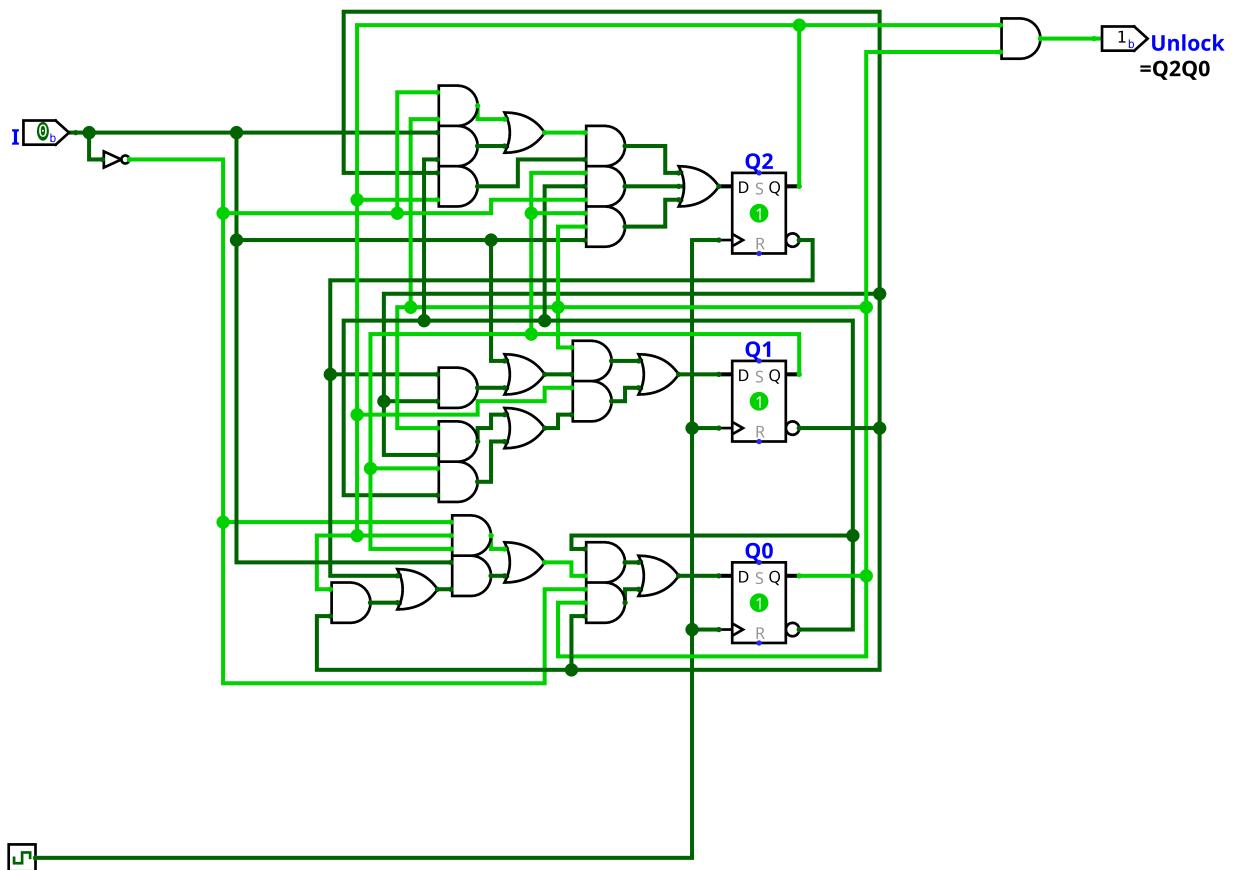


- This circuit is a Moore device, as the input does not directly affect the status of the output
- The code sequence for unlocking this circuit appears to be 1010
- Timing characteristics:



- Sequence detector:

- Moore Implementation:



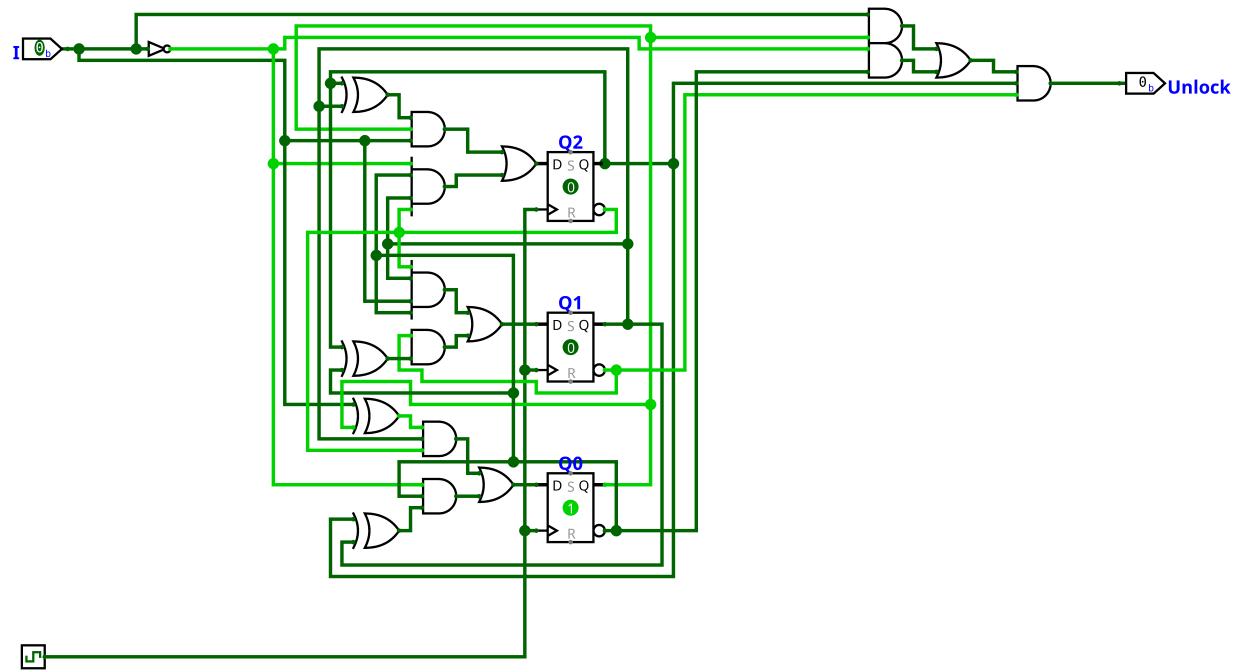
- See attached PDF of hand notes

- Timing Diagram:

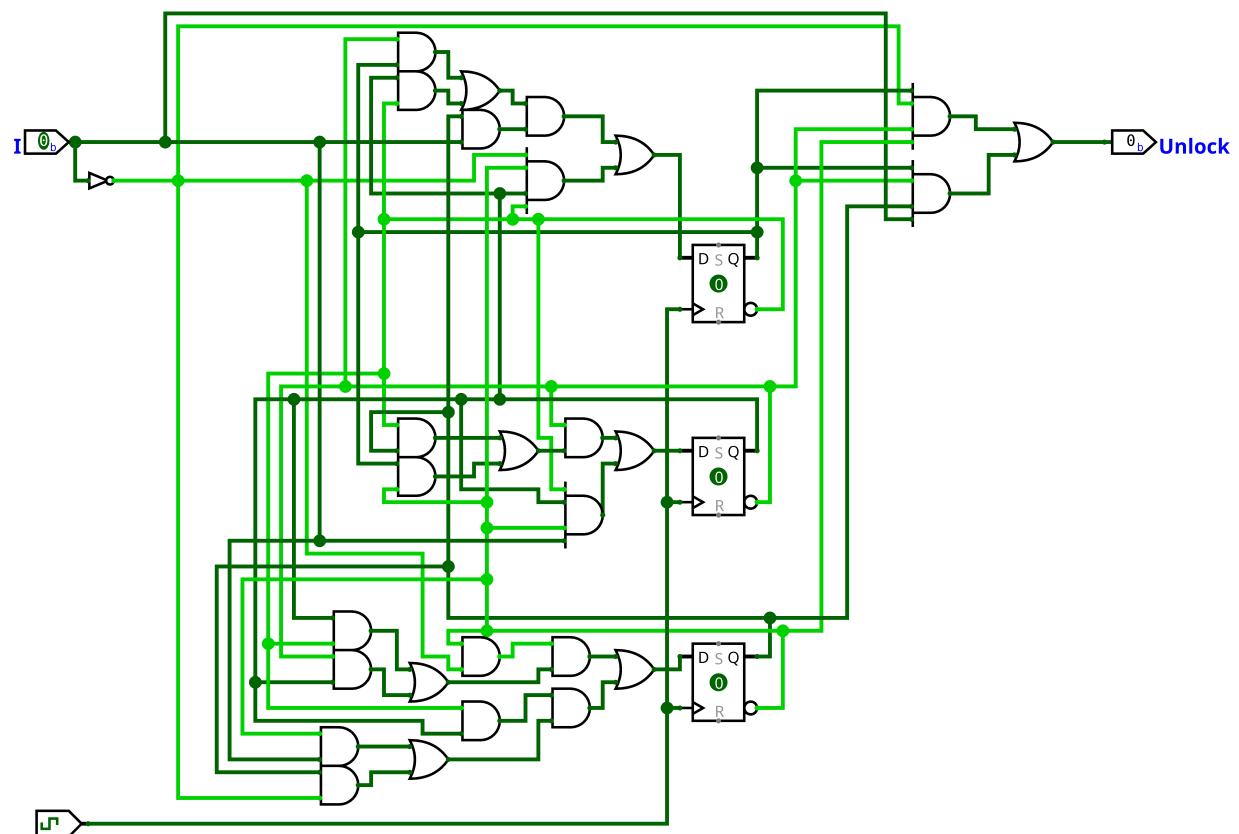
The timing diagram illustrates the logic levels of six signals over time. The horizontal axis represents time from 0 ns to 180.0 μs. The vertical axis lists the signals: Clock(40,...), I, Q2, Q1, Q0, and Unlock. The Clock signal is a standard square wave. The I signal has a pulse at approximately 25.0 μs. The Q2, Q1, and Q0 signals show a sequence of states between 0 and 1. The Unlock signal is low throughout the entire period.

- Mealy Implementation:
 - See attached

- Version 1:



- Version 2:



- Timing Diagram for version 1 implementation:

