Lab 6: Sequential Circuit Design

PURPOSE

The purpose of this lab is to design and simulate a simple sequential logic circuit using flip-flops.

Spin Direction Detector

Consider a system which consists of a spinning circular disk and stationary probes A (at 12 o'clock on the disk frame) and B (at 3 o'clock on the disk frame). One half of the disk is black and causes a probe to register the value 1 when the portion of the disk passes beneath it. The other half of the disk is white and causes a probe to register the value 0 when the portion of the disk passes beneath it. Your goal is to design a digital system that determines if the disk is spinning clockwise or anti-clockwise. The system has three **synchronous** inputs (A, B and ENABLE) and the two **moore** outputs (VALID and DIRECTION) that must realize the following operational characteristics:

- When the disk is spinning at full speed ENABLE is asserted (1). While enabled, the clock frequency will be high enough to guarantee that the disk is sampled 8 times per rotation. Otherwise (when the disk is stopped or changing direction), the external system holds ENABLE low (0).
- The value of the DIRECTION should be low (0) if the direction of the spin is counter-clockwise. The value of DIRECTION should be high (1) if the direction of spin is clockwise. The value of DIRECTION output is ignored (and thus can be treated as don't care) until valid is asserted.
- Whenever ENABLE is low or when ENABLE is high and the DIRECTION is not yet valid, the output VALID is held low (0). Once the direction of the spin is determined (and the value of direction set accordingly) VALID should be asserted.
- Once the VALID is asserted, the outputs should be held stable until ENABLE goes low.

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- [3 points] Design a state diagram for this machine. Include timing diagrams that demonstrate the functionality of your state machine. Attempt to make your design in a minimum number of states.
- [2 points] Make a reasonable state assignment (use the guidelines discussed in class) and construct the state table using these assignments for this state machine. Determine input (excitation) equations using D-type flip-flops for the state memory.
- [1 points] Implement this design using the lab simulator. Draw or print a schematic for the circuit using D-type flip-flops with the SSI and MSI parts of your choice for the next state and output logic. Provide complete documentation for this schematic.

LAB 6 - DEMONSTRATION

[2 points] Demonstrate the correct operation of your clocked synchronous state machine design. Completely verify the operation of the circuit or simulation to your laboratory instructor. Be prepared to answer questions regarding your documentation and the design process.

Integrated Writing [2 points]: Refer to "Digital System Design: Engineering Journals & Lab Policies" for details. 0.5 points each for Completeness, Clarity, Organization, and Testing.