Spring 2019: Advanced Topics in Numerical Analysis: High Performance Computing Assignment 5 (due Apr. 29, 2019)

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1. **MPI ring communication.**

   The C++ program `int_ring.cpp` sends an array of integers around each processor with each processor adding its rank to every element of the array. We "loop" over all of the processors `Nrepeat` times. By the end every element of the array should have the value

   $$\texttt{Nrepeat} \times \frac{\texttt{size} \times (\texttt{size} - 1)}{2}$$

   where `size` is the number of processors. The program can by run with the command

   ```
   mpirun -np 4 ./int_ring
   ```

   with 4 being the number of processors. We loaded the following modules on a CIMS desktop:

   - `gcc-8.1`
   - `mpi/openmpi-x86_64`

   The program was tested on a CIMS desktop with a Intel(R) Core(TM) i7-6700 CPU @ 3.40GHz processor and 4 cores. The table below shows the estimated latency and bandwidth for a different number of processors.

`size`	Latency (ms)	Bandwidth (GB/s)
2	8.57 e-04	1.18 e+00
3	9.52 e-04	7.88 e-01
4	1.22 e-03	5.64 e-01

Table 1: The estimated latency and bandwidth on a CIMS desktop. `Nrepeat` $= 10000$, and the length of the array of integers was 2^{18}, which has a size of approximately 2MB.

2. **Details regarding our final project.**

Project: Parallel KMC		
Week	Work	Who
04/15-04/21	Read paper. Start thinking about implementation.	Anya, Terrence
04/22-04/28	Write pseudo-code. Discuss boundary communication and time updating between blocks and sectors. Write up weekly plan.	Anya, Terrence
04/29-05/05	Implement 1 block for 1D. Compare to 1D serial and PDE (error for different L, β). Implement multiple blocks and compare.	Anya (first item), Terrence (third item)
05/06-05/12	Fix 1D bugs. Check 2D serial. Start 2D implementation for 1 and multiple blocks. Compare to PDE.	Anya (second item), Terrence (third item)
05/13-05/19	Fix bugs. Run scalability tests. Work on presentation slides and report.	Anya, Terrence