Clock constrained at 12.5 ns period (i.e. 80 MHz max clock)

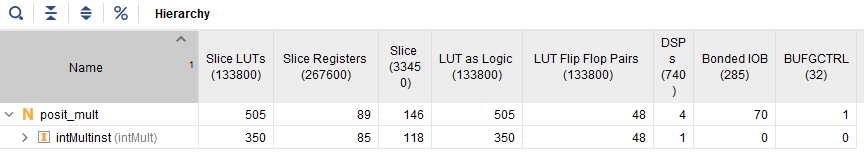
**Latency :**

3 clock cycles

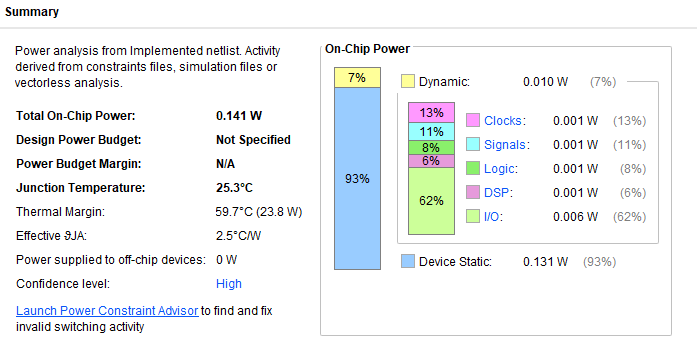
**Min Clock Period**

12.5 ns – 9.777 ns = 2.723 ns

**Utilization**

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**Power**

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