



# Welcome to The Hardware Lab!

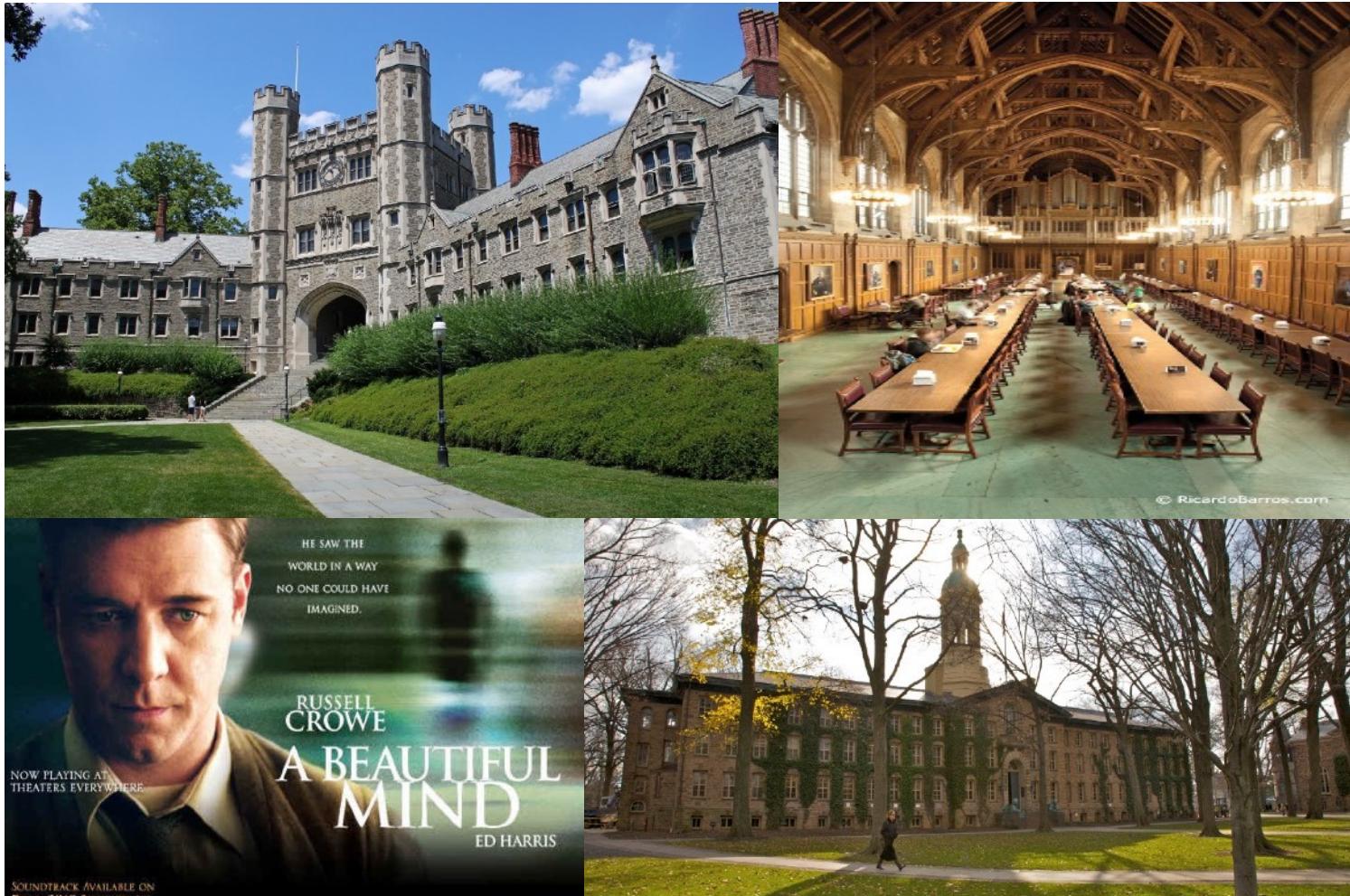
Fall 2018  
Course Syllabus

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Department of Computer Science  
National Tsing Hua University

# Where am I from

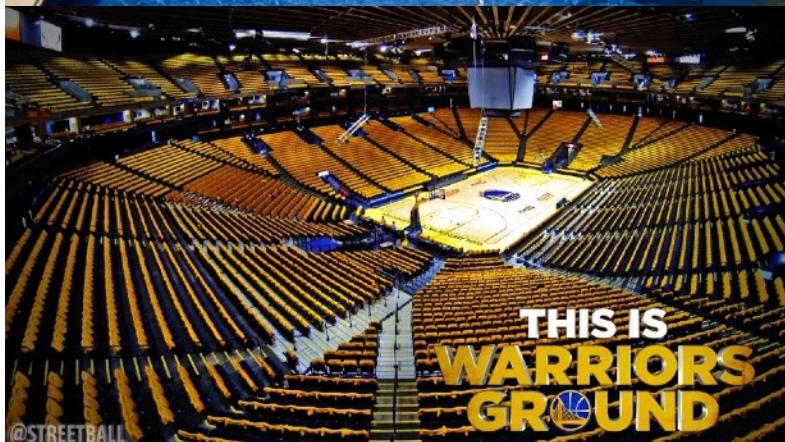
➤ Princeton University



\*Pictures cited from Princeton University and Google for education purpose only

# Where did I work

- Oracle America, Inc., U.S.A.



\*Pictures cited from Oracle America, Inc. and Golden State Warriors for education purpose only

# Course Information

- **Location & time:** 台達105 (lecture, T7T8)  
資電326 & 328 (lab, R7R8)
- **Course website**
  - NTHU digital learning system (<http://lms.nthu.edu.tw>)
- **Your TAs**
  - 林士軒、洪曼峯、曾楷恩、林楷宸
- **Prerequisite courses**
  - Digital logic design or equivalent

# Why Hardware Design Lab?

- Hardware-software **SHOULD BE** engineered together



# Your Goal

- Hands-on experience of digital logic design using Verilog & FPGA

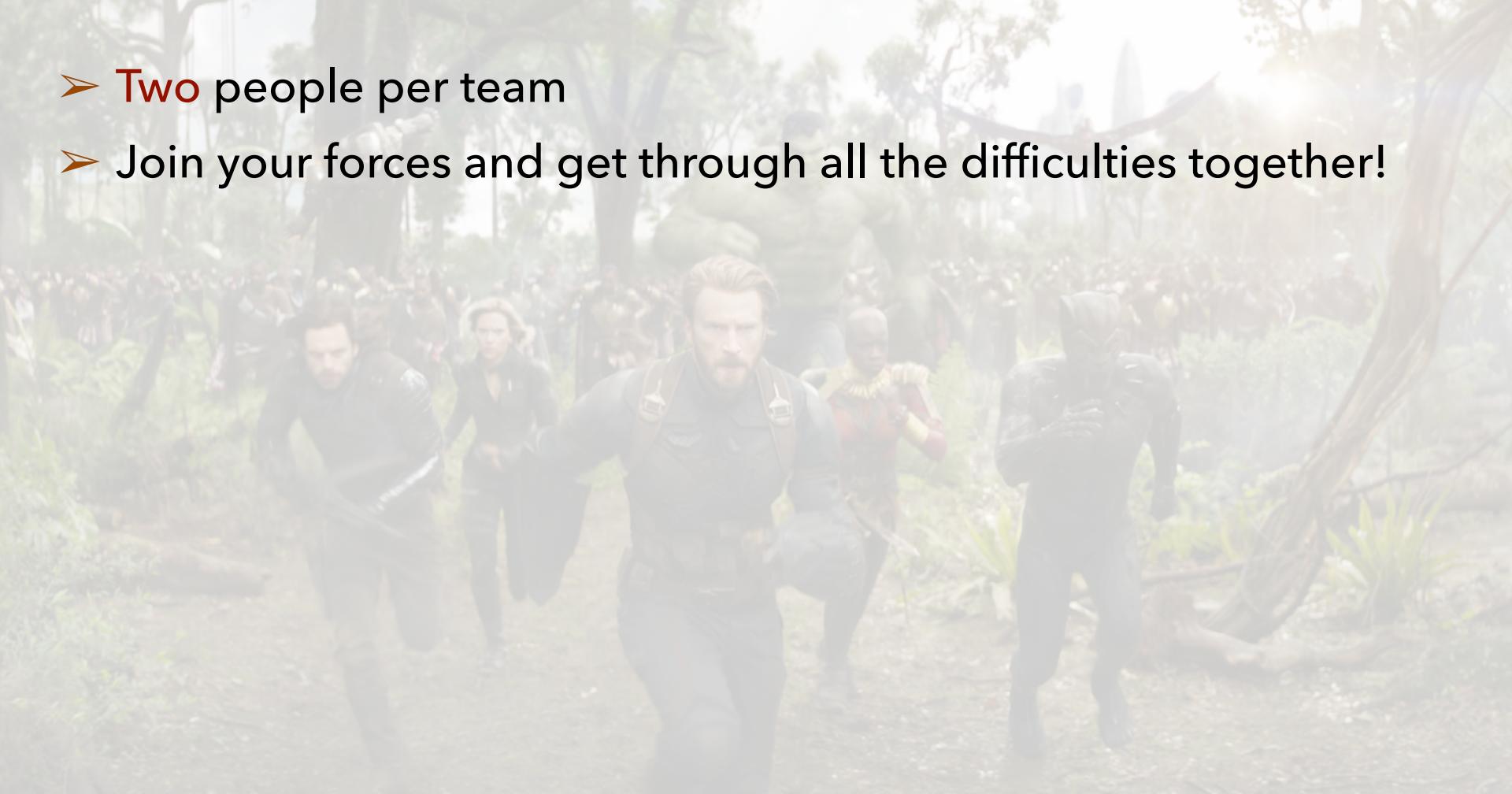


\*Pictures cited from Oracle America, Inc. and Marvel.com for education purpose only

# What We Will Do

- Twelve lab assignments (40%)
  - Six basic labs (**Individual**)
  - Six advanced labs (**Group**)
- One final project (20%)
- One mid-term exam (20%)
- One final exam (20%)

# Team Up!

- 
- A group of five Marvel superheroes are shown running through a dense jungle. In the foreground, Captain America leads the team, followed by Iron Man, Black Panther, Shuri, and Hawkeye. They are all in dynamic, forward-leaning poses, suggesting they are in the middle of a fast-paced chase or battle. The background is filled with lush green trees and foliage, with sunlight filtering through the canopy.
- Two people per team
  - Join your forces and get through all the difficulties together!

# Lab Assignments

- **Twelve** lab assignments in total
  - **Six** basic labs for learning Verilog & logic design
  - **Six** advanced labs for advanced Verilog design questions and FPGA implementations
- Things to submit
  - Demonstration of your work
  - Your source codes and testbenches
  - Lab report
- Responsibility
  - Each person will be responsible for one FPGA board

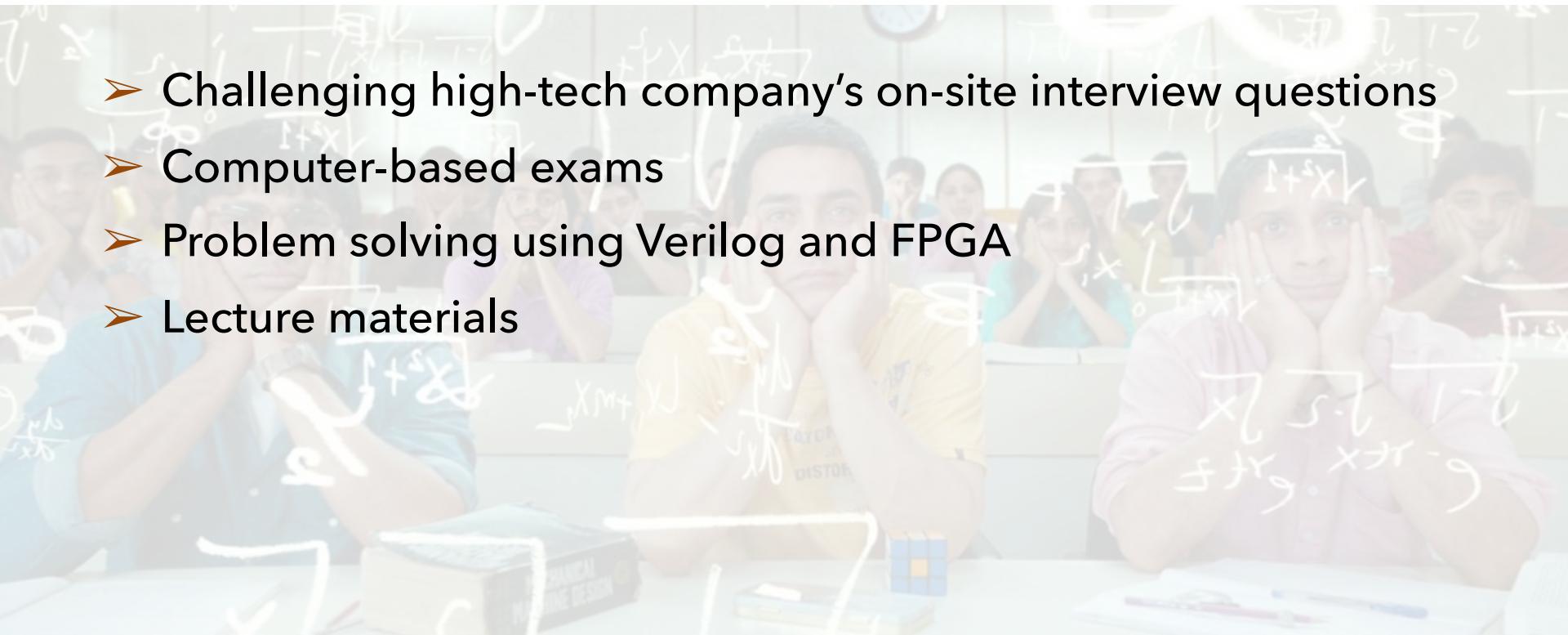


# Our Final Project

- The topic is decided by each team. Be creative!
- Grading rules
  - Final project proposal (5%) (due on 12/4)
  - Presentation (45%)
  - Project report (50%)

# Our Mid-Term and Final Exams

- Challenging high-tech company's on-site interview questions
- Computer-based exams
- Problem solving using Verilog and FPGA
- Lecture materials

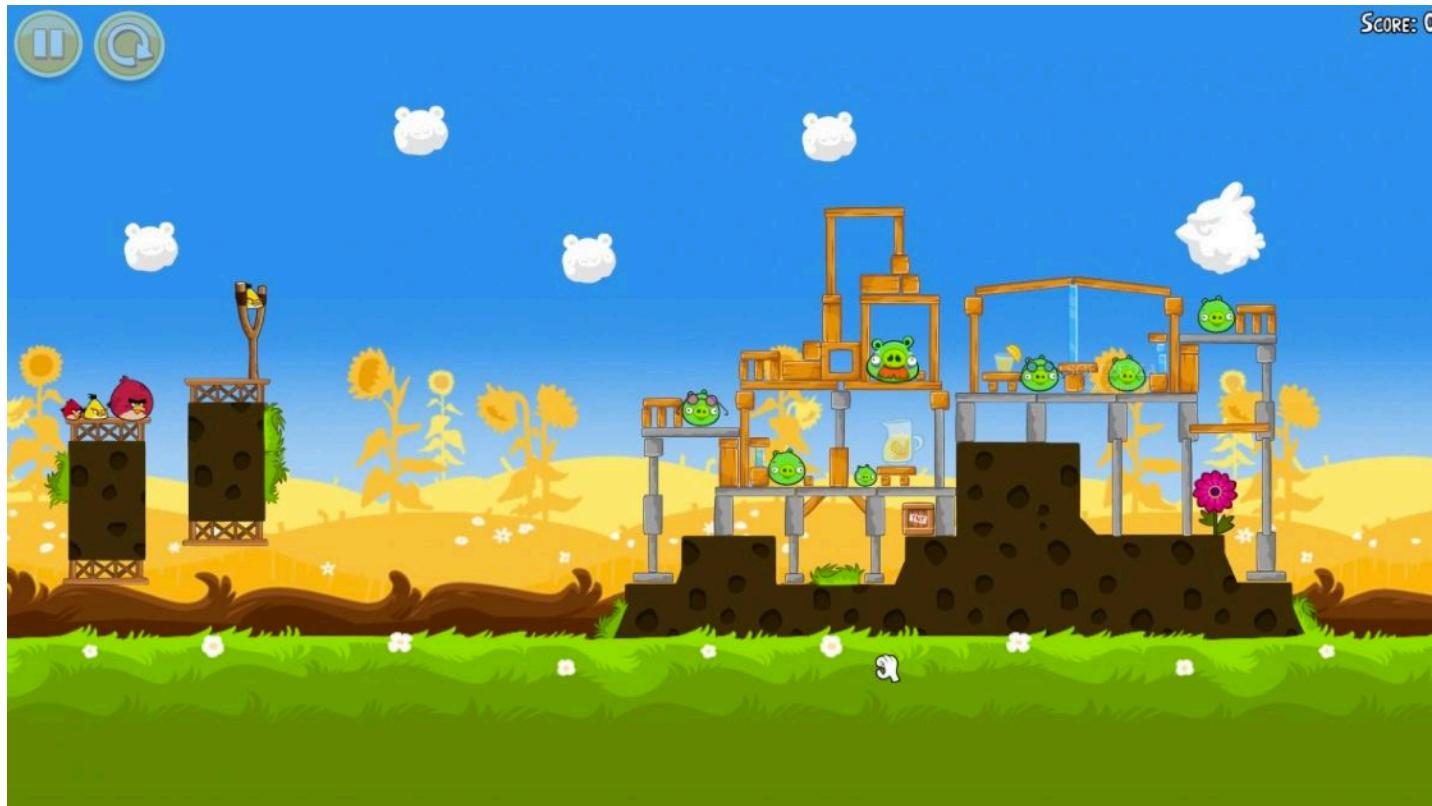


# Our Course Facts

- Late submission policy
  - You have a total of **TWO** late day through the semester for late submission
  - Once you use up, late submission will **NOT BE** accepted
- Roll call
  - Lab: Signup sheet after your demonstration (you **MUST** show up)
  - Lecture: Randomly
- Honor code
  - **NO MERCY** on cheating or copying.
  - If you do, you will get **ZERO** point for the first time.
  - You will **FAIL** this course directly at the second time

# Special Challenge

- Angry bird
  - You will get A+ if you can implement **exactly the same game** on FPGA using Verilog
- The whole class will judge it together



# Our Course Schedule

Week	Date	Tuesday	Thursday
1	9/11, 9/13	Syllabus	Lab 1 Basic Demo
2	9/18, 9/20	<ul style="list-style-type: none"><li>• Introduction to Verilog</li><li>• FPGA Implementation</li></ul>	Lab 1 Advanced Demo
3	9/25, 9/27	Data Flow and Data Types	Lab 2 Basic Demo
4	10/2, 10/4	Behavior Modeling	Lab 2 Advanced Demo
5	10/9, 10/11	Sequential Circuits (I)	Lab 3 Basic Demo
6	10/16, 10/18	Labs 1~3 Review	<b>Midterm Exam</b>
7	10/23, 10/25	Sequential Circuits (II)	Lab 3 Advanced Demo
8	10/30, 11/1	Finite State Machines	Lab 4 Basic Demo
9	11/6, 11/8	Moore and Mealy Conversion	Lab 4 Advanced Demo
10	11/13, 11/15	Keyboard and Audio Tutorial	Lab 5 Basic Demo
11	11/20, 11/22	Verilog Coding Styles	Lab 5 Advanced Demo
12	11/27, 11/29	VGA and Mouse Tutorial	Lab 6 Basic Demo

# Our Course Schedule (Cont'd)

Week	Date	Tuesday	Thursday
13	12/4, 12/6	<ul style="list-style-type: none"><li>Final project proposal due (12/4)</li><li>Labs 3~5 Review</li></ul>	<b>Final Exam</b>
14	12/11, 12/13	Logic Design Flow	Lab 6 Advanced Demo
15	12/18, 12/20	Other Interesting Topics	
16	12/25, 12/27	Course Wrap Up	<b>Final Project Period</b>
17	1/1, 1/3	New Year's Day (No Lecture)	
18	1/11 (Fri)	<b>Final Project Demo + Final Project Report Due</b>	
Happy winter break and Chinese new year!			

# Start Earlier!

- Read Dr. D J Greaves' (Cambridge University) guide to Verilog
  - <http://www.cl.cam.ac.uk/~djh11/teaching/learners.pdf>
- Getting started with Vivado and Basys3
  - [https://www.youtube.com/watch?v=6\\_GxkSlqbcU](https://www.youtube.com/watch?v=6_GxkSlqbcU)
  - Try to get familiar with Vivado and Basys3



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# Thank you for your attention!



\*The Golden Gate Bridge night view taken at Hawk Hill.  
This picture is taken by Chun-Yi Lee himself, who is also a fan of photography