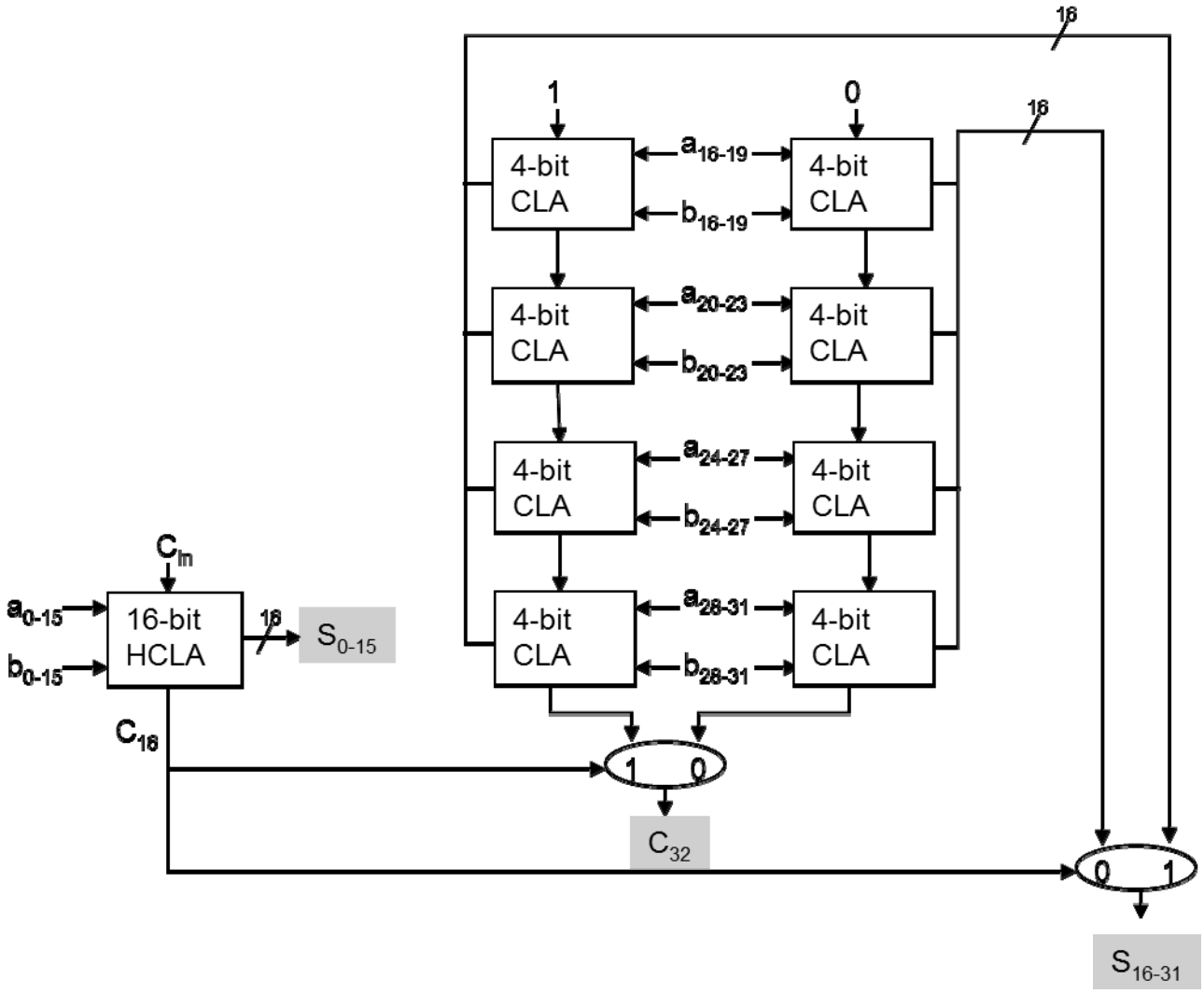
Assume for the rest of this problem that all logic gates have the following delays:

Fan In	Delay
1	T
2	2T
3	3T
4	5T
5	7T
6	10T
7 or more	2T x fan-in

So a 2-input AND gate would have delay 2T and a 4-input OR gate would have delay 5T.

For simplicity, assume that mux's have delay 4T regardless of fan-in.

We will create a 32-bit adder out of some building blocks we've covered in class. We will use the 4-bit CLA that we covered in class as one basic building block of this design. And we will use it (as we did in class) to make 16-bit hierarchical CLAs (HCLA) which will be our other building block. But instead of connecting these in series to make a 32-bit adder, we will use carry select to speed up the 32-bit adder. The design will look as follows (be sure to note where we are using CLAs and where we are using HCLAs):


16
1
0
16
4-bit CLA
4-bit CLA
a_{16-19}
b_{16-19}
4-bit CLA
4-bit CLA
a_{20-23}
b_{20-23}
4-bit CLA
4-bit CLA
a_{24-27}
b_{24-27}
4-bit CLA
4-bit CLA
a_{28-31}
b_{28-31}
C_{in}
a_{0-15}
b_{0-15}
16-bit HCLA
16
S_{0-15}
C_{16}
1 0
C_{32}
0 1
S_{16-31}

Your task is to find the maximal delay of this design – i.e. determine the delays of $S_{0\text{-}31}$ and C_{32} – the maximal delay of these outputs will be the maximal delay of the design. Fill in the values in the table on the following page to receive full credit (and to help with possible partial credit).

Output	Delay	
G0	2T	*(2 points)*
P0	2T	*(2 points)*
Gα	12T	*(2 points)*
Pα	7T	*(2 points)*
C12	20T	*(2 points)*
C15	30T	*(2 points)*
C16	24T	*(2 points)*
S15	32T	*(2 points)*
C20	16T	*(2 points)*
S19	14T	*(2 points)*
C24	30T	*(2 points)*
C31	54T	*(2 points)*
C32 (after mux)	62T	*(2 points)*
S31 (after mux)	60T	*(2 points)*

Find the maximum delay **in terms of T** of the 32-bit adder – take the maximum of all output bits – including the sum bits (S_0-S_{31}) and the final carry out (C_{32}). Show your work clearly in the table above. The two figures on the following pages are taken from the class notes, if you need to refer to them.

Maximal Delay: 62T *(2 points)*

G0: 2T is just a two-input AND gate delay of 2 inputs which are both ready at start
P0: same as G0, delay of a two-fan-in OR gate

Ga: Ga = G3 + G2P3 + G1P2P3 + G0P1P2P3
all G and P are ready at 2T, so the maximum delay is G0P1P2P3 = 2T + 4-input-delay = 7T
the total delay is 7T + 4-input-delay = 12T

Pa: Pa = P0P1P2P3
all entries are available at 2T, so total delay is 2T + 4-input-delay = 7T

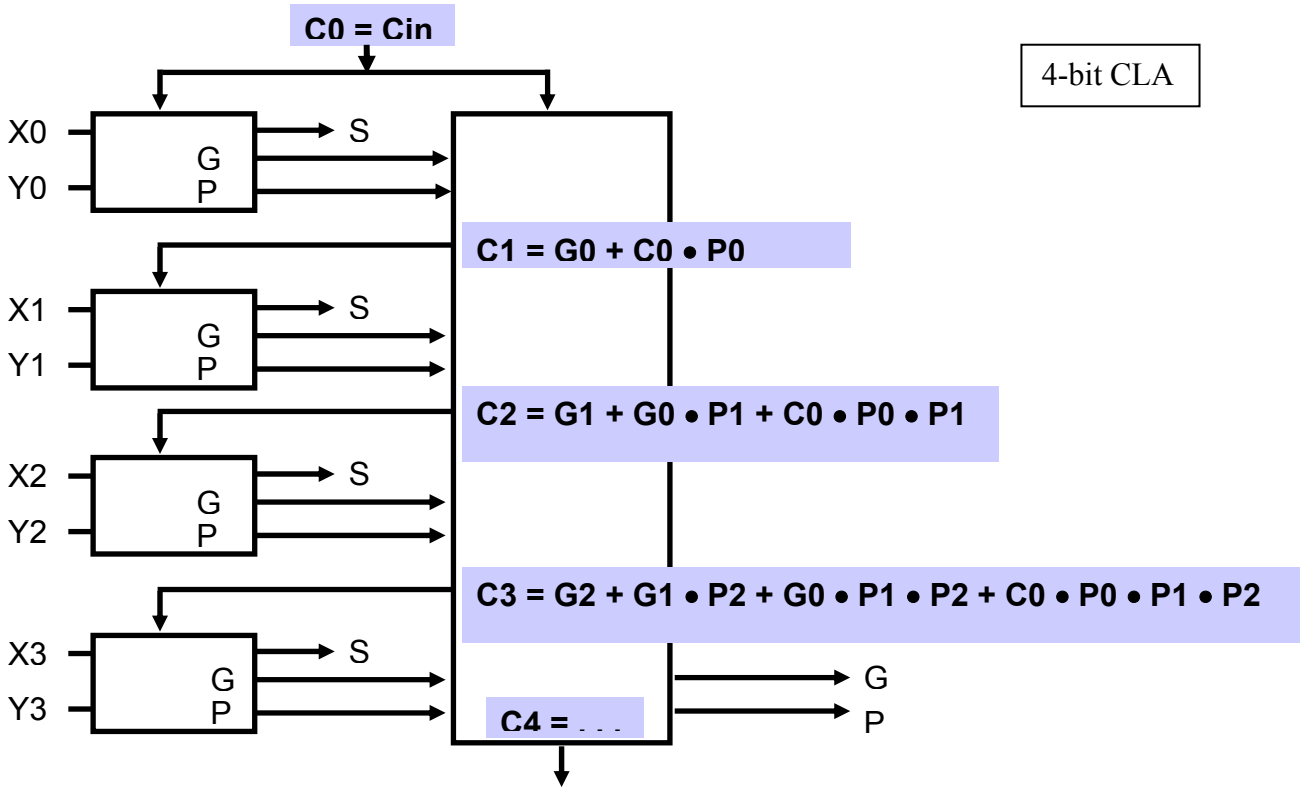
C12: C12 = Gy + GbPy + GaPbPy + C0PaPbPy
all G are ready at 12T and all P are ready at 7T
so the maximum wait time is for GaPbPy = 12T + 3-input-delay = 15T
total delay is 15T + 4-input-delay = 20T

C15: C15 = G14 + G13P14 + G12P13P14 + C12P12P13P14
it is obviously determined by C12P12P13P14 = C12 + 4-input-delay = 25T
total delay is 25T + 4-input-delay = 30T

C16: C16 = Go + Gy..... = Go + C12Po = C12 + 2-input-delay + 2-input-delay = 24T

S15: S15 = (a15 xor b15) xor C15
the delay of C15 is 30T
the total delay is 30T + xor-delay = 30T + 2T = 32T

C20: C20 = G19 + G18P19 + G17P18P19 + G16P17P18P19 + C0P0P1P2P3
every G and P are ready at 2T and C0 ready at start
total delay is 2T + 5-input-delay + 5-input-delay = 16T



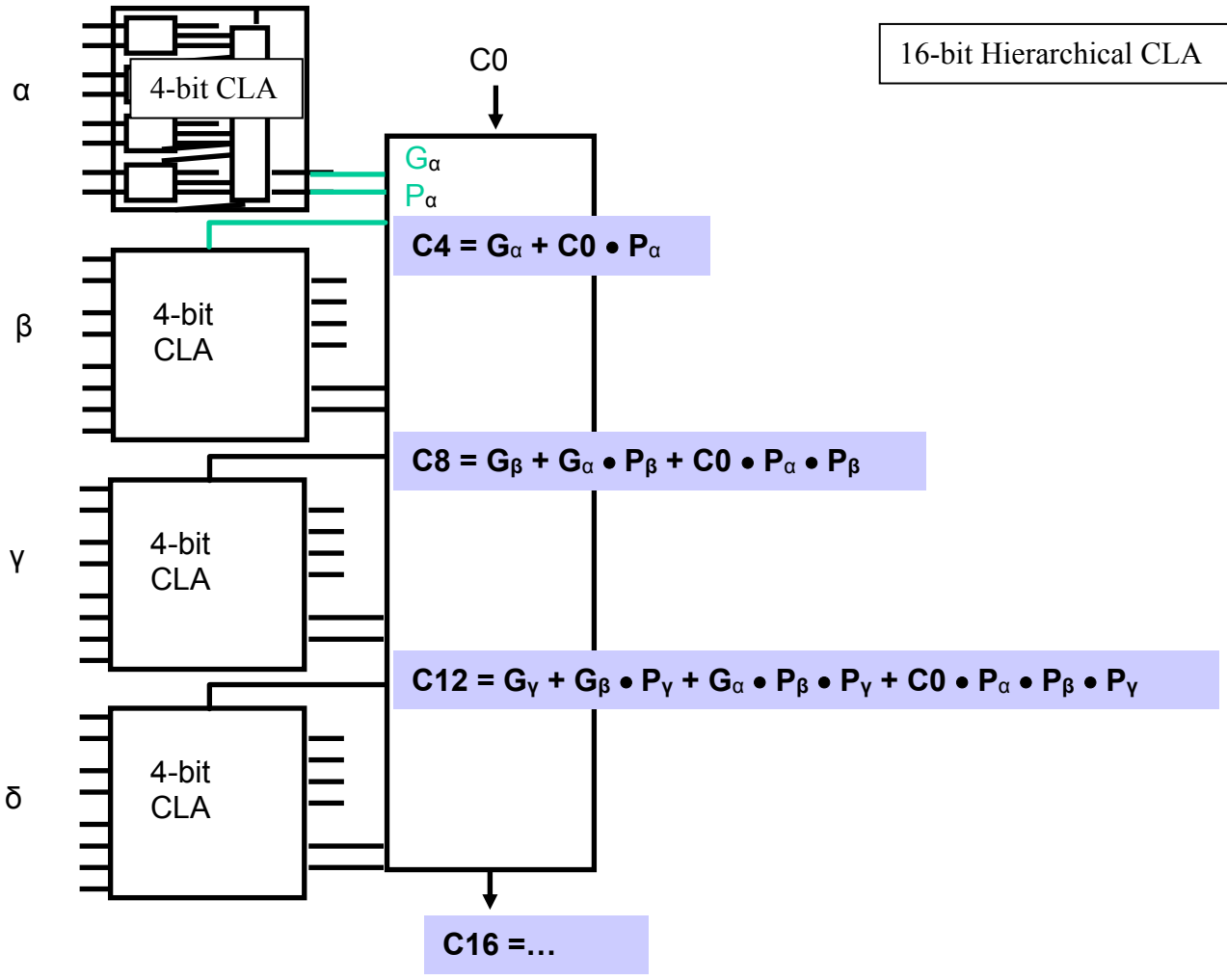
S19: S19 = (a19 xor b19) xor C19
C19 = G18 + G17P18 + G16P17P18 + C0P16P17P18
C19 is decided by C0P16P17P18 = 2T + 4-input-delay = 7T
C19 is available at 7T + 4-input-delay = 12T
S19 = 12T + xor-delay = 14T

C24: C24 = G23 + G22P23 + G21P22P23 + G20P21P22P23 + C20P20P21P22P23
this is determined by C20P20P21P22P23 = C20 + 5-input-delay = 23T
the total delay is 23T + 5-input-delay = 30T

C31: C31 = G30 + G29P30 + G28P29P30 + C28P28P29P30
C28 is similar as C24 = C24 + 14T = 44T
the total delay is 44T + 4-input-delay + 4-input-delay = 54T

C32(after mux):
C32 before mux is ready at C28 + 14T = 58T
C16 is ready at 24T.
the total delay is 58T + mux-delay = 62T

S31(after mux):
S31 before mux = (a31 xor b31) xor C31
S31 is ready at C31 + xor-delay = 56T
C16 is ready at 24T.
The total delay is 56T + 4T = 60T


16-bit Hierarchical CLA
α
4-bit CLA
C0
Gα
Pα
C4 = Gα + C0 • Pα
β
4-bit
CLA
C8 = Gβ + Gα • Pβ + C0 • Pα • Pβ
γ
4-bit
CLA
C12 = Gγ + Gβ • Pγ + Gα • Pβ • Pγ + C0 • Pα • Pβ • Pγ
δ
4-bit
CLA
C16 =…