CS M151B HW4

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1 4.7

1.1 4.7.1

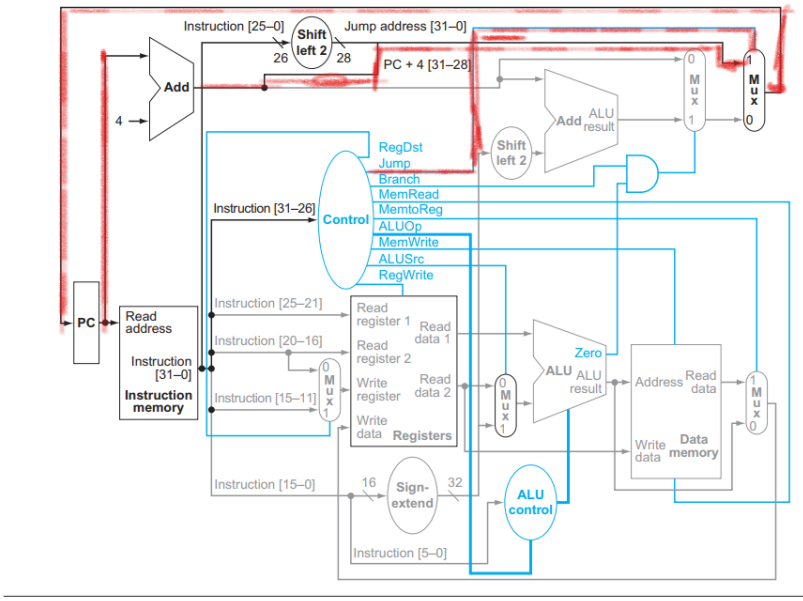
Sign extended: 0000 0000 0000 0000 0000 0000 0001 0100 Left shift 2; 0001 1000 1000 0000 0000 0101 0000

1.2 4.7.2

ALUop is 00 because sw instruction has to perform ADD. The last 6 bits of instruction is 010100

1.3 4.7.3

The new PC address is PC+4.



1.4 4.7.4

MUX for register write: don't care
The RegDst control value does not matter as there is no write to the register.

MUX for ALU input: 20
In sw instruction, immediate value is used to compute the memory address to write. So the last 16 digits is outputted and the value is 20.

MUX for register write data: don't care X
In sw instruction, there is no data to write in register.

MUX for PC: PC + 4
For sw instruction, there is no jump and branch so pc will just move to next instruction.

MUX for PC MUX: PC + 4

1.5 4.7.5

ALU: -3 and 20.
The first input comes from register rs. Rs is 3 and the value is r3 is -3.
The second input comes from sign extended 16-bit immediate value which is 20.

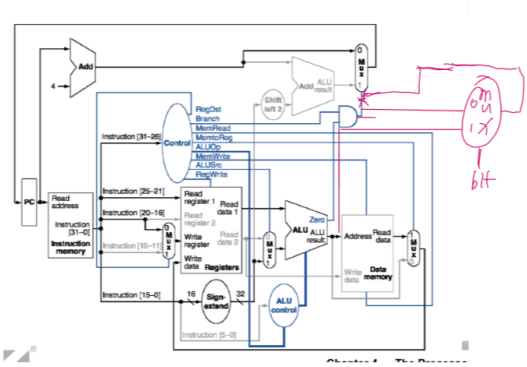
First adder on the left: PC and 4.

Second adder on the right: PC + 4 and 80.
The first input is PC+4, the second is the immediate value left shifted by 2 which is 20*4 = 80

1.6 4.7.6

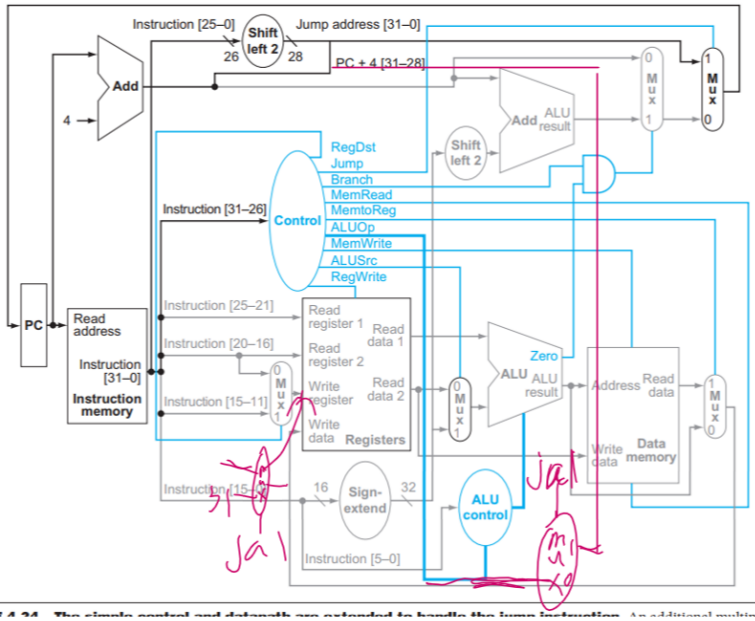
Read register 1: rs = 3
Read register 2: rt = 1
Write register: X
Write data: X
RegWrite: 0

2 blt

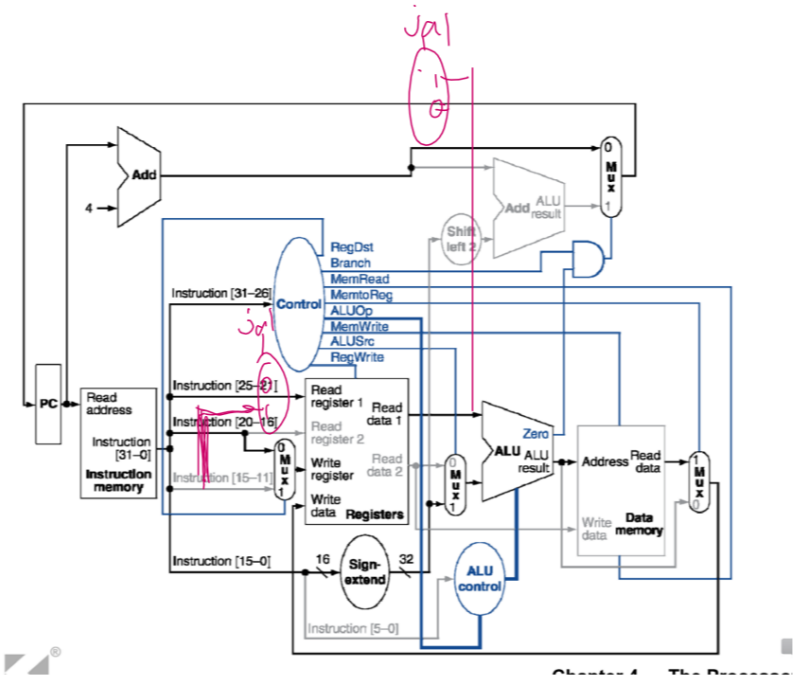


Modify the alu table so 11 forces a slt
Regdst: 0
Branch: 0
Memread: 0
Memtoreg: X
Memwrite: 0
Aluop: 11
Alusrc: 0
Regwrite: 0

3 jal



4 jr


Add
4
PC
Read address
Instruction [31–0]
Instruction memory
Instruction [31–26]
Instruction [25–0]
Instruction [20–16]
Instruction [15–11]
Instruction [15–0]
Instruction [5–0]
Control
RegDst
Branch
MemRead
MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
Registers
16
Sign-extend
32
Shift left 2
Add
ALU result
Zero
ALU
ALU result
ALU control
Address
Read data
Write data
Data memory
M u x