

Teruo Tanimoto

Assistant professor of Research Institute for Information Technology, Kyushu University

Web: <http://ri2t.kyushu-u.ac.jp/~tteruo/>

Email: tteruo@kyudai.jp

Education

- Apr. 2015 – Mar. 2018 Ph.D. of Engeneering.
Kyushu University, Fukuoka
Advisor: Prof. Koji Inoue
- Apr. 2010 - Mar. 2012 Master of Information Science and Technology,
The University of Tokyo, Tokyo
Advisor: Prof. Hiroshi Nakamura
- Apr. 2006 - Mar. 2010 Bachelor of Engineering,
The University of Tokyo, Tokyo
Advisor: Prof. Hiroshi Nakamura

Work Experience

- Apr. 2018 – present Assistant professor of Research Institute for Information Technology, Kyushu University.
(Concurrently Cybersecurity Center, Kyushu University)
- Apr. 2015 – Mar. 2018 Research Assistant at Kyushu University
- Apr. 2012 – Mar. 2015 Researcher at Fujitsu Laboratories Limited, Kawasaki, Japan
I designed and prototyped both hardware and software for an inter-node communication system for UNIX server products.

Refereed Publications

1. Teruo Tanimoto, Takatsugu Ono, and Koji Inoue, "Dependence Graph Model for Accurate Critical Path Analysis on Out-of-Order Processors," IPSJ Journal of Information Processing, Vol.25, pp.983-992, Dec. 2017.
2. Teruo Tanimoto, Takatsugu Ono, and Koji Inoue, "CPCI Stack: Metric for Accurate Bottleneck Analysis on OoO Microprocessors," In Proceedings of the Fifth International Symposium on Computing and Networking (CANDAR '17), pp.166-172, Nov. 2017.
3. Hiroshi Sasaki, Fang-Hsiang Su, Teruo Tanimoto, and Simha Sethumadhavan, "Why Do Programs Have Heavy Tails?" In Proceedings of the 2017 IEEE International Symposium on Workload Characterization (IISWC '17), pp.135-145, Oct. 2017.
4. Teruo Tanimoto, Takatsugu Ono, Koji Inoue, Hiroshi Sasaki, "Enhanced Dependence Graph Model for Critical Path Analysis on Modern Out-of-Order Processors," IEEE Computer Architecture Letters, vol.16, no.2, pp.111-114, July-Dec. 2017.
5. Hiroshi Sasaki, Fang-Hsiang Su, Teruo Tanimoto, and Simha Sethumadhavan, "Heavy Tails in Program Structure," IEEE Computer Architecture Letters, vol.16, no.1, pp.34-37, Jan.-June 2016.

6. Takatsugu Ono, Yotaro Konishi, Teruo Tanimoto, Noboru Iwamatsu, Takashi Miyoshi and Jun Tanaka, “A Flexible Direct Attached Storage for a Data Intensive Application”, IEICE Transaction on Information and Systems, Vol.E98-D, No.12, pp.2168-2177, Dec. 2015.
7. Takatsugu Ono, Yotaro Konishi, Teruo Tanimoto, Noboru Iwamatsu, Takashi Miyoshi and Jun Tanaka, “FlexDAS: A Flexible Direct Attached Storage for I/O Intensive Applications”, In Proceedings of IEEE International Conference on Big Data (IEEE BigData ‘14), pp.147-152, Oct. 2014.
8. Teruo Tanimoto, Takatsugu Ono, Kohta Nakashima and Takashi Miyoshi, “Hardware-assisted Scalable Flow Control of Shared Receive Queue”, In Proceedings of the 28th ACM International Conference on Supercomputing (ICS ‘14), pp.175-175, Jun. 2014. (poster session)
9. Hiroshi Sasaki, Teruo Tanimoto, Koji Inoue, and Hiroshi Nakamura, “Scalability-based Manycore Partitioning”, In Proceedings of the 21st International Conference on Parallel Architectures and Compilation Techniques (PACT ‘12), pp.107-116, Sep. 2012.

Research Interests

Computer architecture, hardware/software co-design, interconnects, operating systems, hardware empowered computer security