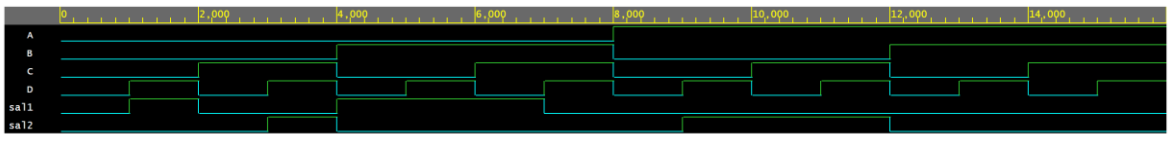
```
// Code your design here
module Circuit2(A,B,C,D,sal1,sal2);
  input A,B,C,D;
  output sal1,sal2;
  wire n1,n2,n3,n4,n5,n6,n7,n8,n9,n10;
  Not_gate u1(A,n1);
  Not_gate u2(B,n2);
  Not_gate u3(C,n3);
  Not_gate u4(D,n4);


  And_gate u5(n1,n3,D,n5);
  And_gate u7(n1,B,n3,n6);
  And_gate u6(n1,n4,B,n7);

  And_gate u10(A,n2,D,n8);
  And_gate u8(A,n2,C,n9);
  And_gate u9(n2,C,D,n10);


  Or_gate u12(n5,n7,n6,sal1);
  Or_gate u11(n8,n9,n10,sal2);
Endmodule
```

```
// Code your testbench here
// or browse Examples
`timescale 1ns/1ps
`include "Not_gate.sv"
`include "And_gate.sv"
`include "Or_gate.sv"

module Circuit2_TB;
  reg A,B,C,D;
  wire sal1;
  wire sal2;


  Circuit2 UUT(A,B,C,D,sal1,sal2);

  initial
    begin
      $dumpfile("Circuit2.vcd");
      $dumpvars(1,Circuit2_TB);
      A=1'b0;
      B=1'b0;
      C=1'b0;
      D=1'b0;
            #1
      A=1'b0;
      B=1'b0;
      C=1'b0;
      D=1'b1;
            #1
```

```
A=1'b0;
B=1'b0;
C=1'b1;
D=1'b0;
    #1
A=1'b0;
B=1'b0;
C=1'b1;
D=1'b1;
    #1
A=1'b0;
B=1'b1;
C=1'b0;
D=1'b0;
    #1
A=1'b0;
B=1'b1;
C=1'b0;
D=1'b1;
    #1
A=1'b0;
B=1'b1;
C=1'b1;
D=1'b0;
    #1
A=1'b0;
B=1'b1;
C=1'b1;
D=1'b1;
```

```
        #1
A=1'b1;
B=1'b0;
C=1'b0;
D=1'b0;
        #1
A=1'b1;
B=1'b0;
C=1'b0;
D=1'b1;
        #1
A=1'b1;
B=1'b0;
C=1'b1;
D=1'b0;
        #1
A=1'b1;
B=1'b0;
C=1'b1;
D=1'b1;
        #1
A=1'b1;
B=1'b1;
C=1'b0;
D=1'b0;
        #1
A=1'b1;
B=1'b1;
C=1'b0;
```

```
  D=1'b1;
        #1
  A=1'b1;
  B=1'b1;
  C=1'b1;
  D=1'b0;
        #1
  A=1'b1;
  B=1'b1;
  C=1'b1;
  D=1'b1;
        #1
  $finish;
 end
endmodule;
```



Note: To revert to FPWave opening in a new browser window, set that option on your user page.

17	Ortega Blanco, Christian Aaron	$f1 = \sum(1,4,5,6)$ $f2 = \sum(3,9,10,11)$