Practica #1

Expresión bool;

AB+BC

Entidad;

```
// Code your design here
module And_Gate(input A,input B,input C, output D);
  assign D=(A&B)|(B&C);
endmodule


arquitectur// Code your testbench here
// or browse Examples
`timescale 1ns/1ps
module And_Gate_TB;
  reg A,B,C;
  wire D;

  And_Gate UUT(.A(A),.B(B),.C(C),.D(D));

  initial
    begin
      $dumpfile("And_Gate2.vcd");
      $dumpvars(1,And_Gate_TB);
      // 00
      A=1'b0;
      B=1'b0;
      C=1'b0;
      #1
      A=1'b1;
      B=1'b0;
```

```
  C=1'b0;
  #1
  A=1'b0;
  B=1'b1;
  C=1'b0;
  #1
  A=1'b1;
  B=1'b1;
  C=1'b0;
  #1
  A=1'b0;
  B=1'b0;
  C=1'b1;
  #1
  A=1'b1;
  B=1'b0;
  C=1'b1;
  #1
  A=1'b0;
  B=1'b1;
  C=1'b1;
  #1
  A=1'b1;
  B=1'b1;
  C=1'b1;
  #1
  $finish;
 end
endmodulea;
```