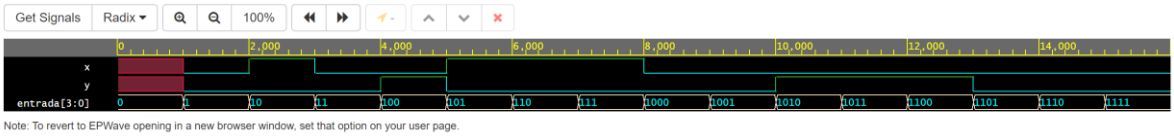


```
// Code your design here

module And_Gate(input [3:0] entrada,output [1:0] salida);


  assign salida[0]=
(~entrada[3]&~entrada[2]&~entrada[1]&entrada[0])|(~entrada[3]&entrada[2]&~entrada[1]&~ent
rada[0])|(~entrada[3]&entrada[2]&~entrada[1]&entrada[0])|(~entrada[3]&entrada[2]&entrada[1]
&~entrada[0])?1:0;

  assign salida[1]=
(~entrada[3]&~entrada[2]&entrada[1]&entrada[0])|(entrada[3]&~entrada[2]&~entrada[1]&entra
da[0])|(entrada[3]&~entrada[2]&entrada[1]&~entrada[0])|(entrada[3]&~entrada[2]&entrada[1]&
entrada[0])?1:0;

endmodule



// Code your testbench here

// or browse Examples

`timescale 1ns/1ps

module And_Gate_TB;

  reg [3:0] entrada;

  wire [1:0] salida;

  integer i;

  reg x;

  reg y;

  And_Gate UUT(entrada ,salida);


  initial


begin
```

```
  for (i=0; i <16; i=i+1)
   begin

    entrada = i;
     x=salida[0];
     y=salida[1];
    #1;
   end

  $finish();
end

 initial begin
    $dumpvars;
    $dumpfile("dump.vcd");
  end

endmodule
```