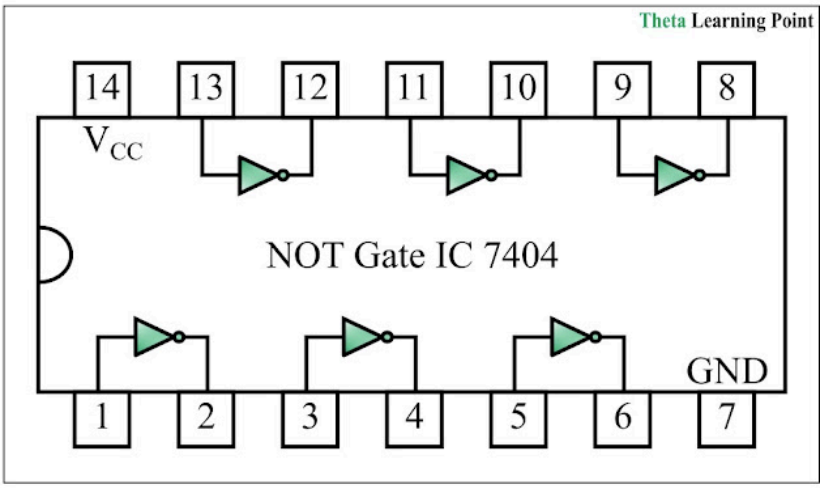
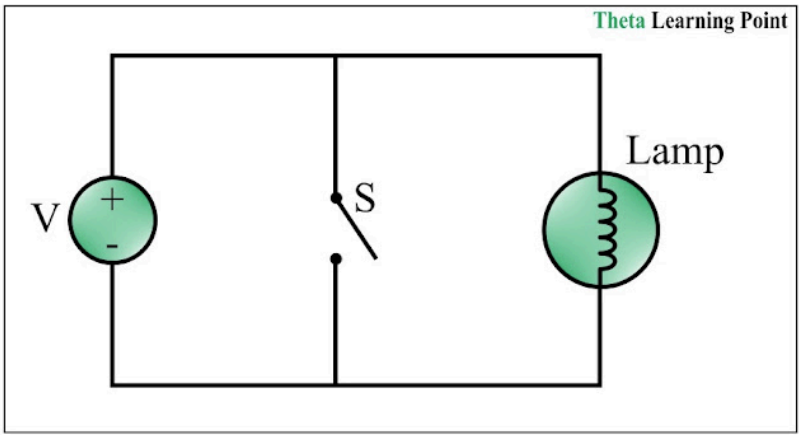
1) Experiment number 3:

Diagram NOT GATE

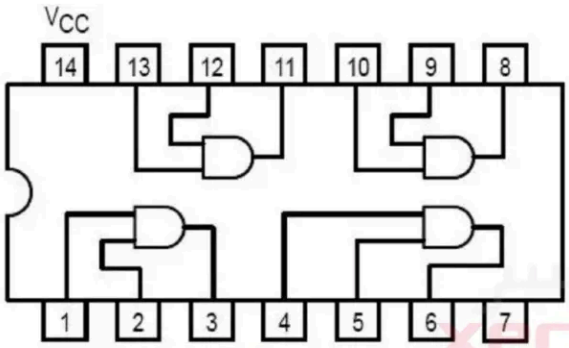
Input	Output
A	Y = A`
0	1
1	0



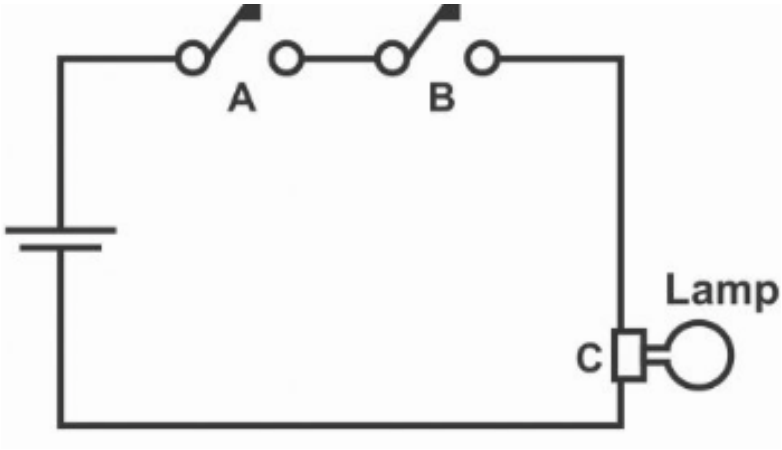


AND GATE

Input	Input	Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



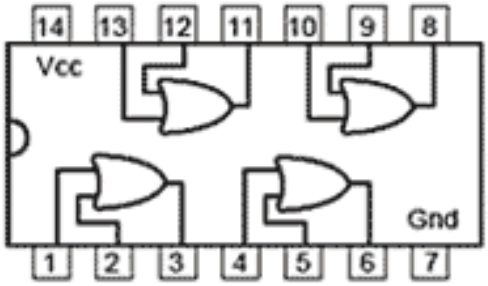
7408 Pinout



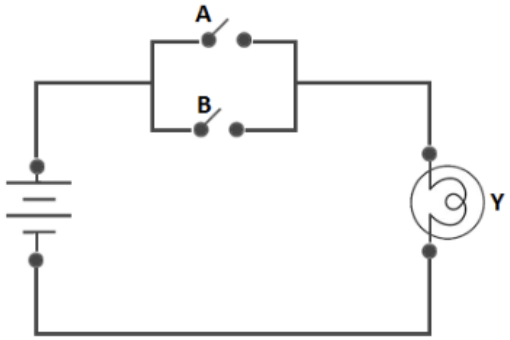
OR GATE

A	B	Y = A + B
0	0	0
0	1	1
1	0	1
1	1	1

Truth Table



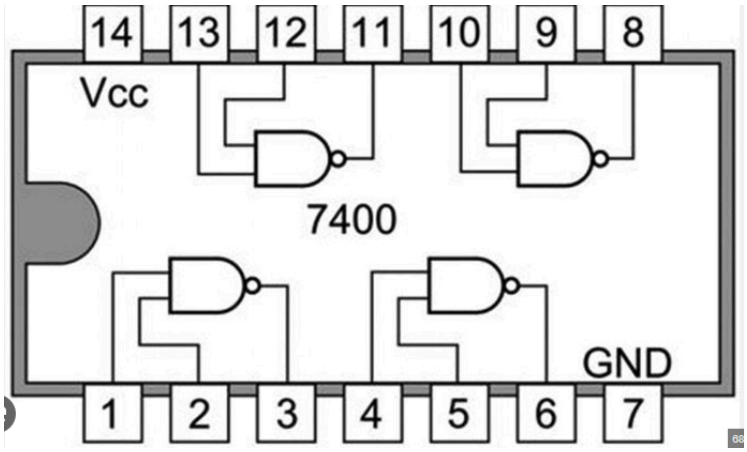
7432 Quad 2 input
OR Gates

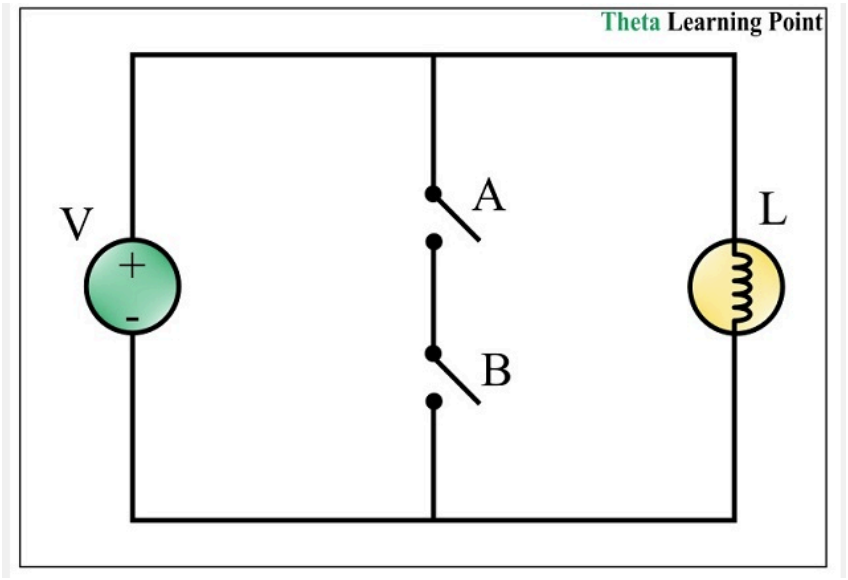


Electrical Circuit

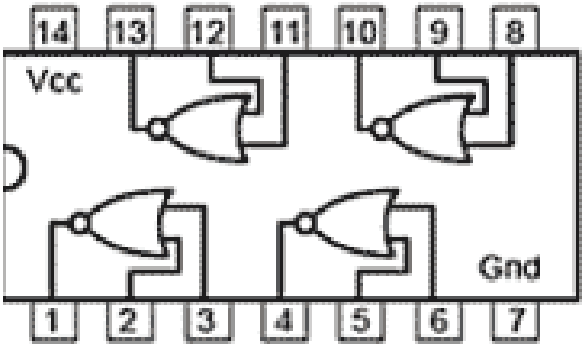
NAND GATE

Input	Input	Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



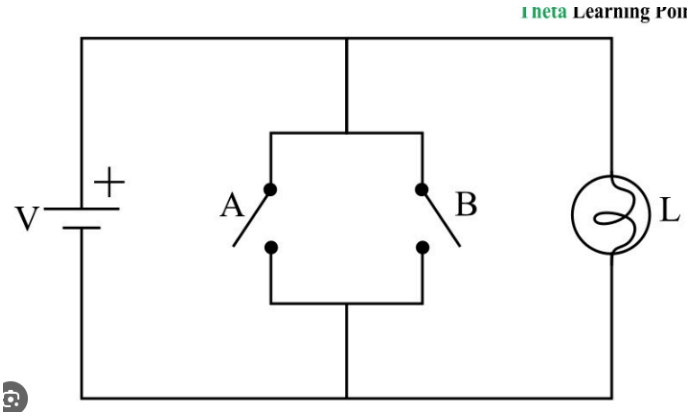


NOR GATE



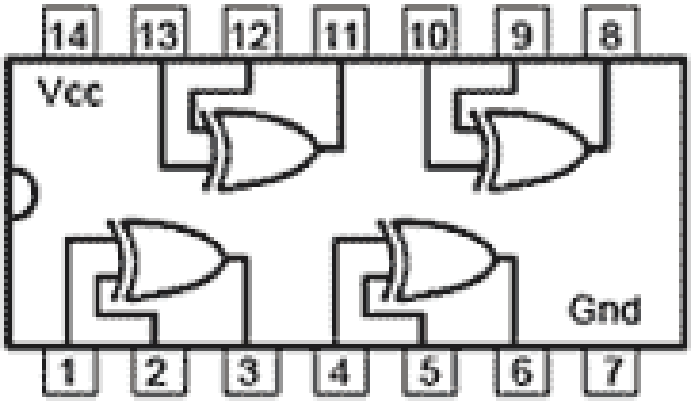
7402 Quad 2 input

A	B	Output
0	0	1
1	0	0
0	1	0
1	1	0

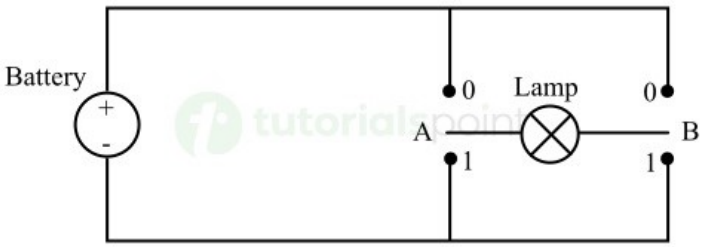


XOR GATE

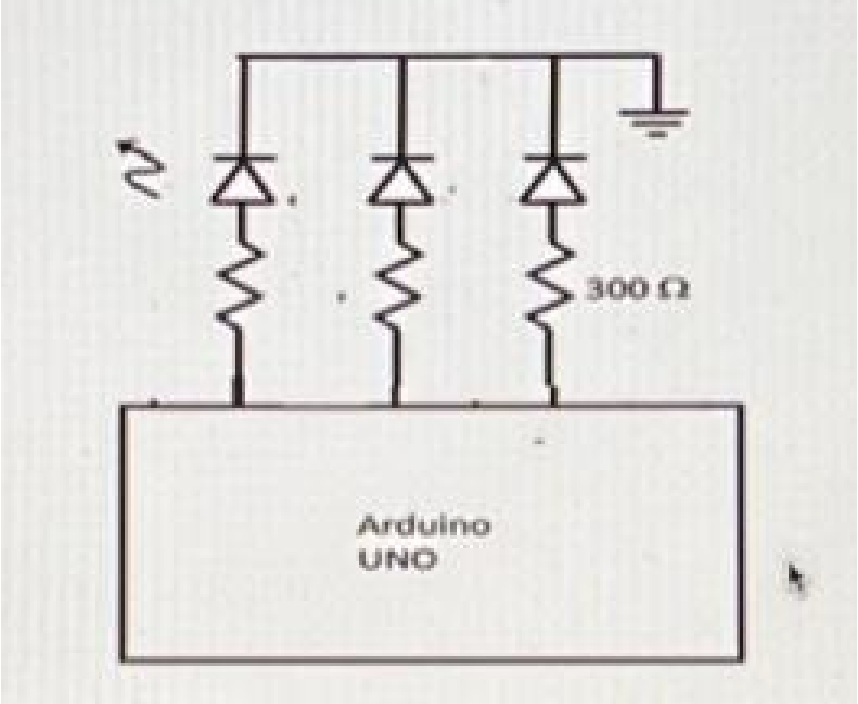
A	B	Output
0	0	0
1	0	1
0	1	1
1	1	0



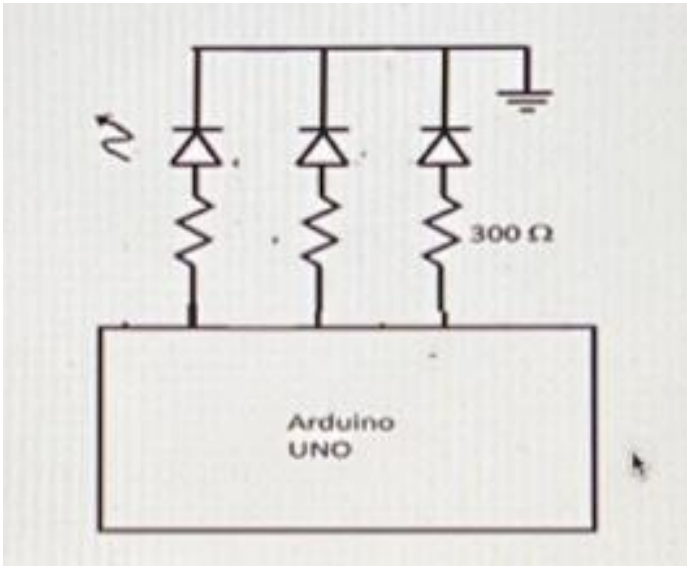
7486 Quad 2 input
XOR Gates



2) Experiment number 6



3) Experiment number 7



4) Experiment number 9