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a-) *Draw the truth table for the Circuit a.*

X	A_4	B_4	C	O_p	R_4	Overflow
0	0	0	0	0	0	0
0	0	0	1	0	Φ	1
0	0	1	0	1	1	0
0	0	1	1	1	0	0
0	1	0	0	1	0	0
0	1	0	1	1	1	0
0	1	1	0	0	1	0
0	1	1	1	0	Φ	1
1	0	0	0	1	1	0
1	0	0	1	1	0	0
1	0	1	0	0	0	0
1	0	1	1	0	Φ	1
1	1	0	0	0	1	0
1	1	0	1	0	Φ	1
1	1	1	0	1	0	0
1	1	1	1	1	1	0

Write the simplest expression for the outputs Op, Sign, and Overflow.

Karnaugh Map Of O_p :

$$\begin{array}{c|c|c|c|c}
\diagdown \; B_4C & & & & \\
XA_4 \diagdown & 00 & 01 & 11 \quad B_4 & 10 \\
\hline
00 & & & 1 & 1 \\
\hline
01 & 1 & 1 & & \\
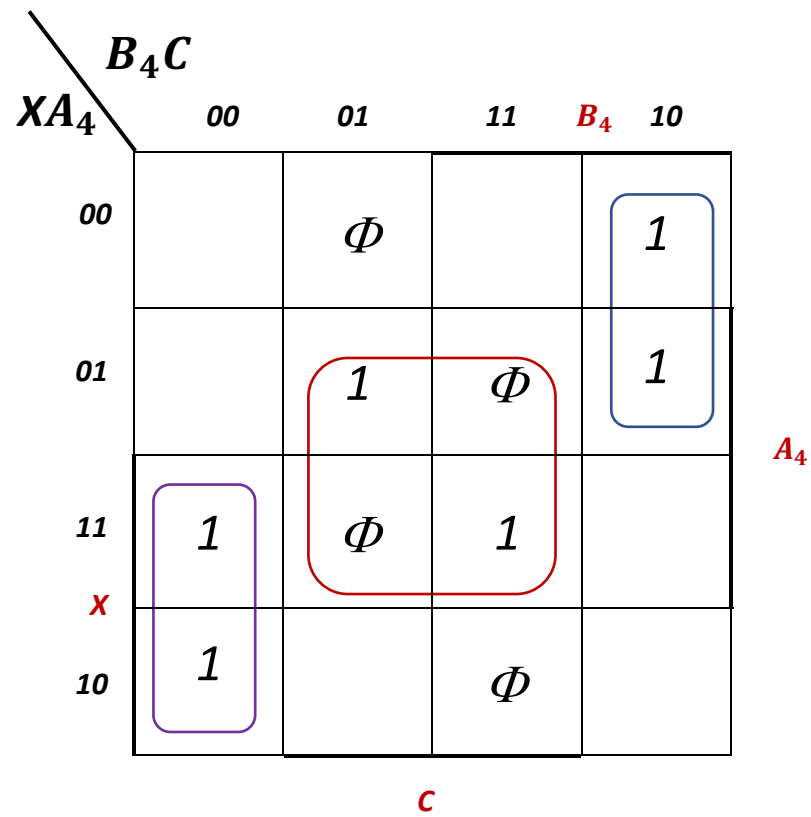\hline
11 & & & 1 & 1 \\
\hline
10 & 1 & 1 & & \\
\end{array}$$
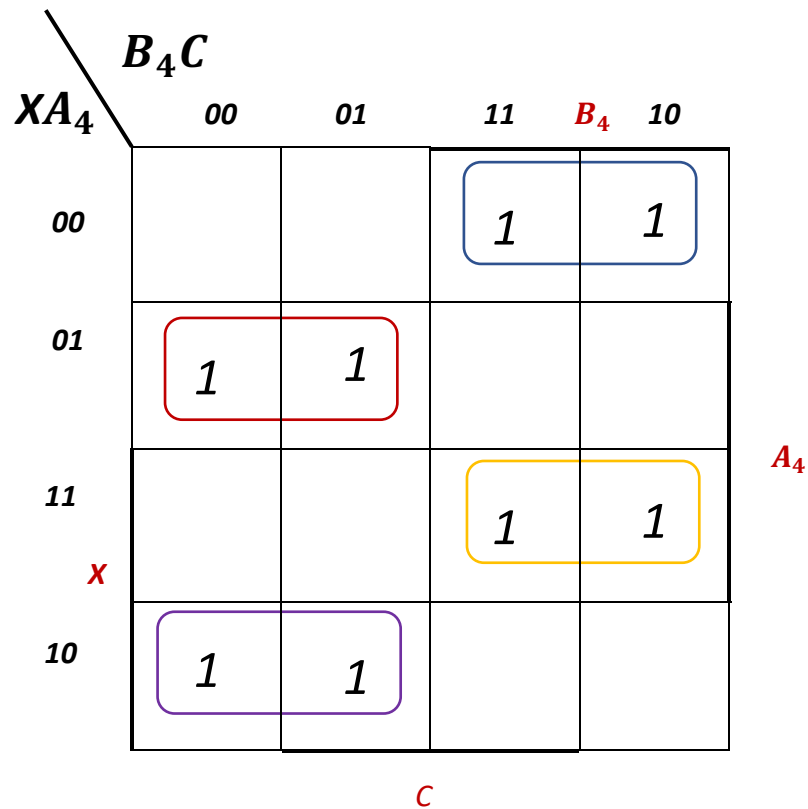
Simplest Expression of O_p is $\overline{X}A_4\overline{B_4} + \overline{X}\,\overline{A_4}B_4 + XA_4B_4 + X\overline{A_4}\,\overline{B_4}$.

Karnaugh Map Of Sign :

$$B_4 C$$
$$XA_4$$

	00	01	11 B_4	10
00		Φ		1
01		1	Φ	1
11 X	1	Φ	1	
10	1		Φ	

A_4

C

Simplest Expression of Sign is $X\overline{C}\,\overline{B_4} + \overline{X}\overline{C}B_4 + CA_4$.
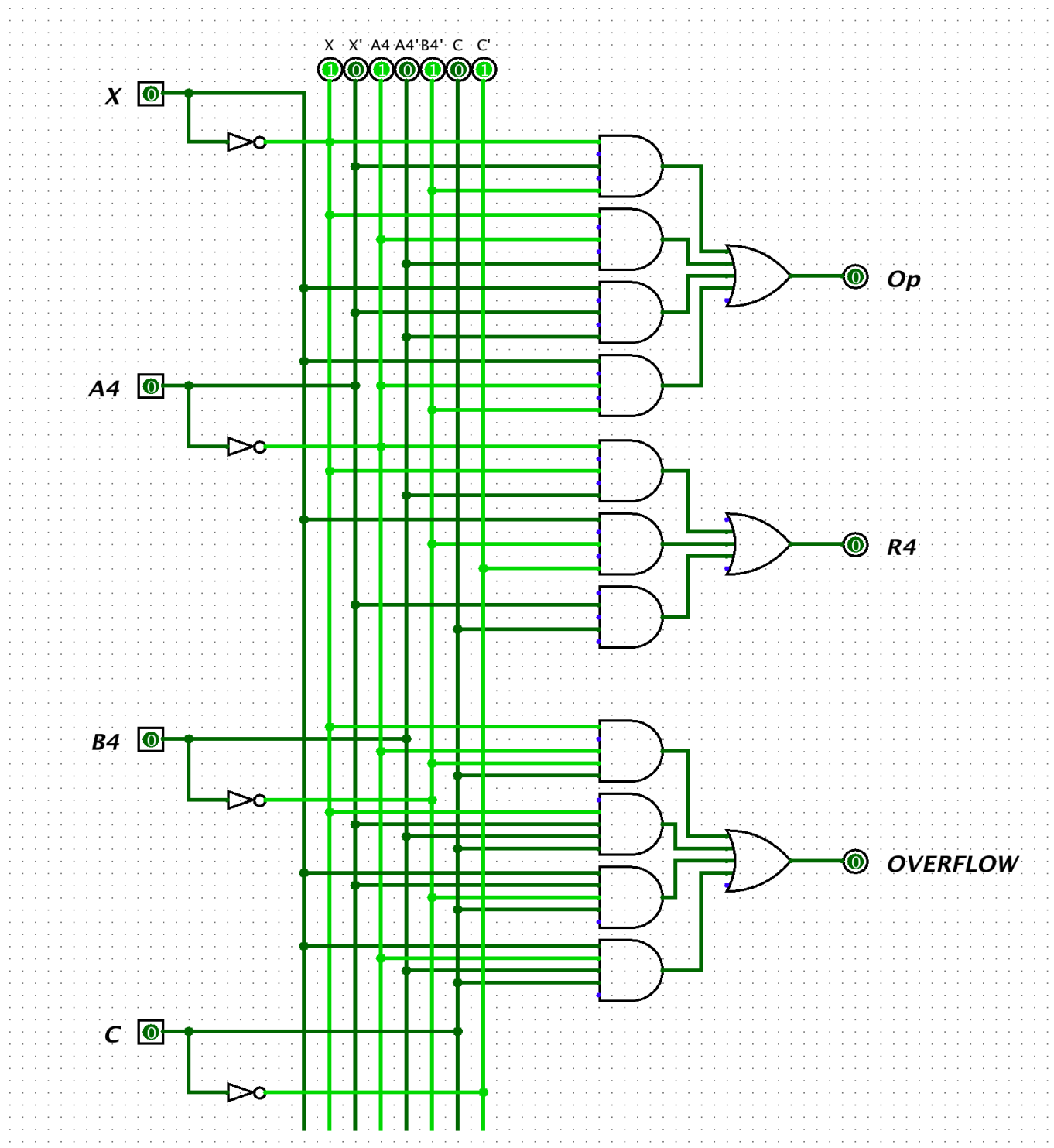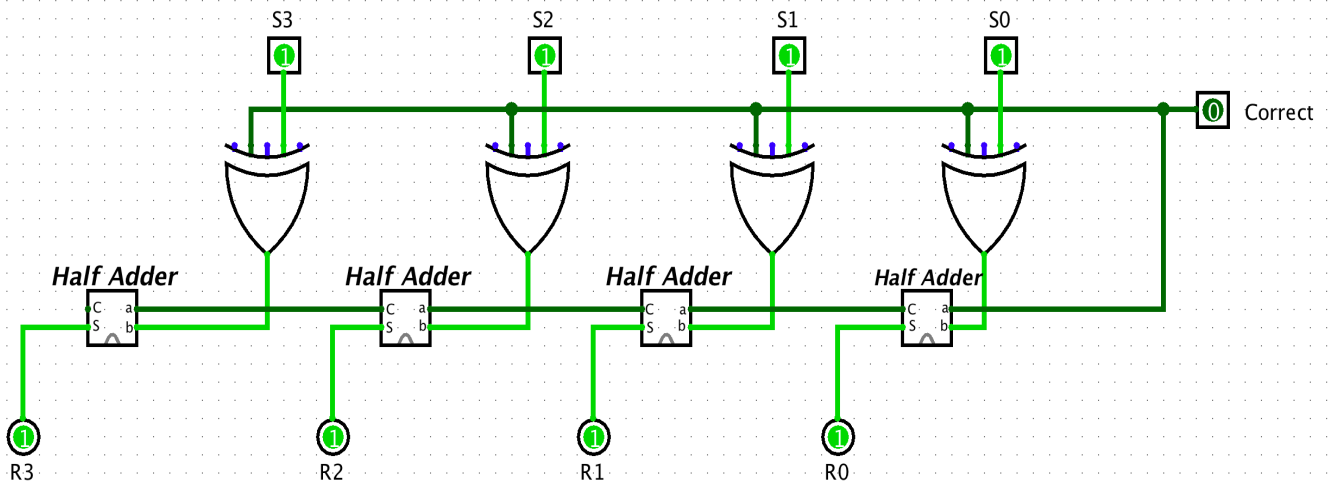
Karnaugh Map Of $Overflow$:

Simplest Expression of Overflow is $\overline{X}\,\overline{A_4}\,\overline{B_4}\,C + \overline{X}A_4B_4C + XA_4\overline{B_4}C + X\overline{A_4}B_4C$.

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Draw the circuit a using any type of logic gates. Fully label all input and outputs.

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b) **Design and draw the Circuit c using only half adders and minimum number of logic gates. Fully label all input and outputs.**

c) **Design and draw the Circuit d using any type of logic gates. Fully label all input and outputs.**