# BLG 231E Digital Circuits

## Fall 2019

| | CRN: 12010 | CRN: 12006 | CRN: 12008 |
|---|---|---|---|
| **Instructors:** | Feza Buzluca<br>http://akademi.itu.edu.tr/buzluca<br>EEB 4318 | Mustafa Kamaşak<br>http://akademi.itu.edu.tr/kamasak<br>EEB 3307 | Sanem Kabadayı<br>http://akademi.itu.edu.tr/kabadayi<br>EEB 3311 |
| **Classrooms:** | EEB 5102 | EEB 6309 | EEB 5202 |
| **Office Hours:** | Thursday 2-5 PM | Thursday 4:30-5:30 PM | Monday 4-5 PM<br>Thursday 3-4 PM |
| **TAs:**<br>(all sections) | Bilge Akkoca, Büşranur Bülbül, Tuğba Pamay, Meral Korkmaz Kuyucu<br>bakkoca @itu.edu.tr | bulbulb17 @itu.edu.tr | pamay @itu.edu.tr | korkmazmer @itu.edu.tr |

**Course site:** `http://ninova.itu.edu.tr`
**Course time and location:** Friday 8:30-11:30 AM, EEB 5102 - EEB 6309 - EEB 5202 (depending on section, check the table above)

**Description:** Boolean algebra, binary numbers, combinational logic design, synchronous sequential circuit analysis and synthesis.

**Required texts:**

- *Digital Design: Principles and Practices*, John F. Wakerly, Prentice Hall, 2005. 4th ed.
- *Digital Design*, Morris Mano, Prentice Hall, 2006. 4th ed.

For each lecture, you should read the relevant sections in the lecture slides as listed in the weekly course schedule on the last page of this syllabus.

**Homework:** You are expected to make an honest, independent attempt to solve and turn in your answers to each homework question. Digital circuits can only be mastered by solving problems, not just by listening to a lecturer. Therefore, doing the homework assignments is crucial to performing well in this class. If you are having considerable difficulty with the early assignments, this is a sign that you may be in over your head - you should come see us immediately. The assignments will require a substantial time commitment over several days (several hours per week outside of class should be expected). Be sure to budget sufficient time to complete assignments before the deadline. You may not copy solutions from a classmate or from the Internet. This is considered cheating! Homework is individual. There are no group assignments in this course.

**Attendance:** It is imperative that you come to class each day and pay attention. You are not allowed to work on your laptop or read anything not related to the class during the lecture. You must attend the section for which you have officially registered. Please check your actual section by logging into `http://www.sis.itu.edu.tr`. You are required to attend 70% of the lectures in order to be allowed to take the final exam. (Since this semester has 14 weeks, you have to attend at least 10 lectures). Those who do not meet the attendance requirement will fail the course with a grade of VF (Article 23, Undergraduate Education Regulations, `http://www.sis.itu.edu.tr/tr/yonetmelik/lisansyonetmelik.html`). Attendance may be taken at any point in the lecture. No additions can be made to the attendance list after that point. If you do miss class, it is your responsibility to find out (from a classmate) what you missed, including class notes, announcements, and worksheets. No make-up exams will be given. Absences from a midterm or final will result in a grade of zero for that exam. Check the exam dates and make sure you will be able to attend class on exam dates. The first midterm will be on Friday, October 18, 2019 in class (if exam rooms cannot be allocated for use during class time, the exam will be given in the late afternoon). The

second midterm will be on Friday, December 6, 2019 in class (if exam rooms cannot be allocated for use during class time, the exam will be given in the late afternoon).

**Evaluation:** The distribution of percentages for the course grade will be as follows:

| | |
|---|---|
| Homework | 15 % |
| Midterm 1 | 20 % |
| Midterm 2 | 25 % |
| Final | 40 % |

**Eligibility to take the final exam:** Students must meet the following criteria to take the final exam:

- Students must attend 70% of lectures.
- Students must have a mid-semester average grade of at least 35/100.

The average mid-semester grade is computed using the formula below:
Avg. mid-semester grade = (0.15 × Assign. + 0.20 × 1st Midterm + 0.25 × 2nd Midterm)*100/60

Any student who gets a grade lower than the required grade on any of these assessments will fail the course with a grade of VF and not be allowed to take the final exam.

**Announcements on course site and by e-mail:** You are expected to check the Ninova web site and your ITU e-mail for homework and announcements. In addition, you are responsible for all announcements that may be made on the course web site and in class (that may or may not be included in this syllabus).

**E-mail etiquette:** Your full name must appear in the e-mail. The e-mail subject must be "BLG 231E". Do not send the same e-mail repeatedly. Your e-mails may be in English or Turkish. Regardless of which language you use, use proper grammar, lowercase/uppercase letters, and punctuation. You e-mails should not look like chat messages.

**Academic honesty:** You are expected to read the Undergraduate Education Regulations (`http://www.sis.itu.edu.tr/tr/yonetmelik/lisansyonetmelik.html`) and ITU Academic Honesty Pledge (`http://www.sis.itu.edu.tr/tr/yonetmelik/AkademikOnurSozuEsaslar.html`) and behave accordingly. Cheating on the exams or on homework will result in disciplinary action. Every piece of work that you turn in with your name on it must be yours and yours alone. No coworking is allowed on any test or homework. You must not turn in work that is not yours. Specifically, you are not allowed to copy someone else's homework. This is plagiarism. You must not enable someone else to turn in work that is not his or hers. Do not share your work with anyone else.

**Final:** The final exam will be given during the final exam period (January 2-11, 2020), at the time and location determined by the University.

**Where does this course fit in?** This course is a prerequisite for BLG 242E Logic Circuits Lab (`http://ssb.sis.itu.edu.tr:9000/pls/PROD/itu_icerik.p_download?file=BLG242E`), BLG 212E Microprocessor Systems (`http://ssb.sis.itu.edu.tr:9000/pls/PROD/itu_icerik.p_download?file=BLG212E`) and BLG 222E Computer Organization (`http://ssb.sis.itu.edu.tr:9000/pls/PROD/itu_icerik.p_download?file=BLG222E`), which are required courses. It is also related to EHB 322E Digital Electronic Circuits (`http://ssb.sis.itu.edu.tr:9000/pls/PROD/itu_icerik.p_download?file=EHB322E`), another required course.

**Tentative course schedule (subject to change):**

| | Date | Subject | Slides |
|---|---|---|---|
| 1 | 20-Sep | Introduction: digital systems, number systems, binary codes, representation of numbers, binary arithmetic | 1.1-1.25 |
| 2 | 27-Sep | Boolean algebra: basic operations, Boolean expressions and truth tables, law&theorems of Boolean algebra, simplifying an expression, order relations | 2.1-2.25 |
| 3 | 4-Oct | Logic functions and their representations, forms (minterms/maxterms) Boolean cubes, Karnaugh maps, intro. logic gates, positive/negative logic | 2.26-2.41 3.1-3.8 |
| 4 | 11-Oct | Impl. of Boolean functions using logic gates, functionally complete sets of logic gates, universal logic gates, implementation using NAND&NOR gates | 3.9-3.24 |
| 5 | 18-Oct | Midterm Exam 1 | |
| 6 | 25-Oct | Timing diagrams, propagation delays, hazards, minimization of logic functions, essential/sufficient prime implicants, prime implicant chart | 4.1-4.27 |
| 7 | 1-Nov | Incomplete functions, don't cares, general functions, prime implicants using Quine-McCluskey, ICs, half adder, full adder, subtraction, multiplexers | 4.28-4.30 5.1-5.14 |
| 8 | 15-Nov | Demultiplexers, decoders, programmable logic devices (PLDs): PLAs, PALs, FPGAs, sequential circuits, FSM, memory units, T flip-flop | 5.15-5.33 6.1-6.7 |
| 9 | 22-Nov | Feedback, S-R latch, D latch, D flip-flop | 6.8-6.23 |
| 10 | 29-Nov | J-K latch and flip-flop, characteristic equations, registers, clocked synch. sequential circuits, Mealy, Moore, analysis of seq. circuits | 6.24-6.31 7.1-7.10 |
| 11 | 6-Dec | Midterm Exam 2 | |
| 12 | 13-Dec | Moore model, role of the clock signal Design of synchronous sequential circuits | 7.11-7.19 8.1-8.8 |
| 13 | 20-Dec | Synchronous circuit design using J-K FFs, multiplexers for synch. circuits, counter design, internal structures of electronic digital circuits, BJT, TTL | 8.9-8.23 9.1-9.4 |
| 14 | 27-Dec | TTL: logic levels, fanout, CMOS: NOT, NAND, NOR, three-state buffer, three-state common bus, logic levels | 9.5-9.17 |
| | 2-Jan - 14-Jan | Final (Tentative) | |

**Last day for add/drop:** The add/drop period ends on Friday, September 20, 2019.
You may withdraw from the course between September 23, 2019 and September 27, 2019.
There is no way to drop or withdraw from a course after September 27, 2019!