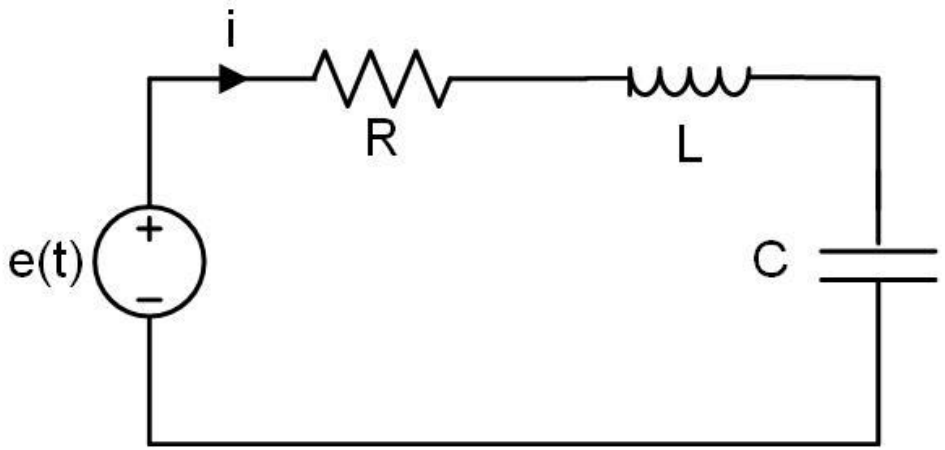
Dynamic Circuit Analysis



$$e(t) = V_R(t) + V_L(t) + V_C(\mathrm{t})$$

$$V_R(t) = Ri(t)$$

$$V_L(t) = L\frac{di(t)}{dt}$$

$$i_C(t) = C\frac{dV_C(t)}{dt} \quad \rightarrow \quad V_C(t) = \frac{1}{C}\int_0^t i_C(t)\,dt + V_C(0)$$

$$e(t) = Ri(t) + L\frac{di(t)}{dt} + \frac{1}{C}\int_0^t i_C(t)\,dt + V_C(0)$$

$$\frac{de(t)}{dt} = L\frac{d^2i(t)}{dt^2} + R\frac{di(t)}{dt} + \frac{1}{C}i(t)$$

State equation: $\dot{x}(t) = f(x,t)$ $\dot{x}(t) = \frac{dx(t)}{dt}$

State variable: $x(t)$

$$x_1(t) \equiv i(t) \qquad x_2(t) \equiv \frac{di(t)}{dt}$$

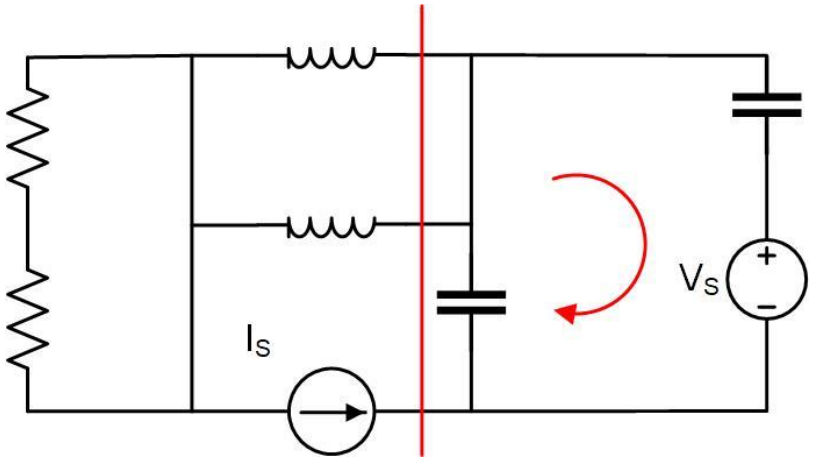
$$\dot{x}_1(t) = x_2(t) \qquad \dot{x}_2(t) = \frac{d^2i(t)}{dt^2}$$

$$\underbrace{\begin{bmatrix}\dot{x}_1(t)\\ \dot{x}_2(t)\end{bmatrix}}_{\dot{\underline{x}}(t)} = \underbrace{\begin{bmatrix}0 & 1\\ -1/LC & -R/L\end{bmatrix}}_{A}\underbrace{\begin{bmatrix}x_1(t)\\ x_2(t)\end{bmatrix}}_{\underline{x}(t)} + \underbrace{\begin{bmatrix}0\\ 1/L\end{bmatrix}}_{B_1}\dot{e}(t)$$

In general case: $\dot{\underline{x}}(t) = A\underline{x}(t) + B\underline{e}(t) + B_1\dot{\underline{e}}(t)$

Assumption:

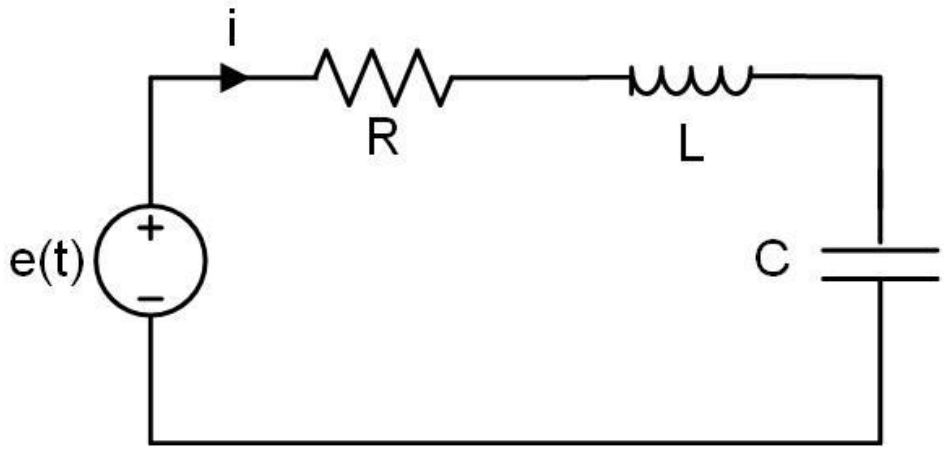
There is no loop which consists of only capacitors and independent voltage sources and
there is no cut set which consists of only inductors and independet current sources.



Analysis method:

1) Pick a tree of the digraph of the circuit which includes all the capacitors and voltage sources. Inductors and current sources will be links.
   → proper tree
2) The twig capacitor voltages and the link inductor currents are chosen as state variables.
3) For each fundamental cut set defined by the twig capacitor, write KCL equations.
4) For each fundamental loop defined by the link inductor, write KVL equations.

Example 9.1 Obtain state equations of the circuit given in the figure.

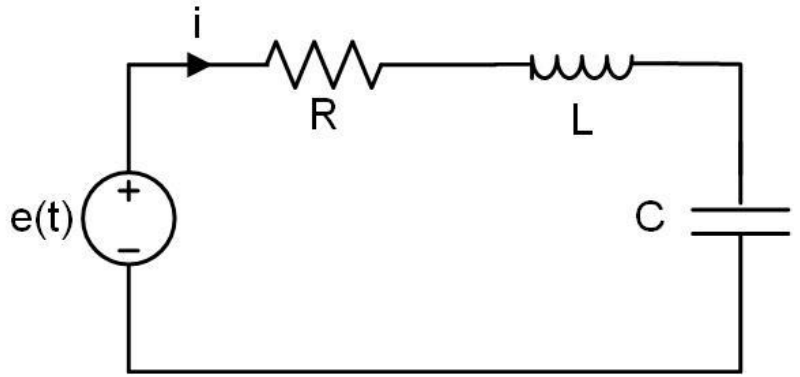


Output equation

$\underline{y}$: currents or voltages of other elements in the circuit

$$\dot{\underline{x}}(t) = A\underline{x}(t) + B\underline{e}(t) + B_1\dot{\underline{e}}(t)$$

$$\underline{y}(t) = C\underline{x}(t) + D\underline{e}(t) + D_1\dot{\underline{e}}(t)$$



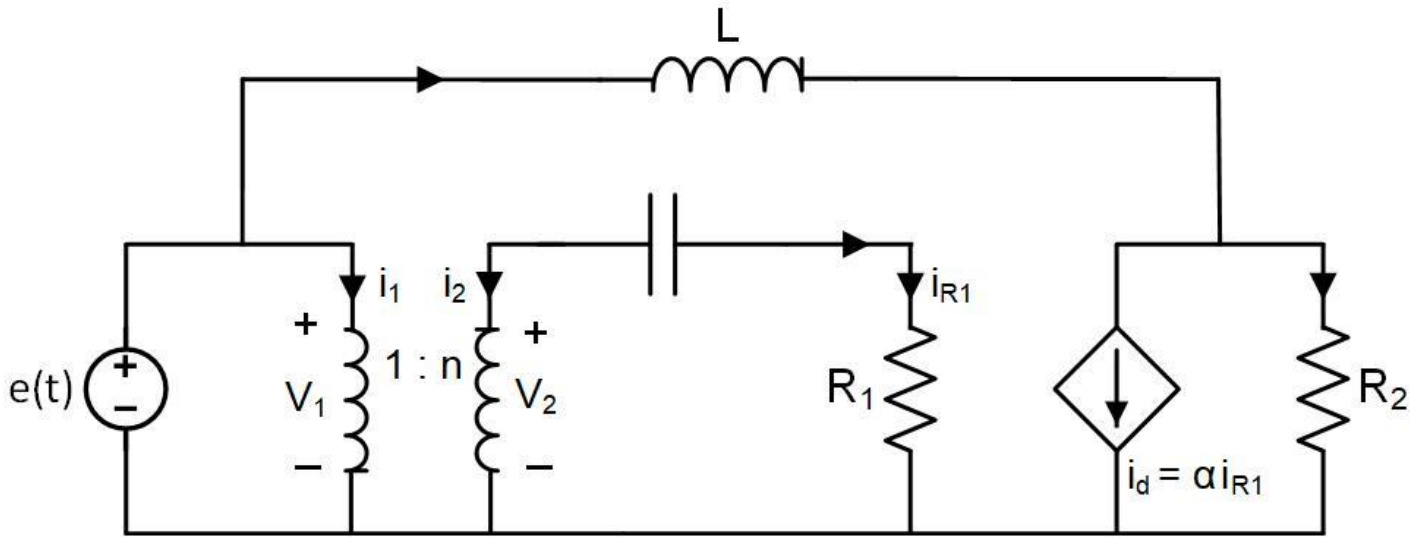
$$y = i_R = [1 \quad 0]\begin{bmatrix} i_L \\ V_C \end{bmatrix}$$

$$y = V_L = -Ri_L - V_C + e(t) = [-R \quad -1]\begin{bmatrix} i_L \\ V_C \end{bmatrix} + e(t)$$

Finding state equations in circuits consisting of RLC and linear multi-ports

1. Capacitors and independent voltage sources will be twigs.
2. Element equations in the element graph are considered if the tree is not complete.
   Element voltages will be twigs; element currents will be links.

Example 9.2



Solution of State Equations

Order of the circuit = number of state variables in the state equations

First order circuits

$$\dot{x}(t) = ax(t) + be(t), \qquad x(t_0) = x_0 \qquad a, b \in \mathbb{R}$$

$$x(t) = \underbrace{e^{a(t-t_0)}x(t_0)}_{zero-input\ response} + \underbrace{\int_{t_0}^{t} e^{-a\tau}be(\tau)d\tau}_{zero-state\ response}$$

$$\tau = \frac{1}{a} : \text{time constant}$$

Definition

1. If zero state response goes to zero for all x_0 as $t \to \infty$, then the circuit is asymptotically stable.
2. If zero state response stays finite for all x_0 as $t \to \infty$, then the circuit is stable.
3. If zero state response goes to infinity for some x_0 as $t \to \infty$, then the circuit is unstable.