x → o/p
P.S → Q_n
i/p → x

08/11

U-5 Synchronous Sequential Ckt Design
Asynchronous " " "

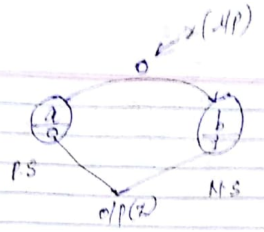
* Synchronous Sequential Ckt Design –

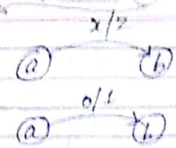
It is analysed by using two model / machine
(M/c – moore m/c
– mealy m/c)

Difference b/w Moore M/c & Mealy M/c

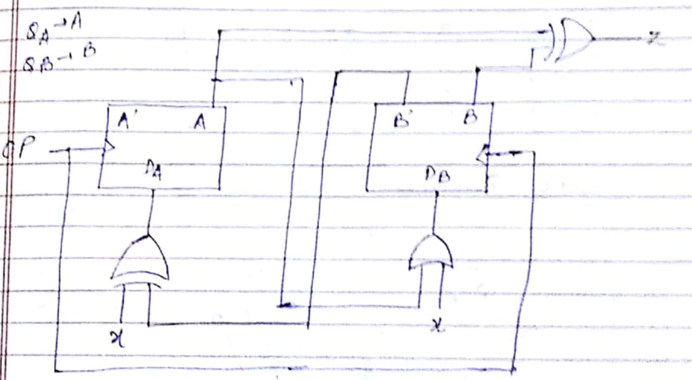
Moore M/c	Mealy M/c
1. O/p Z depends upon only in present state (Q_n); [Z = f(Q)]	1. O/p depends upon present i/p as well as in i/p (x) ; [Z = f(Q, x)]
If i/p changes, o/p doesn't change	2. If i/p changes, o/p Z also changes
More number of states are required	3 Less number of states are required.
Hardware requirement is more	4. Less
A counter is Moore M/c	5 A counter is not Mealy M/c

6.





Q. Analyse the following given sequential synchronous Ckt & determine whether this is an example of Mealy M/c or Moore M/c.
Draw state table.
Draw state diagram.



$D_A = x \oplus B' = x \odot B$
$D_B = x + A$
$Z = A \oplus B$

O/p Z depends upon only in present states A & B so it is an example of Moore M/c

$\therefore Q_{n+1} = D$ (NS) So $A^+ = D_A = x \oplus B$

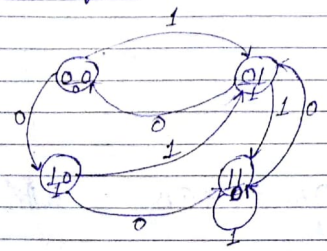
$B^+ = D_B = x + A$

from characteristic table of D ff

State table

PS: A	B	i/p x	NS A^+	B^+	o/p Z
0	0	0	1	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	01	1	1
1	0	0	01	1	1
1	0	1	0	1	1
1	1	0	0	1	0
1	1	1	1	1	0

State diagram

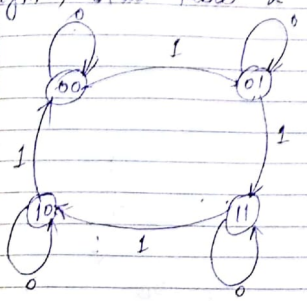


→ State dgm indicates transition from 1 state to next state

Q. In a clocked synchronous sequential ckt there are 2 D ff A & B when value x becomes zero, ff remains in present state & when value of x becomes 1, the following sequence comes →

00 → 01, 01 → 11, 11 → 10, 10 → 00

Design that synchronous seq ckt. (Draw state dgm, state table & value of ff i/ps)



State table:

A	B	x	A^+	B^+
0	0	0	0	0
0	0	1	0	1
0	01	0	0	1
0	1	1	1	1
1	0	0	1	0
1	0	1	0	0
1	1	0	1	1
1	1	1	1	0

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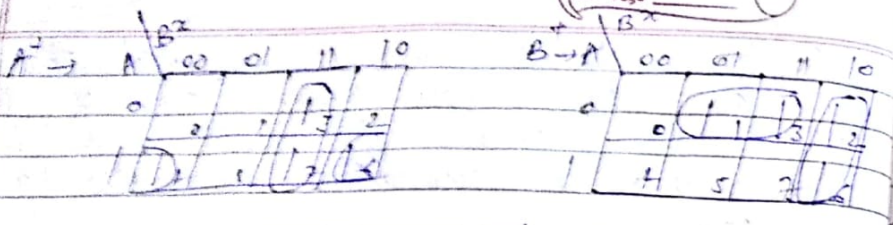
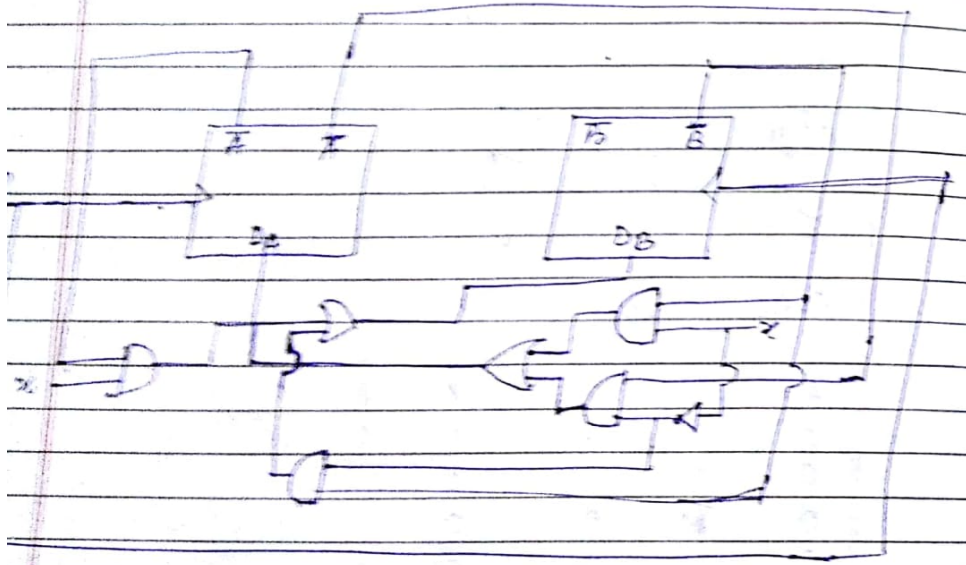




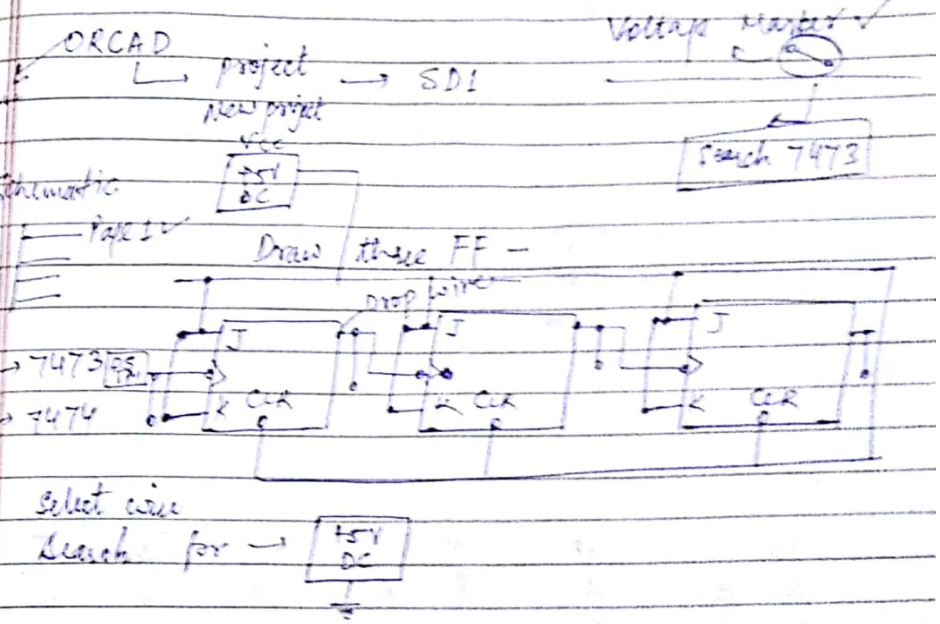
Simulation – Compare expected result wd actual result & then verify.

LAB Practicals

P.9. Design & Simulate MOD 8 Asynchronous/Ripple Counter or 3-bit binary Asyn. Counter

P.10. Design & Simulate MOD 6 Asynchronous Counter

P.11. Design & Simulate 3-bit Johnson Counter



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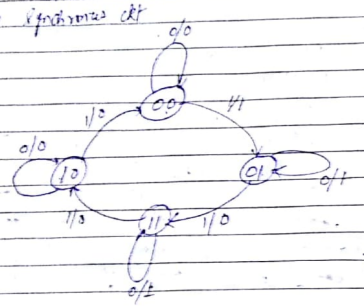
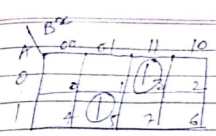
6. State dgm of sequential clocked ckt is given below:
Draw state table
Design synchronous ckt



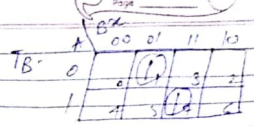
$T = Q \oplus Q^+$

PS		I/P	NS		O/P	T_A	T_B
A	B	x	A	B	Z		
0	0	0	0	0	0	0	0
0	0	1	0	1	1	0	1
0	1	0	0	1	1	0	0
0	1	1	1	1	0	1	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	1	0
1	1	0	1	1	1	0	0
1	1	1	1	0	0	0	1

T_A



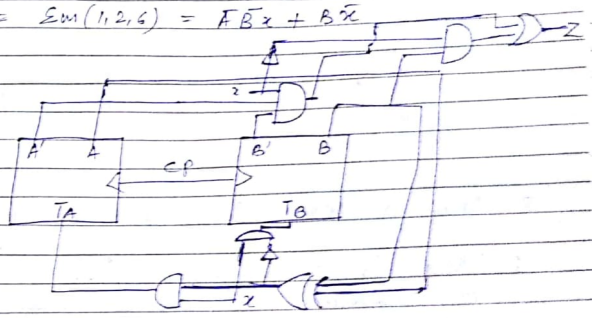
T_B



$T_A \rightarrow A\bar{B}x + \bar{A}Bx$
$= x(A\bar{B} + \bar{A}B)$
$= x \cdot (A \oplus B)$

$T_B \rightarrow ABx + \bar{A}\bar{B}x$
$= x \cdot (A \odot B)$

$Z = \Sigma m(1,2,6) = \bar{A}B\bar{x} + B\bar{x}$



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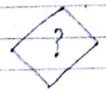
ASM Chart

ASM - Algorithmic State machine

 → start & stop

 → processing

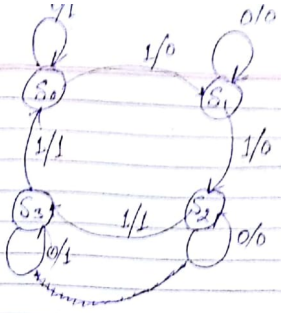
 → decision Making or conditional box

Q. Draw a ASM chart for following problems:

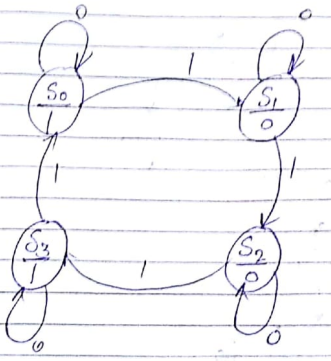
1. There is one control line X if X = 0 it remains in same state & when X = 1 it works as 2-bit up counter & when it reaches to minimum & or maximum value o/p becomes 1 o/w 0. Also draw state dgm.

or

$S_0 \rightarrow 00$
$S_1 \rightarrow 01$
$S_2 \rightarrow 10$
$S_3 \rightarrow 11$



← Mealy



← Moore

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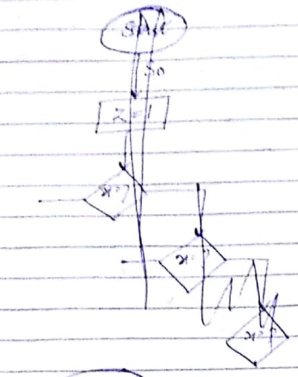
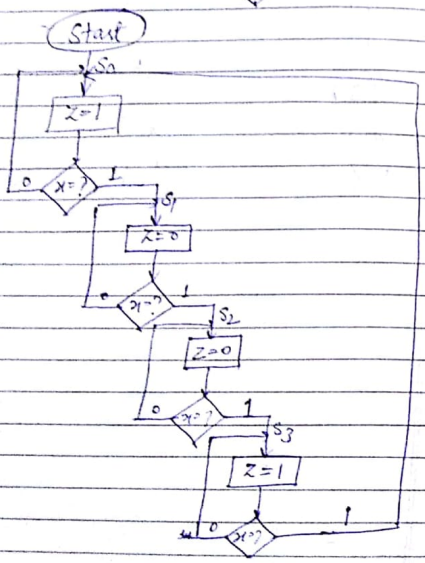
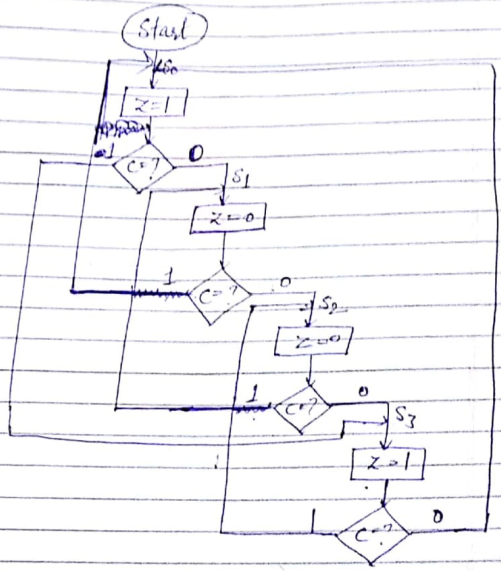
ASM chart





Q. Draw the ASM chart if there is one control line c. if c=1, it works as 2 bit down counter if c=0 it works as up counter & when it reaches min/max value, o/p becomes 1 o/w 0.



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