

Iron Law of Performance

$$CPU_{EXEC\ TIME} = \frac{instructions}{program} * \frac{cycles}{instruction} * \frac{time}{cycle}$$

Iron Law with Unequal Instruction Times

$$CPU_{EXEC\ TIME} = \left(\sum \frac{instructions}{program} * \frac{cycles}{instruction} \right) * \frac{time}{cycle}$$

CPI (Overall or Average)

$$CPI = CPI_{program} + \frac{mispredictions}{instruction} * \frac{penalty}{misprediction}$$

Speed Up:

$$SpeedUp = \frac{Old\ CPU_{EXEC\ TIME}}{New\ CPU_{EXEC\ TIME}} = \frac{New\ Throughput}{Old\ Throughput} = \frac{Old\ Latency}{New\ Latency}$$

Amdahls Law

$$SpeedUp = \frac{1}{(1-P) + \frac{P}{N}} \quad \text{Note: P must be a percent of execution time, not a percent of instructions/cycles.}$$

AMAT

$$AMAT = hitTime + missRate(missPenalty)$$

$$missTime = hitTime + missPenalty$$

$$AMAT = hitRate(hitTime) + missRate(missTime)$$

$$AMAT = L1\ hit\ rate + L1\ miss\ rate * L1\ miss\ penalty$$

$$L1\ miss\ penalty = L2\ hit\ time + L2\ miss\ rate(L2\ miss\ penalty)$$

$$L2\ miss\ penalty = L3\ hit\ time + L3\ miss\ rate(L3\ miss\ penalty)$$

$$GlobalHitRate = 1 - \frac{\# \text{ of Misses this cache level has}}{\# \text{ of all Memory Accesses}}$$

$$LocalHitRate = \frac{\# \text{ of Hits this cache level has}}{\# \text{ of accesses to this cache level}}$$

Fault Tolerance

Reliability = MTTF = average time a system works until a part of it fails

Availability = MTTF / (MTTF + MTTR) = percent of time a system is working correctly

For all RAIDs: f_1 = failure rate of a single disk, f_N = failure rate of N disks = $N * f_1$

$$MTTF_N = MTDDL_N$$

RAID0

$$MTDDL_1 = \frac{1}{f_1}, \quad N \text{ disks: } MTDDL_N = \frac{MTTF_1}{N}$$

RAID1

$$MTDDL_1 = \frac{1}{f_1}$$

$$2 \text{ disks (no disk replacement)} MTDDL_2 = \frac{MTTF_1}{2} + MTTF_1$$

$$2 \text{ disks (with disk replacement)} MTDDL_2 = \frac{MTTF_1}{2} * \frac{MTTF_1}{MTTR_1}$$

RAID 4/5

$$N \text{ disks (no disk replacement)} MTDDL_2 = \frac{MTTF_1}{N} + \frac{MTTF_1}{N-1}$$

$$N \text{ disks (with disk replacement)} MTDDL_2 = \frac{MTTF_1}{N} * \frac{MTTF_1}{N-1} * \frac{1}{MTTR_1}$$

Many Core Challenges

$$\text{power} = C v^2 f$$

$$f_{\text{new}} = f_{\text{old}} * \sqrt[3]{\frac{\text{old number of cores}}{\text{new number of cores}}}$$

$$\text{exe}_{\text{new}} = (\text{exeTime speedup} * \text{old exeTime}) * \text{frequencySpeedup}$$

$$\text{exe}_{\text{time speedup}} = \% \text{ofTimeWeCanUseXCores} * \frac{1}{X} + \dots +$$