VDD_3V3

U1
VDD_3V31 — VCC
         VOUT ── 2 ── R3 ── GPIO1_28
GND ── 3 ── GND   4.7K

actually a DS18B20+

BONE_SCH.pdf, AIN0, P9.39
AIN5

R5
1K

1503_02
  1
  3
  2
X1

R4
33

BONE_SCH.pdf, VDD_ADC, P9.32
VDD_ADC

R1
470K

R2
470K

10UF
C2

R4 burden resistor comments:
assumes Imax is 50A peak (35A RMS)
assumes SCT-013-000 sensor
if AVCC is 5V, R4 = 100
if AVCC is 3.3V, R4 = 66
if AVCC is 1.8V, R4 = 36

GNDA_ADC
BONE_SCH.pdf, GNDA_ADC, P9.34

P9

GND ── 1   2 ── GND
       3   4 ── VDD_3V3
       5   6 ── VDD_5V
       7   8
       9 10
      11 12 ── GPIO1_28
      13 14
      15 16
      17 18
      19 20
      21 22
      23 24
      25 26
      27 28
      29 30
      31 32 ── VDD_ADC
      33 34 ── GNDA_ADC
      35 36 ── AIN5

free to use headers

JP3   JP1   JP2   JP4   JP10   JP11
10   10   10   10   10   10
 9   9   9   9   9   9
 8   8   8   8   8   8
 7   7   7   7   7   7
 6   6   6   6   6   6
 5   5   5   5   5   5
 4   4   4   4   4   4
 3   3   3   3   3   3
 2   2   2   2   2   2
 1   1   1   1   1   1
M10LOCK M10LOCK M10LOCK M10LOCK M10LOCK M10LOCK

JP5   JP6   JP7   JP8   JP9
10   10   10   10   10
 9   9   9   9   9
 8   8   8   8   8
 7   7   7   7   7
 6   6   6   6   6
 5   5   5   5   5
 4   4   4   4   4
 3   3   3   3   3
 2   2   2   2   2
 1   1   1   1   1
M10LOCK M10LOCK M10LOCK M10LOCK M10LOCK

https://github.com/texane/bbone_ct_cape
rev 91c018a3751a
texane@gmail.com

main

10/15/14 1:38 PM

Sheet: 1/1

10/15/14 1:59 PM /buffer/PCLAB2451/lementec/repo/bbone_ct_cape/sch/main.sch (Sheet: 1/1)