Lab 1 – 7-Segment LED Display Decoder

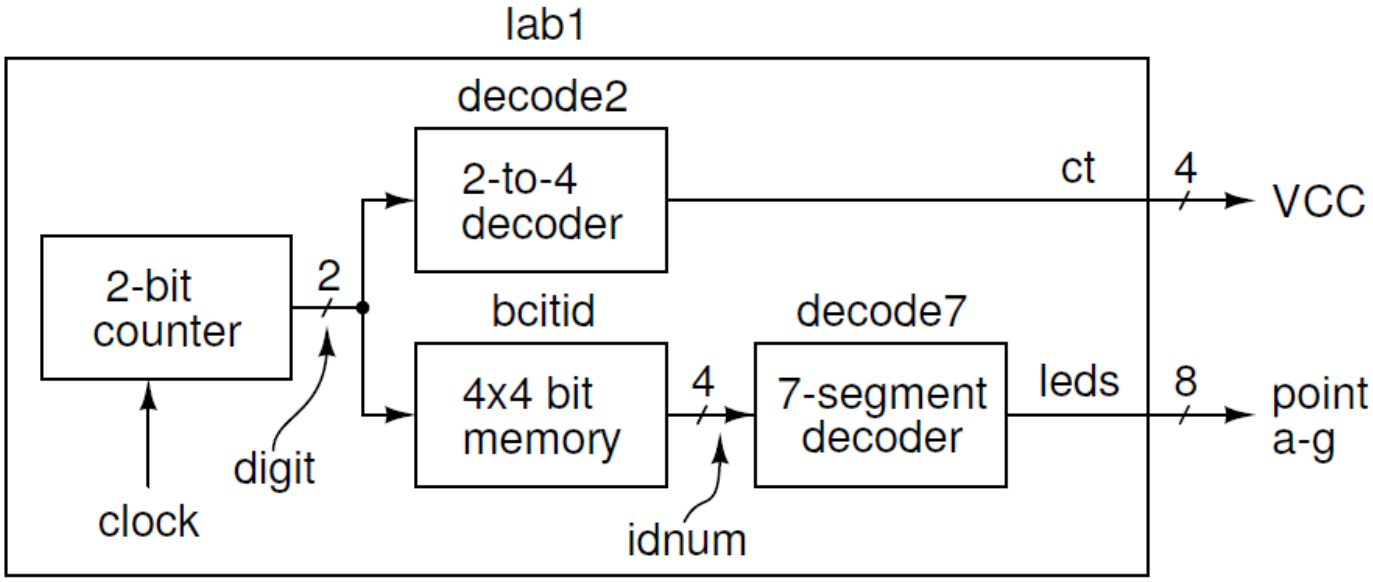
1 Objectives

1. Demonstrate the use of FPGA simulation and synthesis tools to implement a digital design.
2. Implement a moderately complex design using RTL and structural SystemVerilog descriptions.

2 Introduction

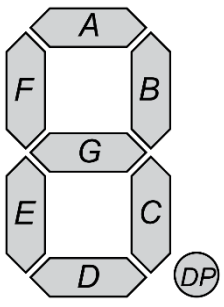
In this lab you will design and implement a circuit to display the last four digits of your student number on a 4-digit 7-segment display module. The lab1.sv file provided implements the **`lab1`** top level module as shown in the figure below.

As this is the first lab and we have barely started with the lectures, the lab will be split over two weeks.



You must design and implement the **`decode2`**, **`bcitid`**, and **`decode7`** modules as follows:

- The **`decode2`** module implements a 2-to-4 decoder. The module has a 2-bit input call **`digit`** and a 4-bit active low output called **`ct`** which controls which digit is displayed. For example, if the input is "00", the output is "1110", and if the input is "01", the output is "1101", etc.
- The **`bcitid`** module implements a 4x4 bit memory that will store the last four digits of your BCIT student ID. The module has a 2-bit input call **`digit`** and a 4-bit output called **`idnum`**. When **`digit`** is 3, the leftmost digit is output as **`idnum`**, and when **`digit`** is 0, the rightmost digit is output.
- The **`decode7`** module converts any 4 bit number **`num`** (0, 1, 2, …E, F) into the signals necessary to control the 7-segment display. The module has a 4-bit input **`num`** and an 8-bit active high output called **`leds`**. The most significant bit of the **`leds`** output signal controls the decimal point, and bits 6 through 0 are connected to segments "g" through "a" respectively. Note that the 7-segment display for hexadecimal symbols A to F should be upper case except for 'b' and 'd' which must be lower case.



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3 Week 1 Activities

Study the "nano_interface_schematic.pdf" and "Quad 7 Segment Display TDCG1060M.pdf" documents provided in the datasheets folder. Note that we are using part TDCG106M, a Common Cathode device. The a, b, c, d, … pins are shared by the anodes of all 4 digits. Each digit is individually enabled by enabling the Dx input pin (x = 1, 2, 3, or 4).

Write the three SystemVerilog modules that meet the requirements given in the introduction. Each module should be defined in its own file (**`decode2.sv`**, **`bcitid.sv`**, and **`decode7.sv`**).

Simulate your designs using the testbenches provided (**`decode2_tb.sv`**, **`bcitid_tb.sv`**, and **`decode7_tb.sv`**) using the instructions given in Appendix A. Create a PDF document which includes the simulation waveforms.

4 Week 2 Activities

Follow the instructions in Appedix B to synthesise the provided **`lab1.sv`** file along with your code. Connect the LED display to the FPGA board, plug in the FPGA board and program it.

Appendix A – Simulation with Modelsim

1. From Windows start "Modelsim - Intel FPGA..."
2. Select File > New > Project..., select the folder where your files are located as the Project Location and enter a suitable Project Name (e.g. lab1), then click OK. Select Add Existing File and select the file(s) that contain the modules you want to simulate then select Close. If you had already created a simulation project and it's not already open, select File > Open, select Files of type: Project Files (*.mpf) and select the project file.
3. Select Compile > Compile All to compile all the files in your project into the work library. If there are syntax errors you will need to fix them and recompile.
4. Select Simulate > Start Simulation. Select your testbench module from the work library and select OK.
5. In the 'sim' window select the module whose signals you wish to view; select Add > To Wave > All items in region,
6. Select Simulate > Run -All; this will run until your testbench executes **`$stop`**. if the results are as expected (select the Wave window, click on '+' and Wave > Zoom > Full), use a screen capture utility (e.g. Windows Snip tool) to save the waveforms for your report.
7. Repeat from steps 4 & 5 for other testbenches.

Appendix B – Synthesis with Quartus

1. From Windows start "Quartus Prime"
2. Select File > New > New Quartus Prime Project > OK.
    a. Create or select a folder as the working directory, name the project (e.g. lab1), click Next,
    b. Select empty project, click Next
    c. don't add files, click Next
    d. select the Cyclone V Family, enter 5CSEMA4U23C6 in the "Name filter" and select the device under "Available Devices", and click Finish.
3. Download the ELEX7660Pins.qsf (Quartus settings) file from D2L. Select Assignments > Import Assignments > and select the .qsf file. This will add settings such as the FPGA pins for port signals.

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4. For the top-level module – the one whose ports represent the FPGA's pins – you must use the project name for the file name (e.g. lab1.sv) and as the module name (e.g. lab1) and ensure that the top-level port names match the signal names in the .qsf file. If you have already created this top-level Verilog file, or to add additional files, select Project > Add/Remove Files in Project and add these file(s). If a file has to be created, select File > New... > System Verilog File > OK.
5. Select Processing > Start Compilation (or press the  icon). Correct any errors and recompile as necessary,
6. Connect the FPGA to the PC's USB port using the supplied cable and plug in the power supply for the FPGA. **There are three USB ports on the board, be sure to connect to the USB port labelled USB Blaster next to the power cord on the FPGA board.**
7. Select Tools > Programmer (or click on the  icon). If no "No Hardware" is displayed, select Hardware Setup..., select DE-SoC [USB-1] and select Close. Push Autodetect and in the "Select Device" window, select the "5CSEMA4" option and click OK. In the Programmer window, select the 5CSEMA4 device, press Change File... and select the projectname.sof file (ie. lab1.sof) in the output_files folder. Set the Program/Configure checkbox on the 5CSEMA4U23 Line. Press Start to program the device. Your design should now be loaded and running in the FPGA.
8. To generate schematics select Tools > Netlist Viewers > RTL Viewer
9. To view the compilation summary select Window > Compilation Report

Note: Project settings include drive and path names so the project must be restored to the same drive and folder to continue working on it. To transfer to a different drive or directory (ie. to move your project from one computer to another), use Project > Archive Project and then Project > Restore Archived Project.

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