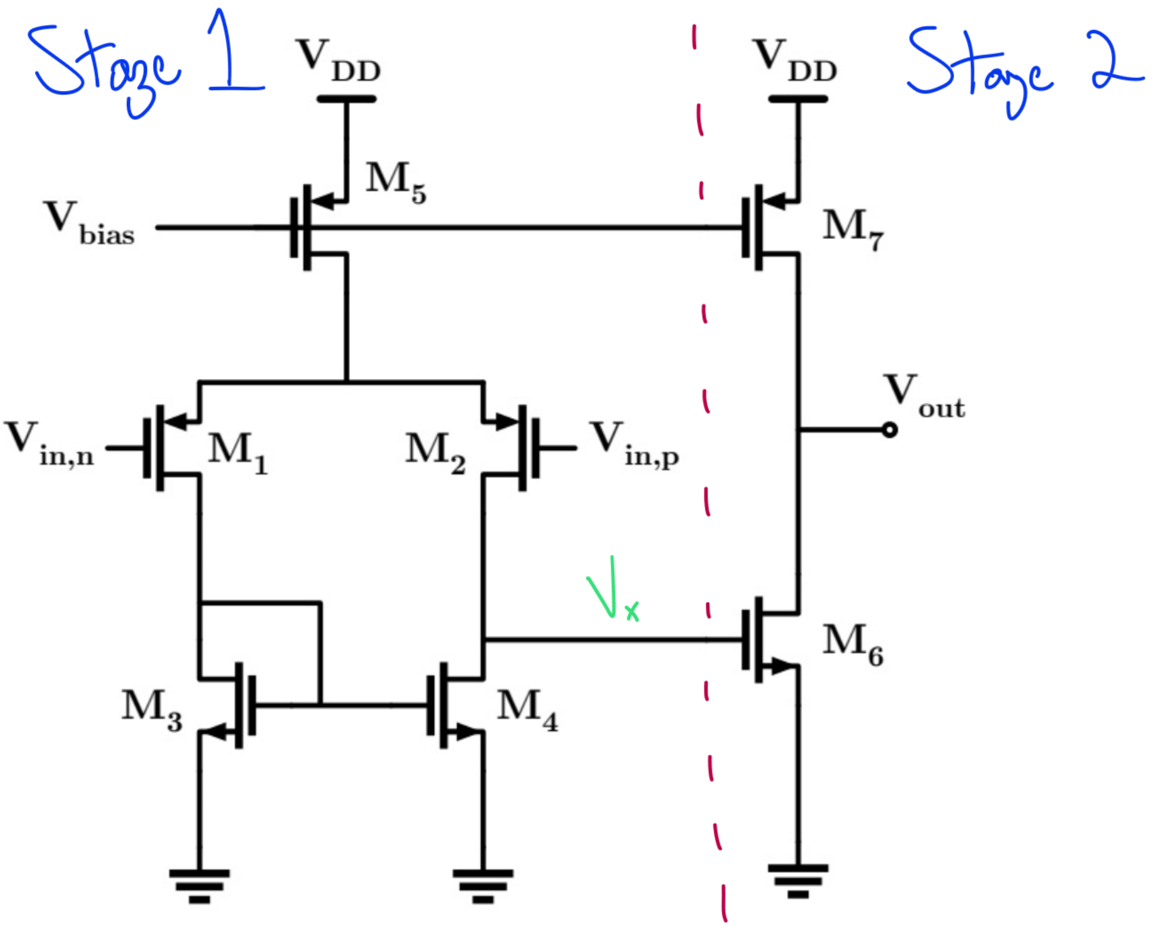
Problem 1 - PSRR of the Two-Stage Amplifier

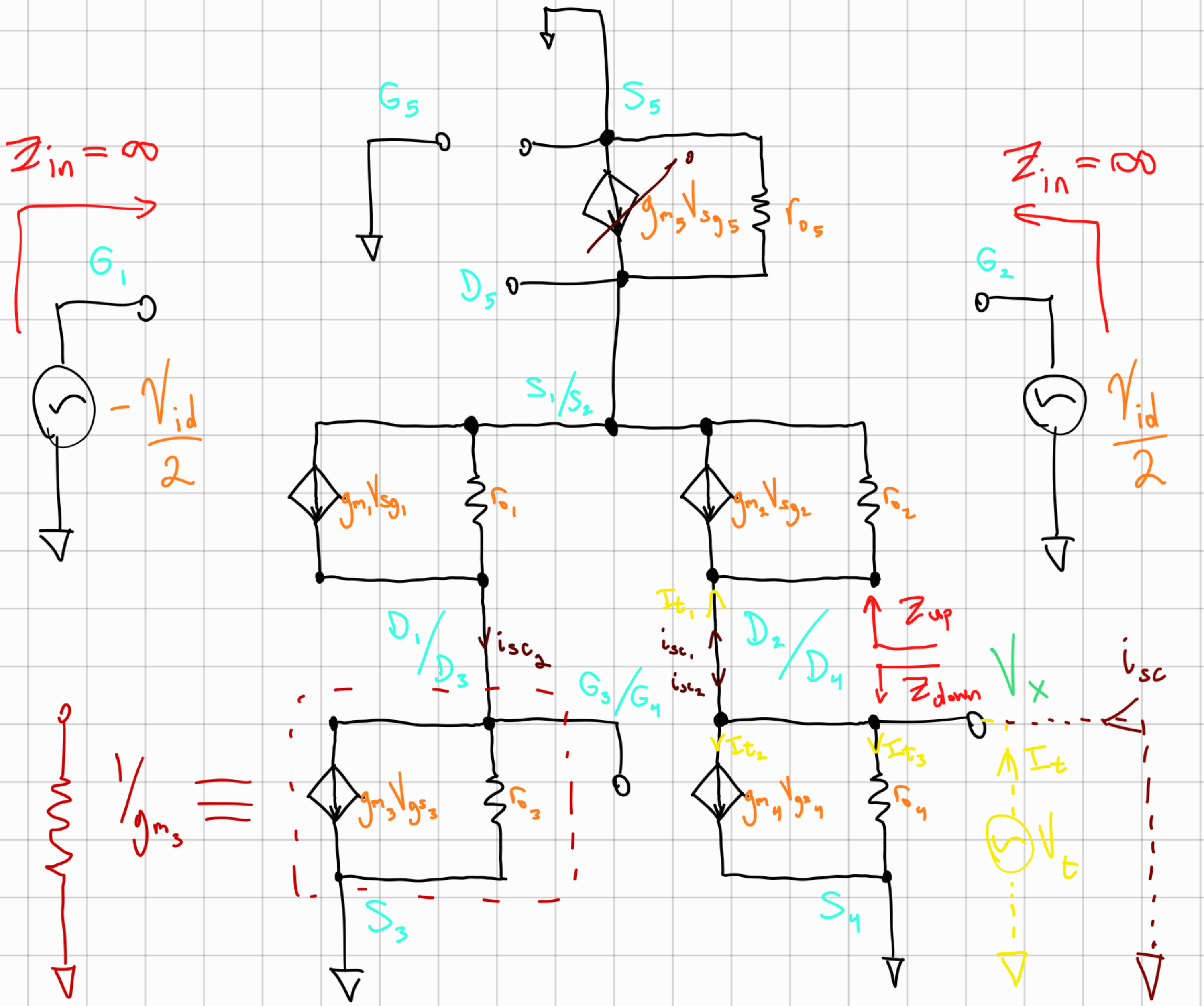
In this problem, we will calculate the PSRR+ of the workhorse two-stage amplifier. In such amplifiers, when V_{bias} is not created in a particular manner such that it tracks the changes in V_{DD}, we may experience a degraded PSRR+ performance. Express all your answers in terms of small-signal parameters of the devices (g_m and r_o of each transistor). Assume that symmetric transistors in the differential amplifier share the same small signal parameters.



(a) Calculate the differential mode gain of the circuit: $A_{vd} = \frac{v_{out}}{v_{in,p} - v_{in,n}}$

$$\Rightarrow \quad A_{vd} = \frac{V_x}{V_{in,p} - V_{in,n}} \cdot \frac{V_{out}}{V_x}$$

Small-signal Model (Stage 1)



Output Resistance

$$I_{t_1} = \frac{V_t}{R_{th,id_2}} \qquad I_{t_2} = \frac{V_t}{r_{o_4}} \qquad I_{t_3} = g_{m_4}V_{gs_4}$$

$$R_{th,d_2} = r_{o_2}\left(1 + g_{m_2} R_S\right) + R_S$$

$$\Rightarrow R_S = \cancel{r_{o_5}} \,\|\, 1/g_{m_1} + 1/g_{m_3}$$

$r_{o_5} \gg 1/g_{m_1}$

$$= 1/g_{m_1} + \cancel{1/g_{m_3}}^{\,\simeq 0} \qquad 1/g_{m_3} \text{ negligible}$$

$$\simeq 1/g_{m_1}$$

$* \; g_{m_1} = g_{m_2}$

$$\Rightarrow R_{th,d_2} = r_{o_2}\left(1 + \cancel{g_{m_1}}^{\,1} / g_{m_2}\right) + 1/g_{m_1}$$

$$= 2 r_{o_2} + \cancel{1/g_{m_1}}^{\,\simeq 0}$$

$$\boxed{\therefore R_{th,d_2} \simeq 2 r_{o_2}}$$

$$\Rightarrow V_{g_5} = I_{t_1} \cdot {}^{1}/_{g_{m_3}} \Rightarrow I_{t_3} = g_{m_4} \cdot \frac{I_{t_1}}{g_{m_3}}$$

$$\Rightarrow I_t = I_{t_1} + I_{t_2} + I_{t_3}$$

$$= \frac{V_t}{2r_{o_2}} + \frac{V_t}{r_{o_4}} + I_{t_1}\cancelto{1}{\left(\frac{g_{m_4}}{g_{m_3}}\right)}$$

$$= V_t\left(\frac{1}{2r_{o_2}} + \frac{1}{r_{o_4}} + \frac{1}{2r_{o_2}}\right)$$

$$\boxed{\therefore R_{out} = \frac{V_t}{I_t} = r_{o_2} \,//\, r_{o_4}}$$

Transconductance

$\Rightarrow$ For differential analysis, $V_{in,p} = \frac{V_{id}}{2}$ & $V_{in,n} = -\frac{V_{id}}{2}$

$$\Rightarrow i_{sc_1} = g_{m_1} \cdot \frac{V_{id}}{2} = g_{m_2} \cdot \frac{V_{id}}{2}$$

$$\Rightarrow V_{g_4} = 1/g_{m_3} \cdot g_{m_1} \cdot V_{sg_1}$$

$$= \frac{g_{m_1}}{g_{m_3}} \cdot -\left(-\frac{V_{id}}{2}\right) = \frac{V_{id}}{2} \cdot \frac{g_{m_1}}{g_{m_3}}$$

$$\Rightarrow i_{sc_2} = g_{m_4} V_{gs_4} = \cancel{\frac{g_{m_4}}{g_{m_3}}}^{1} \cdot \frac{V_{id} \cdot g_{m_1}}{2}$$

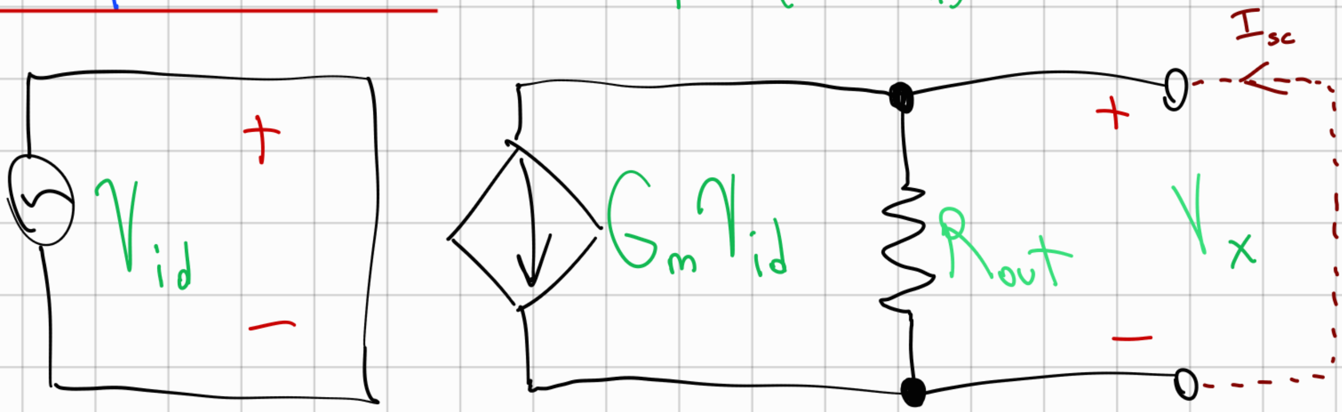
$$\Rightarrow i_{sc} = i_{sc_1} + i_{sc_2} = g_{m_1} \cdot \frac{V_{id}}{2} + \frac{V_{id} \cdot g_{m_1}}{2}$$

$$= V_{id}\left(\frac{g_{m_1}}{2} + \frac{g_{m_1}}{2}\right)$$

$$\boxed{\therefore\ i_{sc} = V_{id} \cdot g_{m_1}}$$

Two-port Model

$* \; V_{in,p} - (-V_{in,n}) = V_{id}$



$$\Rightarrow I_{sc} = G_m \cancel{V_{id}} = g_{m_1} \cancel{V_{id}} = i_{sc}$$

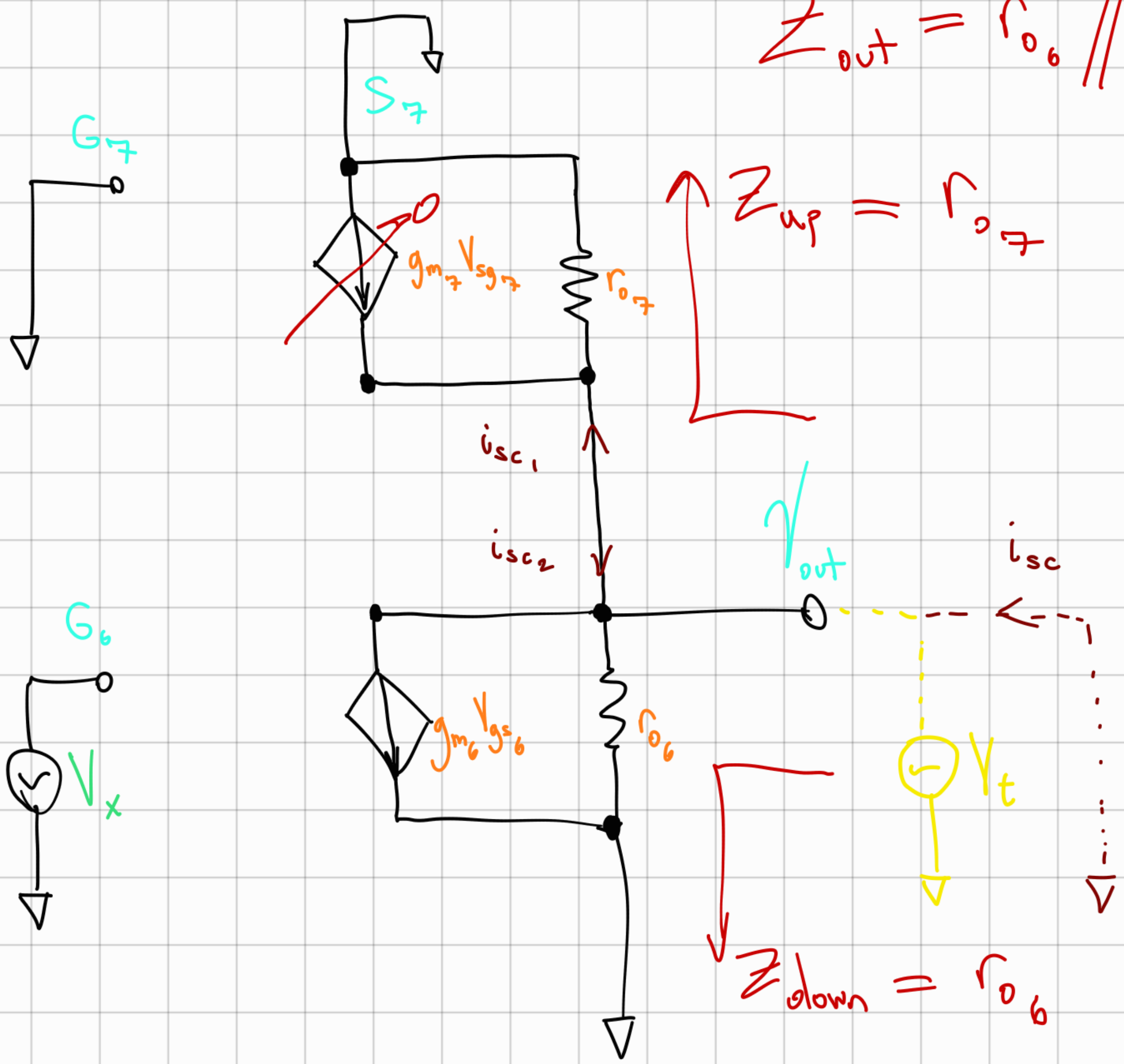
$$\Rightarrow G_m = g_{m_1} \quad \& \quad R_{out} = r_{o_2} \parallel r_{o_4}$$

$$\Rightarrow V_x = -G_m V_{id} \cdot R_{out}$$

$$\Rightarrow \frac{V_x}{V_{id}} = -g_{m_1} \cdot r_{o_2} \parallel r_{o_4}$$

Small-signal Model (Stage 2)

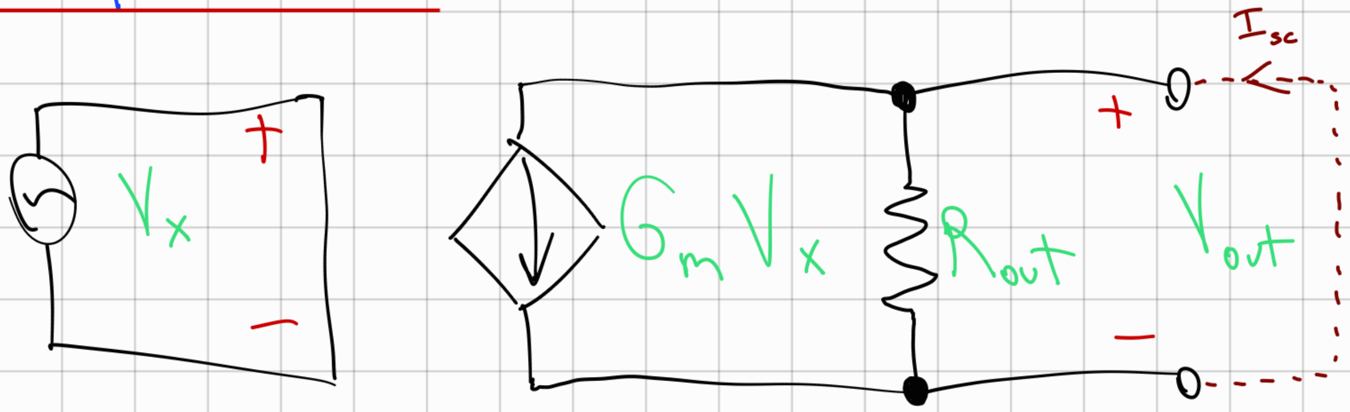
$$Z_{out} = r_{o_6} \,//\, r_{o_7}$$



$$i_{sc_1} = \cancel{\frac{V_{out}}{r_{o_6}}}^{\,0} + g_{m_6} V_x$$

$$i_{sc_2} = \cancel{\frac{V_{out}}{r_{o_7}}}^{\,0} \Rightarrow i_{sc} = g_{m_6} V_x$$

Two-port Model



$$\Rightarrow I_{sc} = G_m \cancel{V_x} = g_{m_6} \cancel{V_x} = i_{sc}$$

$$\Rightarrow G_m = g_{m_6} \quad \& \quad R_{out} = r_{o_6} \,//\, r_{o_7}$$

$$\Rightarrow V_{out} = -G_m V_x \cdot R_{out}$$

$$\Rightarrow \frac{V_{out}}{V_x} = -g_{m_6} \cdot r_{o_6} \,//\, r_{o_7}$$

Full Two-port Model

$$\Rightarrow \quad A_{v_d} = \frac{V_x}{V_{in,p} - V_{in,n}} \cdot \frac{V_{out}}{V_x}$$

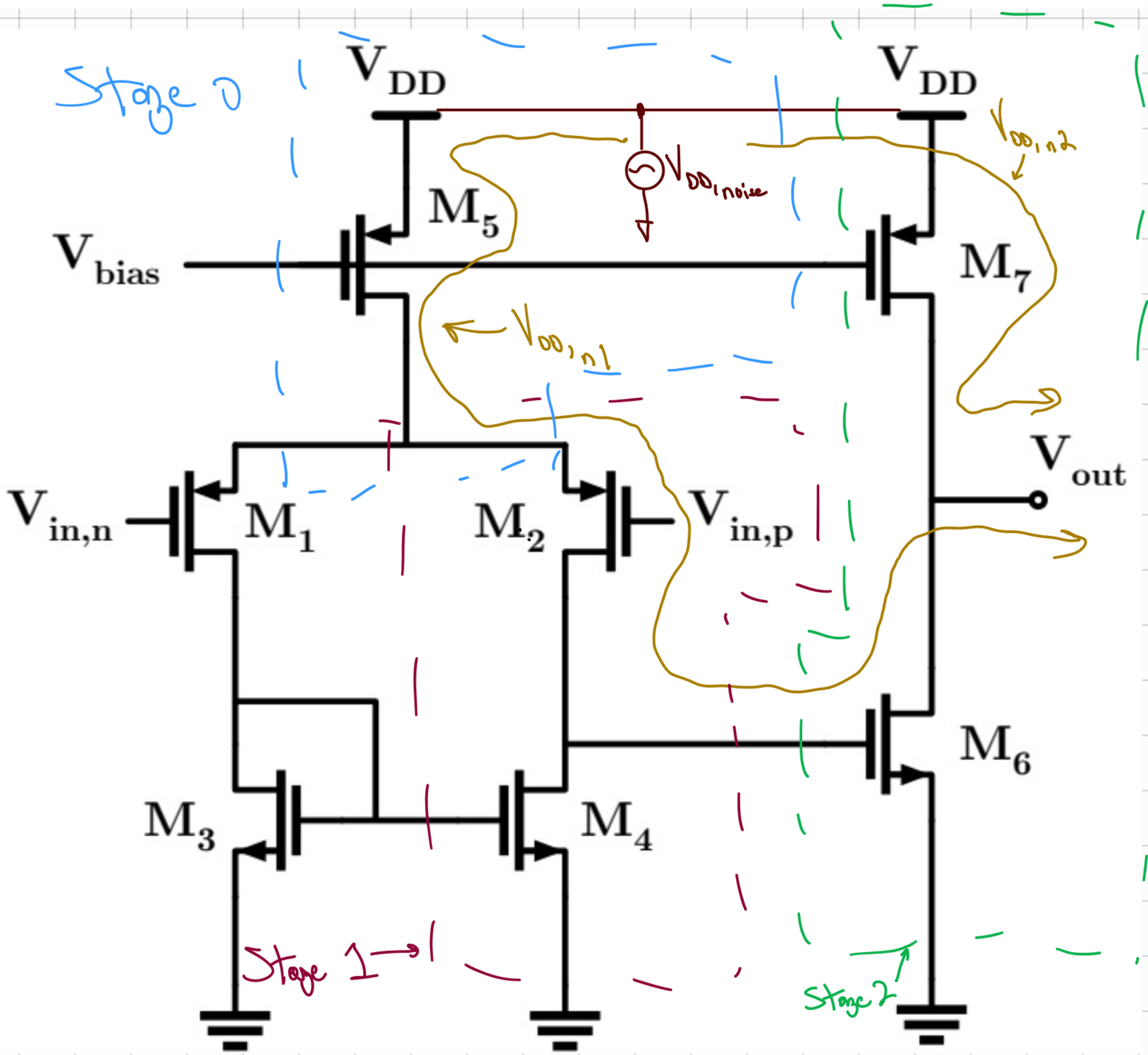
$$= \frac{V_x}{V_{id}} \cdot \frac{V_{out}}{V_x}$$

$$= \left(-g_{m_1} \cdot r_{o_2} \,//\, r_{o_4}\right)\left(-g_{m_6} \cdot r_{o_6} \,//\, r_{o_7}\right)$$

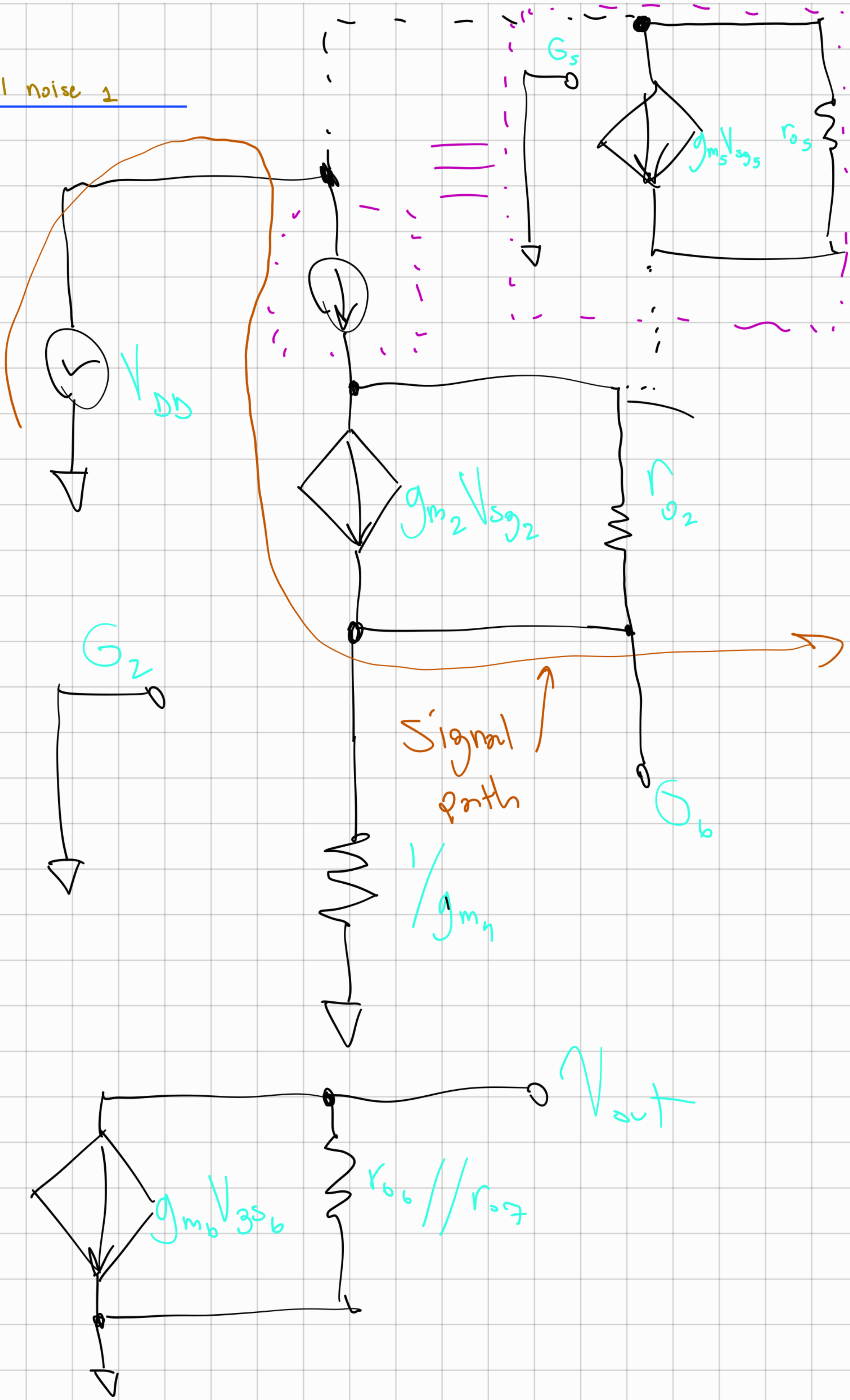
$$\boxed{\therefore A_{v_d} = g_{m_1} g_{m_6} \left(r_{o_2} // r_{o_4}\right)\left(r_{o_6} // r_{o_7}\right)}$$

(b) Now consider that V_{DD} has a noise associated with it, i.e. a small-signal AC source of $v_{dd,n}$ in series with the DC V_{DD}. Calculate the gain from $v_{dd,n}$ to the output, $A_{vp+} = \frac{v_{out}}{v_{dd,n}}$.

Hints: Noise has two paths to reach the output: through M_7 and through M_5. Consider them separately and add them up with the correct sign later. When considering the path through M_5, notice that M_2 is acting as a common gate amplifier. Recall from our discussions that V_{DS} values of M_3 and M_4 track each other in common mode excitations.



V_{DD}, noise 1


G_5
$g_{m_5}V_{sg_5}$
r_{o_5}
V_{DD}
$g_{m_2}V_{sg_2}$
r_{o_2}
G_2
Signal path
G_6
$1/g_{m_4}$
V_{out}
$g_{m_6}V_{gs_6}$
$r_{o_6} // r_{o_7}$

$$A_{v_0} = g_{m5} \cdot \left(\cancel{r_{o5}} \,\|\, 1/g_{m2}\right)$$

$$A_{v_1} = g_{m2} \cdot \left(\cancel{r_{o2}} \,\|\, 1/g_{m4}\right)$$

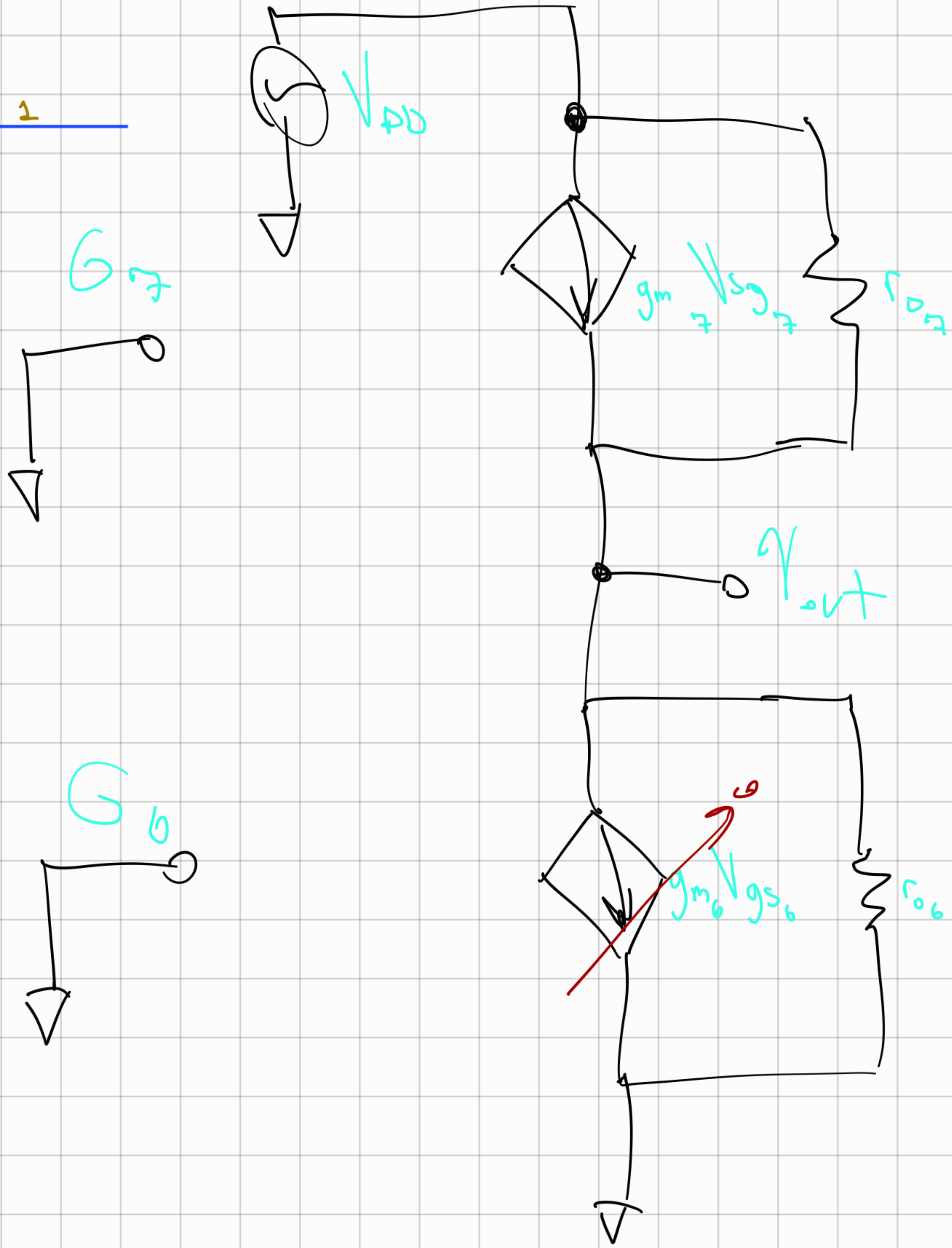
$$A_{v_2} = -g_{m6} \cdot \left(r_{o6} \,\|\, r_{o7}\right)$$

* Assume $r_{o5}, r_{o2} \gg g_{m2}, g_{m4}$

$$A_v = -\cancel{g_{m2}} g_{m5} g_{m6} \cdot \frac{1}{\cancel{g_{m2}} g_{m4}} \cdot r_{o6} \,\|\, r_{o7}$$

$$\boxed{\therefore A_{v_{cm_1}} = \frac{-g_{m5} g_{m6}}{g_{m4}} \cdot r_{o6} \,\|\, r_{o7}}$$

V_{DD}, noise 1



$$\Rightarrow \boxed{A_{V_{CM_2}} = g_{m_7} \cdot r_{o_7} \,//\, r_{o_6}}$$

$$\Rightarrow A_{v_{cm}} = A_{v_{cm_1}} + A_{v_{cm_2}}$$

$$= \frac{-g_{m_5} g_{m_6}}{g_{m_4}} \left(r_{o_6} \parallel r_{o_7} \right) + g_{m_7} \left(r_{o_7} \parallel r_{o_6} \right)$$

$$\boxed{\therefore A_{v_{p+}} = \left[\left(\frac{-g_{m_5} g_{m_6}}{g_{m_4}} \right) + g_{m_7} \right] \cdot r_{o_7} \parallel r_{o_6}}$$

(c) Using your previous results, what is the PSRR+ of this amplifier?

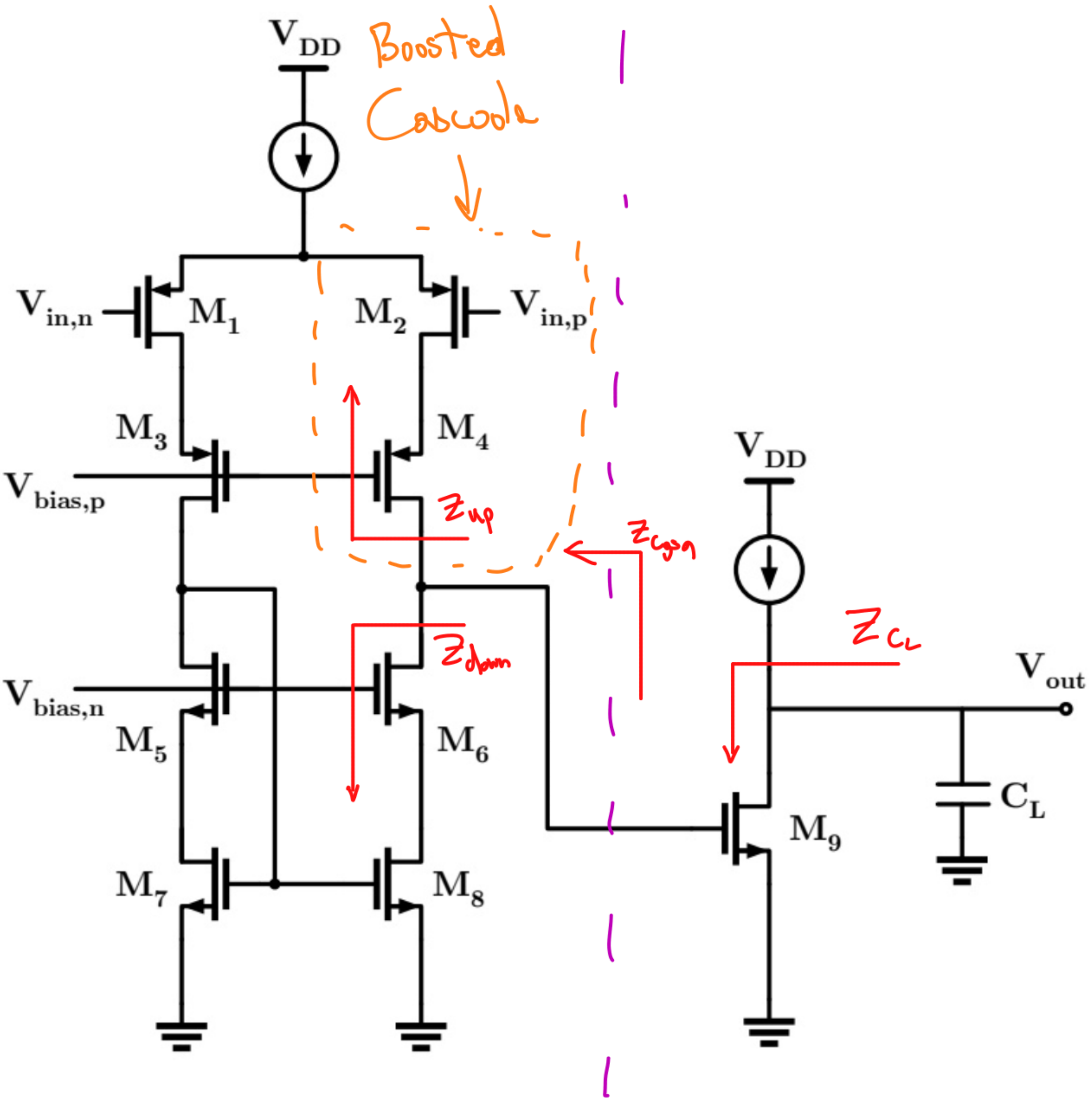
$$PSRR^+ = \left| \frac{A_{v_{DM}}}{A_{v_{p+}}} \right|$$

$$= \frac{g_{m_1} g_{m_6} (r_{o_2} \| r_{o_4}) \cancel{(r_{o_6} \| r_{o_7})}}{\frac{(-g_{m_5} g_{m_6})}{g_{m_4}} + g_{m_7} \cdot \cancel{r_{o_7} \| r_{o_6}}}$$

$$\boxed{\therefore\ PSRR^+ = \frac{(-g_{m_5} g_{m_6})}{g_{m_4}} + g_{m_7} \cdot r_{o_2} \| r_{o_4}}$$

Problem 2 - Miller Compensation of Two-Stage Amplifiers

There are applications we want a really high DC gain, and in those cases the workhorse amplifier in Problem 1 doesn't always cut it. One idea to improve the gain is to make the first stage gain higher by moving to the "telescopic cascode" topology, which is a power efficient topology that provides a high gain. In this problem we will analyze the Miller compensation of this two-stage amplifier. Assume that symmetric transistors in the differential amplifier share the same small signal parameters.



We want to use this amplifier in a feedback loop with feedback factor $\beta = 1/2$. The load capacitor C_L is very large ($C_L > g_m r_o C_{gs}$). Other than C_L, only consider the C_{gs} of the transistors, ignore any other capacitance. You may approximate $g_m r_o >> 1$ wherever appropriate. Assume all current sources are ideal.

Boosted Cascode $R_{out} \cong g_m r_o^2$

(a) Find the DC loop gain $H\beta$. Estimate the dominant pole frequency and the first non-dominant pole frequency.

Because of the virtual gand,
we only need the transconductance
of the first stage, and the
output resistance.

$$\Rightarrow Z_{up} \cong R_{th,d_4} \quad \& \quad Z_{down} \cong R_{th,d_6}$$

$$\Rightarrow R_{th_{d_4}} = r_{o_4}\left(1 + g_{m_4} r_{o2}\right) + r_{o2}$$

$$\cong g_{m_4} r_{o_2} r_{o_4}$$

$$\Rightarrow R_{th_{d_6}} = r_{o_6}\left(1 + \frac{g_{m_6}}{g_{m_8}}\right) + \frac{1}{g_{m_8}}$$

$$\cong 2 r_{o_6}$$

$$\Rightarrow R_{out} = 2 r_{o_6} \,//\, g_{m_4} r_{o_2} r_{o_4}$$

$$\Rightarrow A_{v_1} = -\frac{g_{m_2}}{\cancel{2}} \cdot \left(\cancel{2}\, r_{o6} \,//\, g_{m_4} r_{o2} r_{o4} \right)$$

$$\Rightarrow A_{v_1} = -g_{m_2} \left(r_{o6} \,//\, g_{m_4} r_{o2} r_{o4} \right)$$

$$\cong -g_{m_2} r_{o6}$$

$$\Rightarrow A_{v_2} = -g_{m_9} r_{o9}$$

$$\boxed{\therefore \beta H(s) = \frac{g_{m_2} g_{m_9} r_{o6} r_{o9}}{2}}$$

The dominant pole is C_L.

The first non-dominant pole is C_{gs_9}.

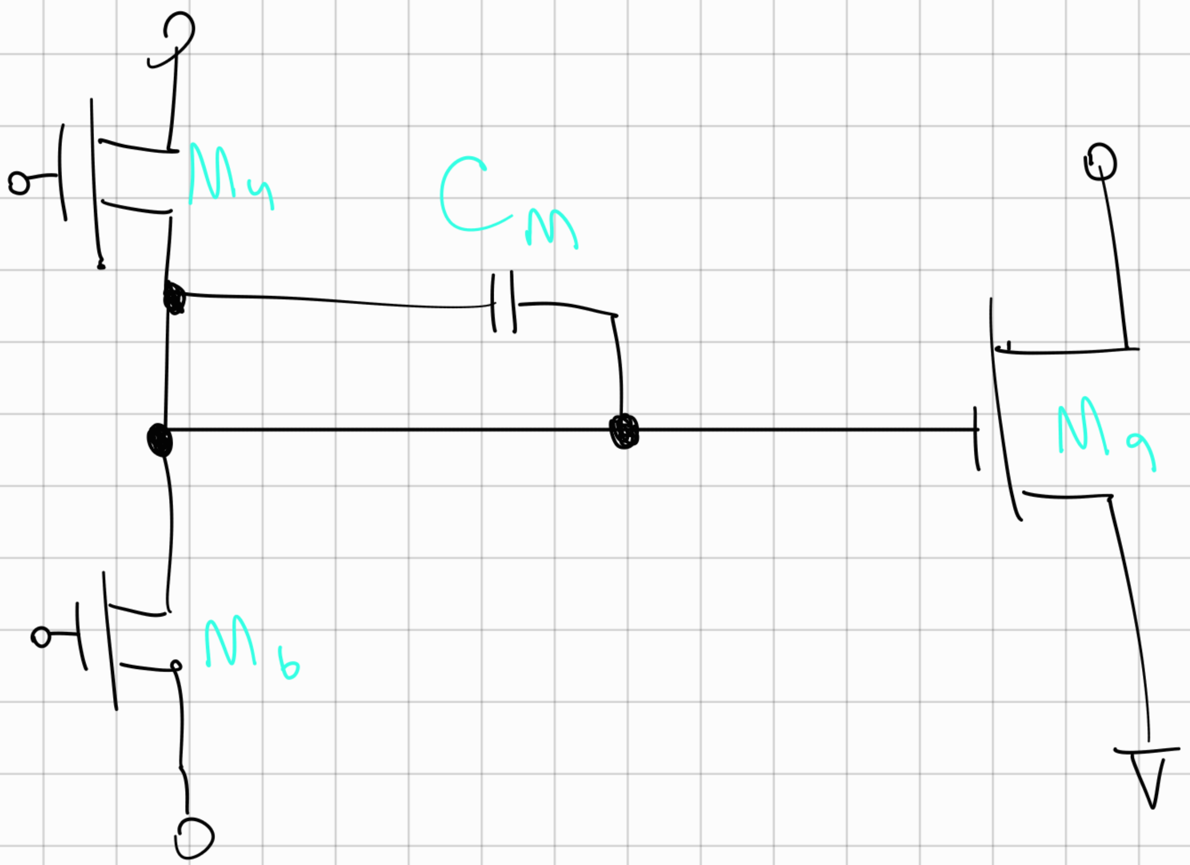
$$\Rightarrow Z_{C_L} = R_{th,d_9} \cong r_{o_9}$$

$$\therefore \quad \boxed{\omega_{p_1} \cong \frac{1}{r_{o_9} C_L}}$$

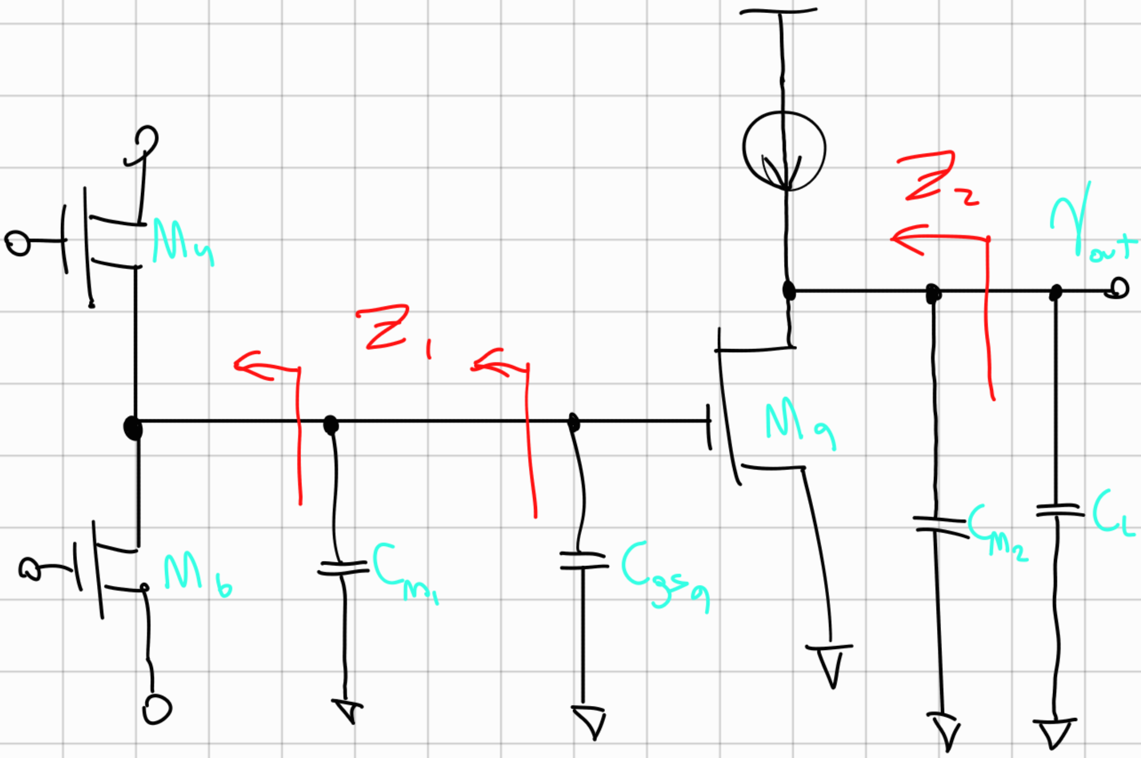
$$\boxed{\omega_{p_2} \cong \frac{1}{2r_{o_6} // g_{m_4} r_{o_2} r_{o_4} \cdot C_{gs_9}}}$$

(b) To Miller compensate this amplifier, where would you add a capacitor?

We would split the poles between the output of the differential stage and the input stage of the common source stage.



(c) Considering the capacitor you added, estimate the locations of the new dominant pole, first non-dominant pole, and the zero. Assume the dominant pole results from the added compensation capacitor.



$$Z_1 \cong 2r_{o_6} \qquad Z_2 \cong r_{o_9}$$

$$\Rightarrow C_{M_1} = C_M\left(1 - \left(-g_{m_9} r_{o_9}\right)\right)$$

$$= C_M\left(1 + g_{m_9} r_{o_9}\right)$$

$$\Rightarrow C_{M_2} = C_M\left(1 - \left(\frac{1}{-g_{m_9} r_{o_9}}\right)\right)$$

$$= C_M\left(1 + \underbrace{\cancel{\frac{1}{g_{m_9} r_{o_9}}}}_{\cong 0}\right) \cong C_M$$

$$W_{p_1} = \frac{-1}{Z_1 (C_{m_1} + C_{gs_9})}$$

$$= \frac{-1}{2 r_{o_6} (C_{m_1} + C_{gs_9})}$$

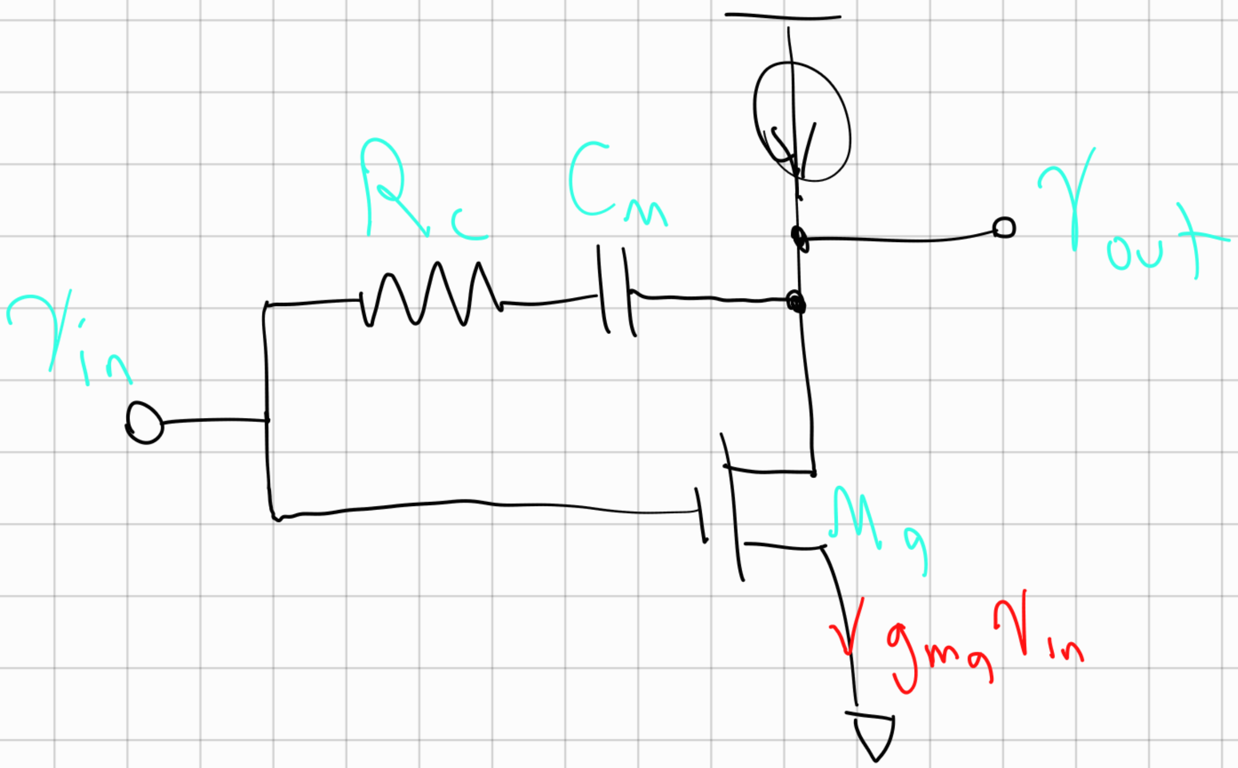
$$W_{p_2} = \frac{-1}{Z_2 (C_{m_2} + C_L)}$$

$$= \frac{-1}{r_{o_9} (C_{m_2} + C_L)}$$

$* \; C_{m_1} >> C_{m_2}$

$$\boxed{\begin{array}{l} \therefore \text{ New Dominant Pole} = W_{p_1} \\ \quad \text{First Non-Dominant Pole} = W_{p_2} \\ \quad \text{Zero} \cong \dfrac{g_{m_9}}{C_m} \end{array}}$$

(d) To move the RHP zero to infinity, we could add a resistor in series with the capacitor. What would its value be?



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$$g_{ma} \cdot V_{in} = \frac{V_{out} - V_{in}}{Z_c + Z_m}$$

$$= \frac{V_{out} - V_{in}}{R_c + 1/sC_m}$$

$$\Rightarrow V_{out} = V_{in}\left(1 - g_{ma}\left(R_c + \frac{1}{sC_m}\right)\right)$$

$$\Rightarrow \frac{V_{out}}{V_{in}} = \frac{sC_M - g_{m9}\left(1 + sR_cC_M\right)}{sC_M}$$

$\Rightarrow$ want $g_{m9} - sR_cC_M g_{m9} = g_{m9}$

$\Rightarrow$ set $R_c = \frac{1}{g_{m9}}$

$$\Rightarrow sC_M - g_{m9}R_cC_M s - g_{m9}$$

$$\Rightarrow sC_M - g_{m9}\frac{1}{g_{m9}}C_M s - g_{m9}$$

$$= \cancelto{0}{sC_M - 1 \cdot sC_M} - g_{m9}$$

$\Rightarrow$ Zero cancels / moves to ∞

$$\boxed{\therefore \; R_c = \frac{1}{g_{m9}}}$$

(e) Your colleague suggests that you can actually fine tune the value of the resistor to cancel your non-dominant pole to extend your bandwidth and improve your stability! What would be the value of the resistor in this case?

With the resistor, the zero becomes:

$$W_z = \left(\frac{g_{ma}}{C_M}\right)\left(\frac{1}{1 - g_{ma} R_C}\right)$$

$\Rightarrow$ Set equal to non-dominant pole and solve for R_C.

$$\frac{g_{ma}}{C_M(1 - g_{ma} R_C)} = \frac{-1}{r_{oa}(C_M + C_L)}$$

$$-C_M + C_M g_{ma} R_C = g_{ma} r_{oa} (C_M + C_L)$$

$$= g_{ma} r_{oa} C_M + g_{ma} r_{oa} C_L$$

$$\Rightarrow C_M g_{m_g} R_L = C_M + g_{m_g} r_{og} C_M + g_{m_g} r_{og} C_L$$

$$= C_M \left(1 + g_{m_g} r_{og}\right) + g_{m_g} r_{og} C_L$$

$$\boxed{\therefore R_L = \frac{C_M \left(1 + g_{m_g} r_{og}\right) + g_{m_g} r_{og} C_L}{C_M g_{m_g}}}$$

Problem 3 - Calculating Settling Errors

For this problem, you should use MATLAB/Python for all parts. No hand calculation is necessary. Provide your code alongside your solution.

Hint: For Python, ***control*** *package is your friend for this assignment. MATLAB has the* ***Control System Toolbox****. You can take the following Python code snippet as a starting point if you'll use Python:*

```
import control
import numpy as np
s = control.TransferFunction.s
wp1 = 2*np.pi*10e6
A0 = 1e4
t = np.linspace(0, 100e-12 , num =5000)
AOL = A0 /(1 + s/wp1)
ACL = AOL /(1+ AOL )
t, y = control.step_response(ACL , t)
```

(a) Assume an amplifier has an open loop response containing a single pole at 10MHz and a DC gain of 10^4. The amplifier is placed in unity gain feedback ($\beta = 1$). Plot the step response of the closed loop system. Then create a plot of settling error (log scale) vs time, and find the times needed to settle to within 10%, 1%, and 0.1% of the final value.

$$V_o(t) = V\left(1 - e^{-t/\tau}\right)$$

$$\Rightarrow |\text{Error}| = \left|e^{-t/\tau}\right|$$

$$\text{Error}\,\% = e^{-t/\tau} \times 100\,\%$$

Set $t = \tau \longrightarrow E = e^{-1} \times 100\% = 36\%$ error

$t = 5\tau \rightarrow E = e^{-5} \times 100\% = 0.7\%$ error

$$\boxed{\therefore \text{ For every } 10\times \Rightarrow 2.3\tau}$$


0
-90

(b) Repeat the previous part using the same amplifier, except now with a DC gain of 999.

(c) Compare the settling times from part (a) with those from part (b). Did they change significantly? If so, explain why.

$$1 \cdot \omega_{unity} = A \cdot \omega_{3dB}$$

$$\omega_0 = 10k \cdot 2\pi \cdot 10^6$$

$$= 6.28 \times 10^{10} \text{ Hz}$$

$$\simeq 63 \text{ GHz}$$

$$10\,\omega_0 = 180°$$

$$1 + \frac{s}{\omega_p} + A_0 = 0$$

Find the BW by setting C_c pole to 0, ⇒ Find break point,

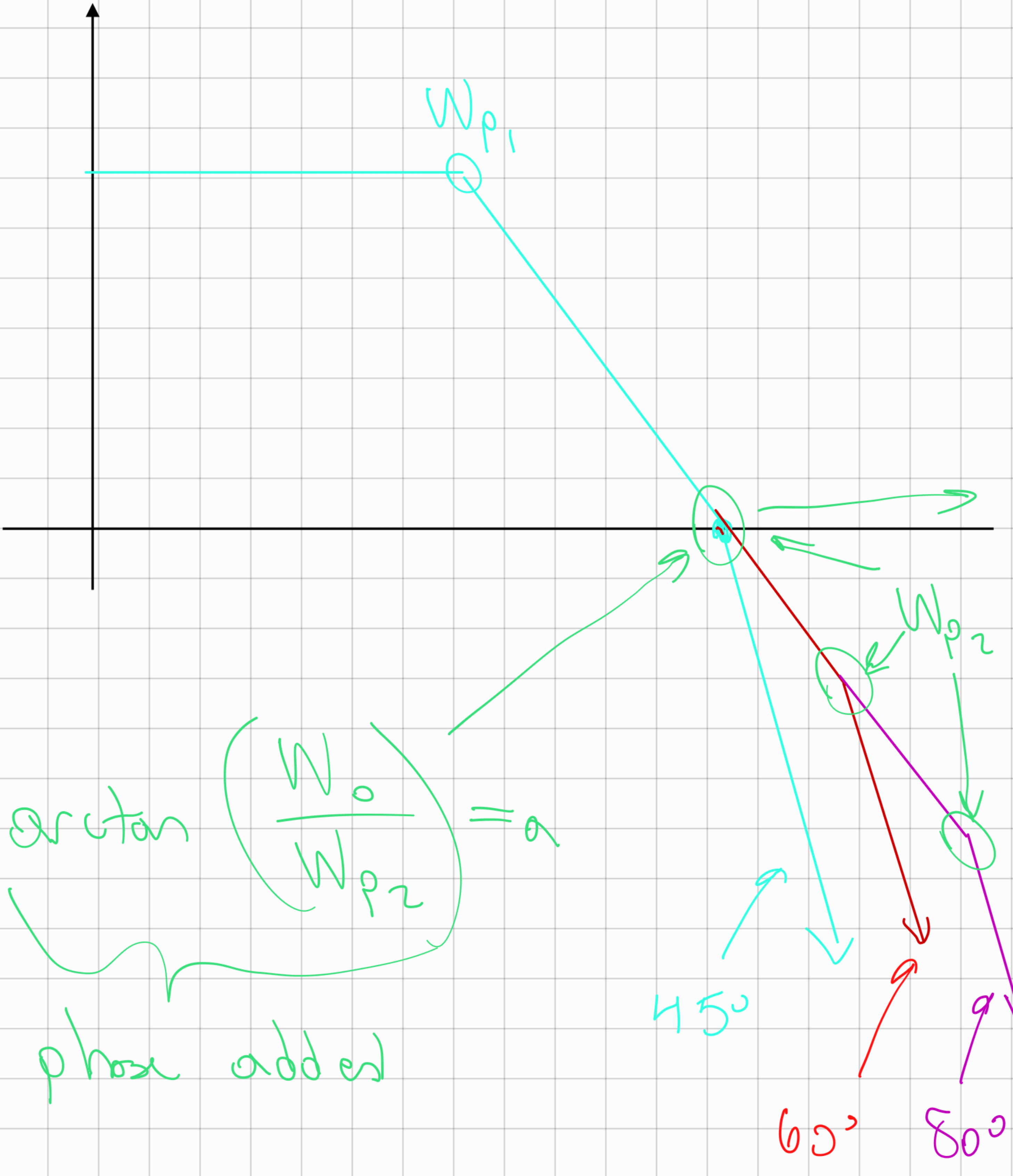
$$s = \omega_p \cdot -(A_0 + 1)$$

↓

$$\omega_{C_c} = \omega_p \cdot -(A_0 + 1)$$

(d) Now use the amplifier from part (a), except that the amplifier now has a second pole. Plot the closed loop step responses if the second pole is chosen to give 30°, 45°, 60°, 80° of phase margin.

(e) Using the same amplifier as the previous part, find the phase margin that gives the best settling time if your settling error margin is 10%. Repeat for 1% and 0.1%. Comment on your results. In particular, focus on the shape of the optimal step response as settling error margin decreases.



$$\underbrace{\arctan\left(\frac{W_o}{W_{p_2}}\right)}_{\text{phase added}} = a$$

$$PM = 180 - (90 + a)$$

* $\beta \cdot H(s) \uparrow \Rightarrow$ static error $\downarrow$