Topics

- Elementary Boolean operators
- Duality
- Basic theorems
- Algebraic minimization

Problems

Recall the truth table of the elementary Boolean operators. Solve the following system of equations for the variables A, B, C and D

$$\begin{cases} A' + A.B & = & 0 \\ A.C & = & A.B \\ A.B + A.C' + C.D & = & C'.D \end{cases}$$

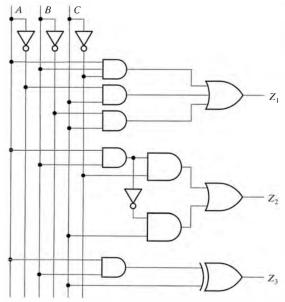
2 Verify, by perfect induction, the following simplification theorems. Write the dual counterpart of each theorem.

a)
$$x + x$$
. $y = x$

b)
$$x + x' \cdot y = x + y$$
 c) $x \cdot y + x \cdot y' = x$

c)
$$x. y + x. y' = x$$

- 3 Show that x'.y'.z' + x'.y'.z + x'.y.z' + x'.y.z + x.y.z' + x.y.z = x' + y
- 4 Show that x.y + x'.z + y.z = x.y + x'.z. Write the dual version of the previous expression.
- 5 Write the truth table of the XOR operation $x \oplus y$. Express this operator as an elementary sum of logic products.
- 6 Consider the logic circuits in the figure and show, by algebraic methods, that $Z_1 = Z_2 =$ Z_3 .



7 Use DeMorgan's laws to obtain the complement of:

a)
$$(x.y' + x'.y)$$

b)
$$(x. y + z. (x + y') + z. y)$$

- 8 Show that (a'.b + a.c).(a + b').(a' + c') = 0
- 9 Show that the dual of an XOR is an XNOR, that is $(x \oplus y)^D = (x \oplus y)'$.
- **10** Implement the XOR operation with NAND gates. Assume that both uncomplemented and complemented inputs are available.
- 11 Consider the following Boolean functions:

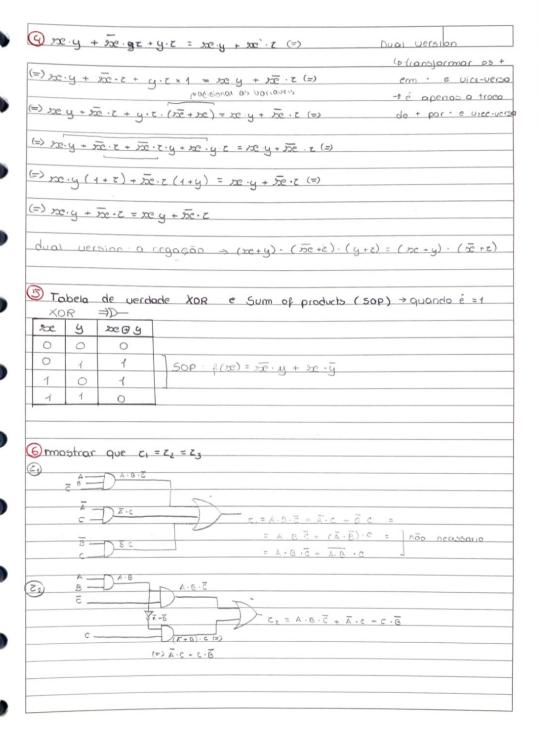
$$S = x \oplus y \oplus c_i$$

$$C_o = x \cdot y + c_i \cdot (x + y)$$

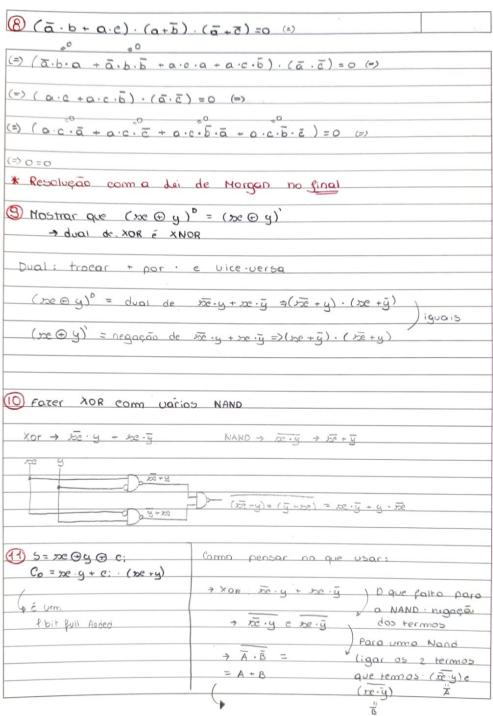
- a) Draw the logic circuit.
- b) Redraw the circuit using only NAND gates.
- 12 The Majority function M(x, y, z), is 1 whenever there are at least two inputs equal to 1.
 - a) Write the truth table for M(x, y, z).
 - b) From the truth table propose a Boolean expression for M(x, y, z).
 - c) Draw the corresponding logic circuit.
 - d) Show that using the set $S = \{M(x, y, z), NOT, "0"\}$ we can express any logic function. Suggestion: show how to implement the fundamental Boolean operators $\{"+",""\}$ using the elements of S.

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	-	A.C = A.	3		(=)	1.C=1.	0		/ (=)	1 C = 0		(=)		
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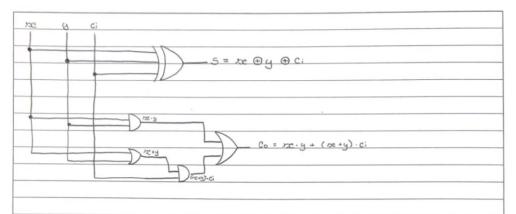
(3) indução perjeita -> substituir se ey portodos os valores possíveis



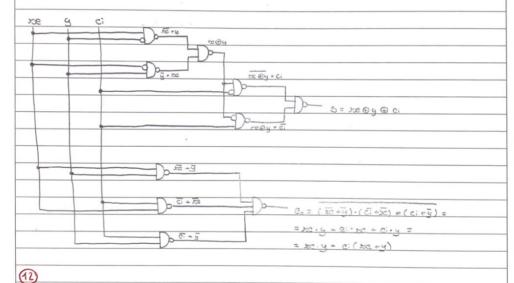
(2)	
A DA'B	
$c = \overline{(A \cdot B) \cdot c} + (A \cdot B) \cdot \overline{c} =$	
$= (\overline{A} + \overline{B}) \cdot c + A \cdot B \cdot \overline{c} =$	
= AB·C+ A·C+ B·C	
Concluimos que Z1=Z2=Z3	
② USOr a dei de Morgan : apenas negar	
a) (xe. g + xe.g)	
•	
→ o negação /complemento.	
· (xe·g) + xe·y) =	
$= (me. \overline{g}) \cdot (\overline{me} \cdot g) \qquad (basta fare(ista))$	
	f)
k .	
b) ****** (xe·y +z(xe+\bar{y}) + z·y)	
, , , , , , , , , , , , , , , , , , ,	
→ a negação / complemento: (xp.y+z.(xp+y)+z.y)	=
= xe.q . z(xe+y) . zy	
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a) Desenhar o exevito



b) Desenhar com portos NAND



H (xx,y,z)=1 quando pelo menos & input =1

a) Tabeia de verdade

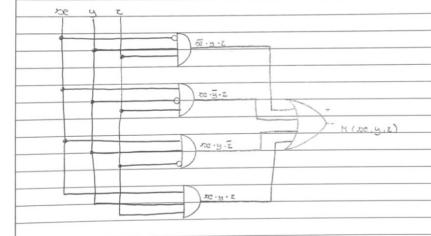
೨೦೮	9	ح	H(xx,y,z)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
4	0	0	0
1	0	1	1
1	1	0	1
1	1	1	4

b) Expressão booleana para M(xc.y.12)

Podermos forer SOP:

M(ne,y,z) = xe.y.z + xe.y.z + xe.y.z + xe.y.z

e) circuito logico



d) 5= [M(xe,y, E), NOT, "0"} -> significa que temos de provar que ao tornaramos uma das variaveis o complemento de zero , que é um tomos um output valido AND Para as ar quando termos o complemento vai dor sempre 1, por isso não usamos o complemento O mesmo acontece com outras portas logicas Não sei se o exercício pretendia que fixeremos isso, pode estar errado 3 com a lei de Morgan (ā-b+ac). (a+b). (ā+c) =0 (=) (=) $(\bar{a} \cdot b + a \cdot c) \cdot (a + \bar{b}) \cdot (\bar{a} + \bar{c}) = (e)$ (=) a.b+a.c + a+5 + a+E =1 (=) (=) (a+b) - (a+c) + a.b + a.c = 1 (=) (=) a.a + a.z + b.a + b.z + a.b , a.c =1 (=) E) a (c+c) + a (+b) + b.c =1 () (F) a+a+b·c =1 (F) 1=1