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Novel systematic mathematical computation based on the spiking frequency gate (SFG): Innovative organization of spiking computer

Soheila Nazari[a,b], Karim Faez[a,*]

[a] Department of Electrical Engineering, Amirkabir University of Technology, Tehran, Iran
[b] Nano Drug Delivery Research Center, Kermanshah University of Medical Sciences, Kermanshah, Iran

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ABSTRACT

The idea that the brain is composed of logical gates similar to IP cores of today's computers were provided by McCulloch and Pitts in 1943. In this paper, six structures for the interaction of dynamic neurons have been proposed to create neural circuits with spike coding that operate similarly to Boolean gates. It was concluded that the network of the dynamic model of spiking neurons and synapses called spiking frequency gates (SFG) can emulate the operations of digital gates AND, OR, NOT, NOR, XOR, and NAND. Also, an attempt was made to construct complex spiking circuits like full-adder, multiplexer, and arithmetic-logic-unit using cascade connections of SFGs. Extending simple designs to more complex spiking circuits can continue in order to access sophisticated computing tools based on SFGs. SFGs are not limited to zero and one and respond to the continuous range of spike train frequencies. Therefore, the information coding of SFGs is more powerful than Boolean gates. This paper illustrates a novel Boolean computation platform in a neural-like manner, which can provide a potential and clear horizon for designing neural circuits with complex applications. We hope that our results will lead to a deeper comprehension of the brain's functionalities and the development of new systematic methods based on the proposed spiking approach of Boolean logic gates.

1. Introduction

More than 70 years have passed since the publication of a seminal article "A logical calculus of the ideas immanent in nervous activity" [10]. They tried to understand how the brain, using the interactions of the interconnected networks of neurons, could produce very complex patterns. According to their approach, the brain consists of Boolean units that act based on the threshold function. Boolean units incorporate basic logic gates (e.g., AND, OR, NOT,…) to form the cores of today's computers. The development of the introduced simple framework of Boolean units was presented by von Neumann's novel paper, which introduced more flexible computational elements [35]. These concepts, together with Shannon's seminal work [43] in Boolean circuit optimization, form the infrastructure of today's computational framework. The development of artificial neural networks [13] and machine learning theories [18] are the debtor of the computational paradigm of McCulloch and Pitts. Actually, the development of the next generation of neural networks called Perceptron (linear classifier prototype)

* Corresponding author.
E-mail addresses: kfaez@aut.ac.ir, kfaez@ieee.org (K. Faez).

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[39], which was introduced by Frank Rosenblatt in 1958, had been triggered by previous scientists' efforts. Today, the recursive and multi-layered structures of this network have been developed and have found numerous practical applications [27]. Fairly we can conclude that the concept of Boolean neurons adopted from the first and second generation of neural networks had a limited impact on neuroscience.

With the rapid advancement of scientific reports in the field of neuroscience, the fundamental aspects of computational abilities of the nervous system remain unclear [37]. On the other hand, it is evident that the implementations of complex brain functions consist of the interconnected structure of the basic neural element called neurons, the functionalities of which have enhanced when operating as an ensemble [1]. Spiking neural networks (SNNs) are known as the third generation of neural network models. SNNs have increased the level of realism in a neural simulation, which incorporate the concept of time into the operating model of the neuron [12].

So far, two different aspects of the logical gates with spiking quiddity have been studied: the logic gate in the form of spiking neural P systems [44,14,19,25,20,28,50] and experimental observations [15,48].

The reason for the formation of spiking neural networks was to bring artificial neural network calculations closer to the computational approach of the nervous system [2]. The spiking neural P system (SN P system) can be classified as a static spiking neural network (SSNN) that considers firing rate and refractory time in neural activation compared to the second-generation neural networks [21]. In fact, the SN P system introduces a behavioral protocol of firing activity of neurons [21]. Pioneering works of designing the neural-like logic gates proposed computational structures based on SN P systems with a simple behavioral protocol instead of real dynamical neurons [20,28,50]. Dynamic spiking neural networks (DSNN) are the context that connects the nature of spiking networks to the biological aspect of the nervous system [22]. In DSNN, neurons and synapses are described by dynamic equations, which are defined in the computational neuroscience based on the ionic basis of electrical activity in the nervous system [17]. The distinction of this article with the previous works on the SN P system [44,14,19,25,20,28,50,7,16] is that we used DSNN to propose spiking gates based on the dynamic quiddity of the nervous system. Therefore, the computational model of the pyramidal neuron (PY), interneuron (IN), excitatory and inhibitory synapses AMPA and GABA, which are the basic elements of the hippocampus [30], was considered as the basis of the design of spiking frequency gates. The proposed approach compared to the logic gates using SN P systems has a more realistic approach of the brain dynamic. Therefore, it can be more compatible with information coding of the nervous system.

On the other hand, some experimental studies reinforce the view that nervous system consists of dynamic logic gates based on time-dependent logic modes [15,48]. Through the experimental paradigm, researchers [15,48] proved that a significant difference exists between the functional structure of brain logical operation and computer logic. It has been observed that unlike logic gates embedded on chips with a rigid truth-table, the function of the brain's gates is related to the frequency of their activity. Therefore, it was encouraged us to provide a new systematic approach and computational tools to develop traditional Boolean algebra in spiking networks. Inspired by these findings, we designed SFGs based on the dynamic model of neurons and synapses. We hope that machines consisting of SFGs might go beyond the computation paradigm of the universal Turing machine [29,47].

What we are facing now is the computational and cognitive ability of the nervous system against artificial neural networks. Compared to computational machines, the nervous system has a lower computational speed, but at the same time, the ability of the nervous system in generalization, decision-making, and learning relative to today's machines is significantly higher. Unique abilities of the nervous system in cognitive processes have been created by powerful information coding [9]. Therefore, by designing spiking gates based on the dynamic elements of the nervous system, powerful coding such as Prolate spheroidal wave functions [33], temporal coding [40] and so on can be used to extract and transfer information in the spiking computing system. With this approach, it can be hoped that the current computing systems that transmit data based on the sequence of zero-and-one will be replaced with the spiking machines, based on the dynamic model of neurons and synapses adapted from the computational model of brain. The horizon that illustrates our main motivation is to propose a dynamic structure for computational machines based on SFGs.

The proposed layout leads to a new class of mathematical computation based on SFGs. After that, by combining a set of SFGs, we constructed important spiking circuits (full-adder, multiplexer, arithmetic-logic-unit) with neural spiking gates.

These results can be expanded to a pioneering method for designing logic circuits working in a neural-like manner. On the other hand, multi-valued logic simulates fuzzy logic that is valuable in reasoning which is not fixed and exact. Boolean logics as the crisp logics are true or false logic, while fuzzy logic consists of variables with truth-value in the ranges between 0 and 1 [11]. Regarding the considered frequency range for the operation of SFGs, we will be able to introduce spiking gates with fuzzy coding in future works.

In the next section, we explain the dynamic model of neuron and synapse. Section 3 illustrates the designing procedure of spiking frequency gates. Section 4 demonstrates spiking circuits based on SFGs and finally, Section 5 concludes the paper.

2. Spiking model of neuron and synapse

In the last 100 years, neuroscientists have obtained detailed information about the function and structure of the brain. The fundamental processing units in the nervous system are neurons that are connected to each other with the complex pattern by synapses. Neural activity is modeled at several levels of dynamic richness and neural interactions. Multiple ion channels, pores in the cell membrane that react depending on the voltage and various chemical messengers, are consid-

ered in microscopic and detailed modeling. In microscopic models, each part of the neuron is modeled with a set of ionic equations that describe the role of that segment, which is called the compartmental model. On the higher levels of model simplification, accurate implementation of ionic mechanisms and spatial structure is not the modeling concern. In the mathematical model of neurons, regardless of the details of the operation of the ion channels, as a homogeneous unit, the neuron produces a spike if the sum of the input excitation is sufficiently high. Given that the precise mechanism of information processing and coding in the nervous system is poorly understood, spiking neural networks (SNN) inspired by the bio-model of spiking neurons have been presented for studying the neural system. In addition to the diversity of spiking neuron models, biological neurons play two major roles (excitatory and inhibitory) in the information transmission of neural circuits. Activity regulation of the excitatory neurons is done by inhibitory neurons and the main responsibility for the information transmission rests with the excitatory neurons. On the other hand, an essential aspect for an accurate modeling of neuronal interactions in SNNs is abstracted in the presence of synapses. Synapses can either be excitatory or inhibitory. Excitatory synapses increase the level of excitation so that input excitatory synapses increase the spiking activity of the neuron. Vice versa, Inhibitory synapses decrease the likelihood of the firing action potential and increase the level of inhibition.

In this paper, the dynamic of spiking neurons of SFGs are described by a leaky integrate and fire model. Membrane potential $v_k(t)$ of neuron k is defined by the following equation [30]:

$$\tau_m \frac{dv_k}{dt} = -v_k(t) + I + I_{AK}(t) - I_{GK}(t) \tag{1}$$

Membrane time constant $\tau_m$is 20 ms for excitatory neurons (pyramidal neuron) and 10 ms for inhibitory neurons (Interneuron). The fixed input current I is considered 2 mA. The received excitatory and inhibitory synaptic current by neuron k, is denoted by I_{Ak} (AMPA current) and I_{Gk} (GABA current), respectively. The resting potential (v_{res}) of all neurons is equal to zero. With a more complementary expression, when the membrane potential passes the threshold value, the neuron potential falls to the resting potential and the neuron cannot fire again for refractory time τ_{rp}, which is 2 ms for excitatory neurons and 1 ms for inhibitory neurons. Excitatory and inhibitory synaptic currents of neuron k can be obtained using auxiliary variables x_{Ak}, x_{Gk} as follows:

$$\tau_{dA} \frac{dI_{Ak}}{dt} = -I_{Ak} + x_{Ak} \tag{2}$$

$$\tau_{rA} \frac{dx_{AK}}{dt} = -x_{Ak} + \tau_m \left(J_{k-Pyr} \sum_{pyr} \delta(t - t_{k-pyr} - \tau_L) \right) \tag{3}$$

$$\tau_{dG} \frac{dI_{Gk}}{dt} = -I_{Gk} + x_{Gk} \tag{4}$$

$$\tau_{rG} \frac{dx_{Gk}}{dt} = -x_{AG} + \tau_m \left(J_{k-int} \sum_{int} \delta(t - t_{k-int} - \tau_L) \right) \tag{5}$$

where $t_{k-pyr.int}$ is the spike time received from pyramidal neurons/interneurons inputs connected to neuron k. Decay and rise time of the AMPA-type (GABA-type) synaptic current are denoted by $\tau_{dA}(\tau_{dG})$ and $\tau_{rA}(\tau_{rG})$, respectively. The latency of the post-synaptic currents is $\tau_L = 1$ ms. The efficacy of the connections from pyramidal neurons/interneurons inputs on neuron k are defined with $J_{k-pyr.int} = 0.01$.

In order to clarify the neural connections, all possible scenarios of excitatory and inhibitory interaction between pyramidal neurons and interneurons are shown in Fig. 1.

As is evident, the presynaptic pyramidal neuron excites postsynaptic neurons with excitatory synapse and presynaptic interneuron inhibits the postsynaptic neurons with inhibitory synapse. In the next section, with the combination of excitatory and inhibitory neurons and synapses, an attempt was made to construct spiking gates, which would help us to design a complex logical circuit in a neural-like manner.

3. Basic spiking frequency gates

In this section, spiking frequency gates using the dynamic model of neurons and synapses are constructed to emulate the function of basic logic gates AND, OR, NAND, NOR, NOT and XOR, respectively. In the designing procedure, only one type of excitatory and inhibitory neuron is used, which has a unique equation as a LIF neuron model. Neurons are thought to be able to encode analog and digital information because sensory and intrinsic information in the brain is transmitted by the activity of networks of neurons in interaction. In fact, information in the brain is encrypted (transmitted) in the form of a sequence of action potentials. Typically, in neural coding studies action potentials with different amplitude, phase, refractory time and duration are considered as identical stereotyped events. Here, we have maintained this aspect of the design and focused on the frequency of neurons activity in the gate performance, but different properties of action potentials can be used to extract information that can be considered in future works. If the spike apparent characteristics are ignored in information coding, the sequence of action potential or spike train is considered as the main event in time. The lengths

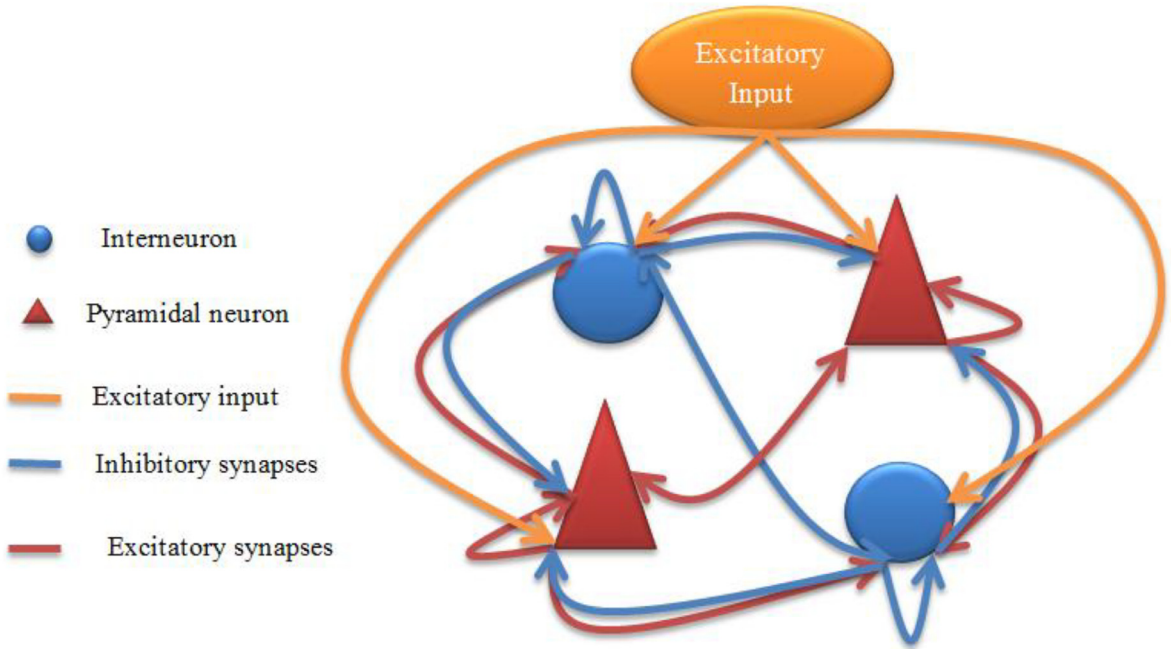


Fig. 1. The excitatory and inhibitory interaction of pyramidal neurons and interneurons on each other. Through the synaptic current AMPA and GABA, neurons have excitatory and inhibitory effects on their connected neurons.

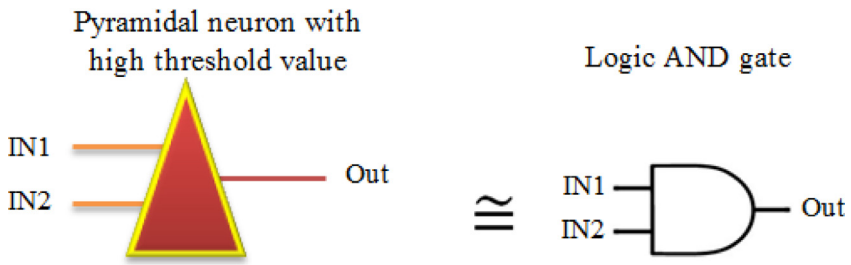


Fig. 2. Spiking AND gate emulates the operation of logic AND gate through the spike coding.

of inter-spike intervals between two consecutive spikes in a spike train contain information. In fact, information coding of spiking frequency gates due to the different coding schemes of the pattern of spike train can be powerful. The average number of spikes per unit time as a 'rate code' called 'firing rate' is important in information coding in the nervous system. Also, another main coding in the brain is 'temporal code', which is based on the precise timing of single spikes. Spiking frequency gates have been designed based on rate coding. In the spiking frequency gate, in order to receive spikes from the environment, multiple input synapses are used but only one output synapse is considered to emit computation results into the environment. As noted, 'rate code' is a dominant code in SFGs; therefore the inputs and outputs (logic values 0 and 1) are encoded by the frequency rate of the spikes. In the proposed design, if the input digit is 0, then the input synapse will deliver spikes at the rate of below 5 Hz from the environment; otherwise, if the input digit is 1, then the input synapse will deliver spikes at a rate of over 5 Hz. At the output synapses of the system, if the spike rate of the output synapse is at a frequency range of [0–5) Hz, then it denotes that the computation result of the spiking gate is 0. If the rate of output spikes is over 5 Hz, then the computation result is equal to 1. In other words, the logic values 0, 1 were encoded in the spike rate at a frequency range of [0–5) Hz and over 5 Hz, respectively.

The spiking AND gate can be emulated by a homogeneous and simple spiking neuron using one excitatory neuron (Pyramidal neuron) with the threshold value 35 mv ($v_{thr} = 35$ mv). Eq. (1) describes the dynamic equation of the neuron. The output synapse of the excitatory neuron is excitatory and excitatory or inhibitory input synapses to the Pyramidal neuron are denoted by Eqs. (3) and (5). The constructed spiking AND gate is shown in Fig. 2, which can imitate the operation of a logic AND gate.

The spiking AND gate has two input synapses IN1 and IN2 to receive spikes from the system, and one output synapse to generate the computation result. The four cases of inputs to spiking AND gate: 1,2 Hz (00); 3,7 Hz (01); 8,4 Hz (10); 9,10 Hz

Table 1
Result of spiking gates AND, OR, NAND, NOR, XOR in response to the spike train of input synapses.

Frequency of input spike train		Frequency of output spike train Out				
Frequency of input spike train IN1	Frequency of input spike train IN2	AND	OR	NAND	NOR	XOR
1 Hz (Boolean value 0)	2 Hz (Boolean value 0)	1.3 Hz	3.1 Hz	5.2 Hz	5.5 Hz	2.1 Hz
3 Hz (Boolean value 0)	7 Hz (Boolean value 1)	2.7 Hz	10.2 Hz	9.8 Hz	3 Hz	9.2 Hz
8 Hz (Boolean value 1)	4 Hz (Boolean value 0)	3 Hz	9.4 Hz	7.9 Hz	3.4 Hz	8.4 Hz
9 Hz (Boolean value 1)	10 Hz (Boolean value 1)	13.5 Hz	16.4 Hz	2.5 Hz	1.5 Hz	3.5 Hz

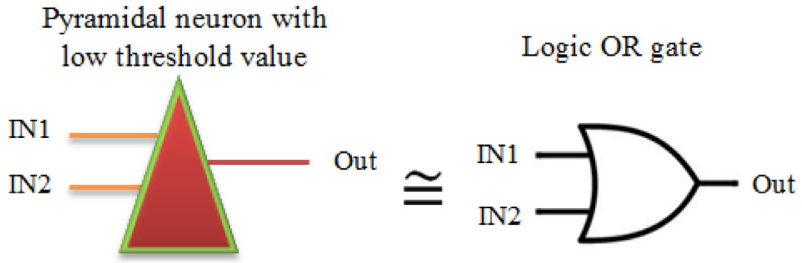


Fig. 3. Spiking OR gate imitates the operation of logic OR gate through the spike coding.

(11); are considered in Table 1. As can be seen from the results, in spiking gates, the logic values 0 & 1 are found at spike frequencies below 5 Hz and above 5 Hz, respectively.

As an example, if the inputs are IN1 = 1, IN2 = 0, synapse_IN1 receives spikes with a firing rate over 5 Hz and synapse_IN2 receives spikes with a firing rate below 5 Hz from the environment. Under these input conditions, the Pyramidal neuron emits spikes with a firing rate below 5 Hz, which imitates computation results of the logic AND gate when the result is 0. The computation process of spiking AND gate is quite similar to logic AND gate, with the difference that the Boolean numbers are coded at the frequency of the spikes. Briefly, in case that one or both input synapses deliver spikes with a firing rate below 5 Hz, the spike rate in output synapse is below 5 Hz. Also, if the firing rate of both input synapses is higher than 5 Hz, spikes with a frequency over 5 Hz are generated via the output synapse. Based on the description of spiking AND gate and the firing frequency in Table 1, it is clear that this spiking gate can correctly mimic the operation of a logic AND gate.

The spiking OR gate can be constructed using one excitatory neuron (Pyramidal neuron) with the threshold value 8 mv ($v_{thr} = 8$ mv). Eq. (1) describes the dynamic equation of neuron. The designed spiking OR gate is shown in Fig. 3, which can imitate the operation of a logic OR gate.

If the inputs are IN1 = 0, IN2 = 1, synapse_IN2 receives spikes with a firing rate over 5 Hz and synapse_IN1 receives spikes with a firing rate below 5 Hz from the environment. If the inputs are set in this arrangement, the Pyramidal neuron emits spikes with a firing rate over 5 Hz, which imitates the case in which computation result of the logic OR gate being 1. The computation result of spiking OR gate with a different input spike train is quite similar to its logical counterpart. Briefly, in case that one or both input synapses deliver spikes with a firing rate over 5 Hz, the spike rate in output synapse is over 5 Hz. Also, if the firing rate of both input synapses is lower than 5 Hz, spikes with frequency below 5 Hz are generated in the output synapse.

Based on the description of spiking OR gate and the firing frequency in Table 1, it is clear that this spiking gate can correctly emulate the operation of a logic OR gate with spike coding. Table 1 shows the firing frequency of input and output of the spiking OR gate when the spiking activity of input synapses correspond to the logic values 00, 01, 10, and 11, respectively. As is evident, the frequency of output fluctuations confirms the correct operation of this gate.

The combination of homogeneous spiking neurons was used to construct spiking NAND gate. The logic NAND gate can be emulated by one inhibitory neuron (Interneuron) with the threshold value 35 mv ($v_{thr} = 35$ mv) and two excitatory neurons with the threshold value 8 mv. Eq. (1) describes the dynamic equation of neurons. The output synapse of the inhibitory neuron is inhibitory and excitatory or inhibitory input synapses are denoted by Eqs. (3) and (5). The constructed spiking NAND gate is shown in Fig. 4, which can emulate the function of a logic NAND gate.

If the inputs set in IN1 = 1, IN2 = 1, synapses_IN1& IN2 receive spikes with a firing rate above 5 Hz from the environment. The configuration of Fig. 4, which represents the spiking NAND gate, with the spike trains above 5 Hz in the input synapses_IN1& IN2, generates spike train below 5 Hz in the output synapse. The computation process of spiking NAND gate with spike coding is quite similar to the logic NAND gate with Boolean coding. Briefly, in case that one or both input synapses deliver spikes with a firing rate below 5 Hz, the spike rate in the output synapse is over 5 Hz. Also, if the firing rate of both input synapses is higher than 5 Hz, spikes with frequency below 5 Hz are generated in the output synapse.

Based on the description of spiking NAND gate and the firing frequency in Table 1, it is clear that this spiking gate can correctly emulate the performance of a logic NAND gate. Table 1 shows the firing frequency of input and output of spiking

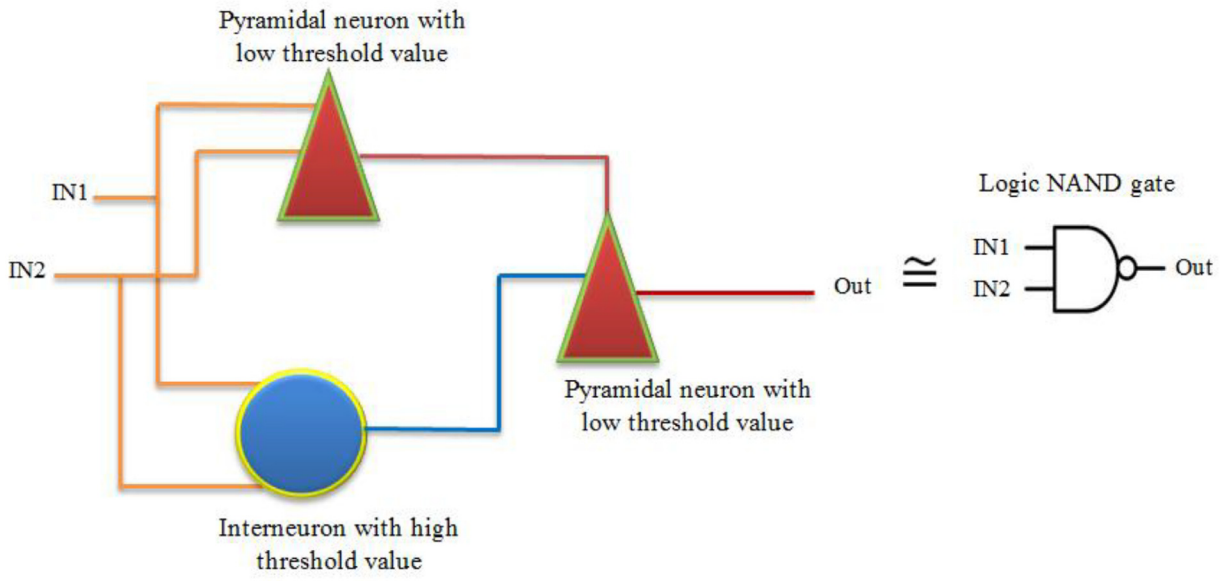


Fig. 4. Spiking NAND gate emulates the operation of logic NAND gate through the spike coding and excitatory/inhibitory neurons and synapses.

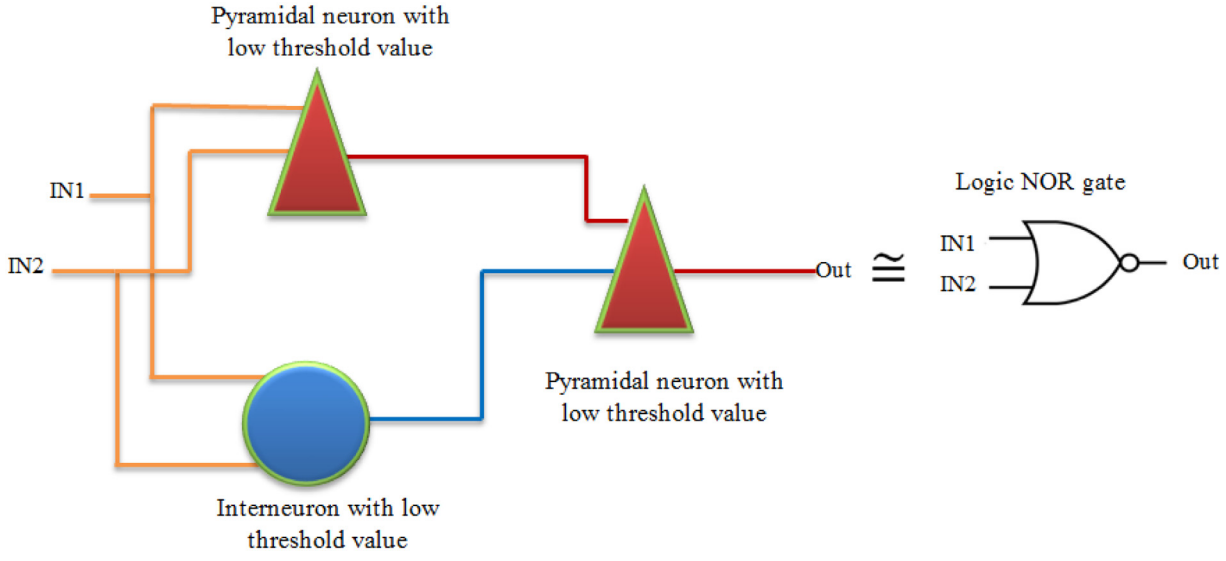


Fig. 5. Spiking NOR gate emulates the operation of logic NOR gate through spike coding.

NAND gate when the spiking activity of input synapses corresponded to the logic values 00, 01, 10, and 11, respectively. As is evident, the frequency of output fluctuations confirms the correct operation of this gate.

Simple connection of homogeneous spiking neurons in Fig. 5 can be used to construct a spiking gate, which imitates the operation of logic NOR gate. The spiking NOR gate can be simulated by one inhibitory neuron (Interneuron) with the threshold value 8 mv ($v_{thr} = 8$ mv) and two excitatory neurons with the threshold value 8 mv. Eq. (1) describes the dynamic equation of neurons and excitatory or inhibitory synapses denoted by Eqs. (3) and (5). The constructed spiking NOR gate is shown in Fig. 5, which can imitate the function of a logic NOR gate.

If the inputs are considered as IN1 = 1, IN2 = 0, synapse_IN1 receives spikes with a firing rate over 5 Hz and synapse_IN2 receives spikes with a firing rate below 5 Hz from the system. The computation result of the spiking NOR gate is quite similar to the case in which inputs of logic NOR gate are IN1 = 1, IN2 = 0. In this state of inputs, the system configuration of Fig. 5 emits spikes with a firing rate below 5 Hz into the environment, which imitates the computation process of the logic NOR gate when it is 0. Briefly, in case that one or both input synapses deliver spikes with a firing rate over 5 Hz, the spike rate in the output synapse is below 5 Hz. Also, if the firing rate of both input synapses is lower than 5 Hz, spikes are generated in output synapse with a frequency over 5 Hz.

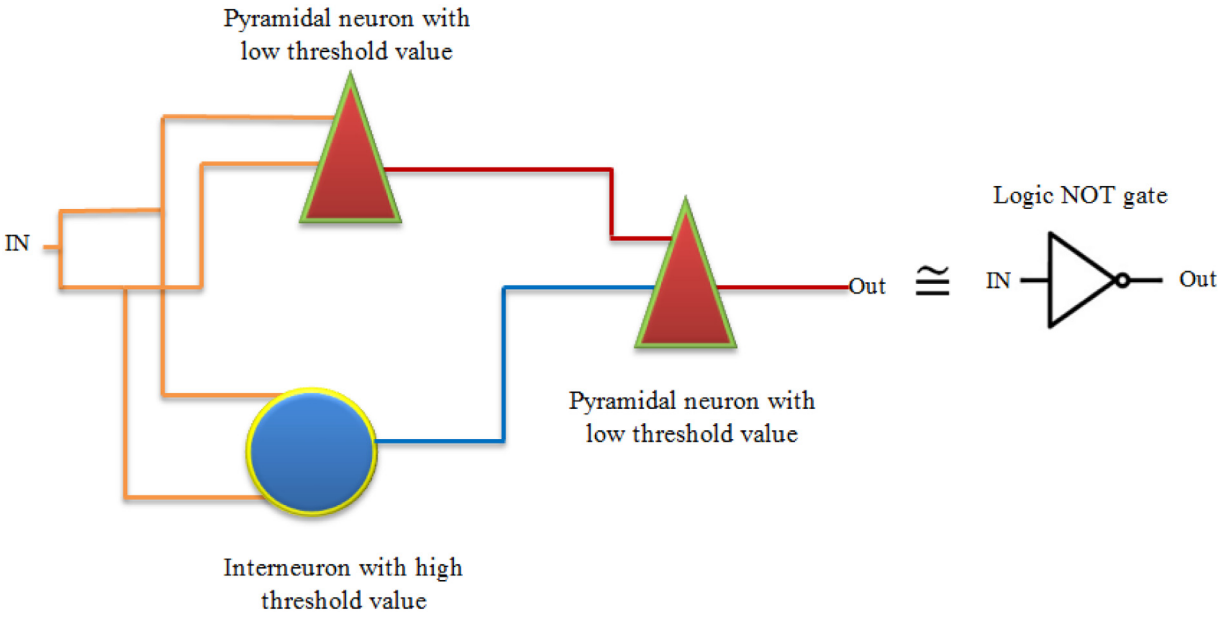


Fig. 6. Spiking NOT gate is constructed through the connection between two inputs of spiking NAND gates.

Table 2
Result of spiking NOT gate in response to the spike train of input synapse.

	Frequency of input spike train IN	Frequency of output spike train Out
NOT	1 Hz (Boolean value 0)	6 Hz spike train through AMPA synapses
	8 Hz (Boolean value 1)	3.4 Hz spike train through AMPA synapses

Based on the description of spiking NOR gate and the firing frequency in Table 1, it is evident that the spiking NOR gate with spike coding from the functional aspect imitate the operation of logic OR gate with Boolean coding. Table 1 shows the firing frequency of input and output of spiking NOR gate when the spiking activity of input synapses corresponded to the logic values 00, 01, 10, and 11, respectively. As is evident, the frequency of output fluctuations confirms the correct operation of this gate.

The spiking NOT gate can be constructed by connecting two inputs of the spiking NAND gate. The configuration of this spiking gate is shown in Fig. 6, which can imitate operation of the logic NOT gate.

If the input is IN = 1, synapse_IN receives spikes with a firing rate over 5 Hz from the environment and the output synapse delivers the spike train with a firing rate below 5 Hz to the system. The computation process of the spiking NOT gate is quite similar to its logical counterpart but with different coding.

Based on the computation process of spiking NOT gate and the firing frequency in Table 2, it is clear that this spiking gate can correctly imitate the operation of a logic NOT gate when the Boolean values have been translated to the frequency of spike trains. Table 2 shows the firing frequency of input and output of the spiking NOT gate when the spiking activity of input synapse corresponded to the logic value 0,1, respectively. As is evident, the frequency of output fluctuations confirms the correct operation of this gate.

The spiking XOR gate can be designed by connecting excitatory and inhibitory neurons with high threshold value (v_{thr} = 35 mv) and an excitatory neuron with low threshold value (v_{thr} = 8 mv). Excitatory neurons connect to other neurons with excitatory (AMPA) synapses, and inhibitory neurons with inhibitory (GABA) synapses are attached to other neurons. The constructed spiking XOR gate is shown in Fig. 7, which can imitate the operation of a logic XOR gate.

If the inputs are set to IN1 = 1, IN2 = 0, synapse_IN1 receives spikes with a firing rate over 5 Hz and synapse_IN2 receives spikes with a firing rate below 5 Hz from the environment and the spiking XOR gate generates the spike train in the output synapse by firing frequency above 5 Hz. This state is equivalent to the situation in which the logic XOR gate is derived with inputs 0,1 and logic value 1 has been generated. The computational result of spiking gates is quite similar to the logical gates, with the difference that spike based gates work unlike logic gates with spike coding. Briefly, in case that one input synapses delivers spikes with a firing rate above 5 Hz and another input delivers spikes with a firing rate below 5 Hz, the spike rate in output synapse is above 5 Hz. Also, if the firing rate of both input synapses is lower than 5 Hz or higher than 5 Hz, spikes with frequency below 5 Hz are generated in the output synapse.

Based on the description of spiking XOR gate and the reported firing frequency in Table 1, it is clear that this spiking gate can correctly emulate the operation of a logic XOR gate. Table 1 shows the firing frequency of input and output of the

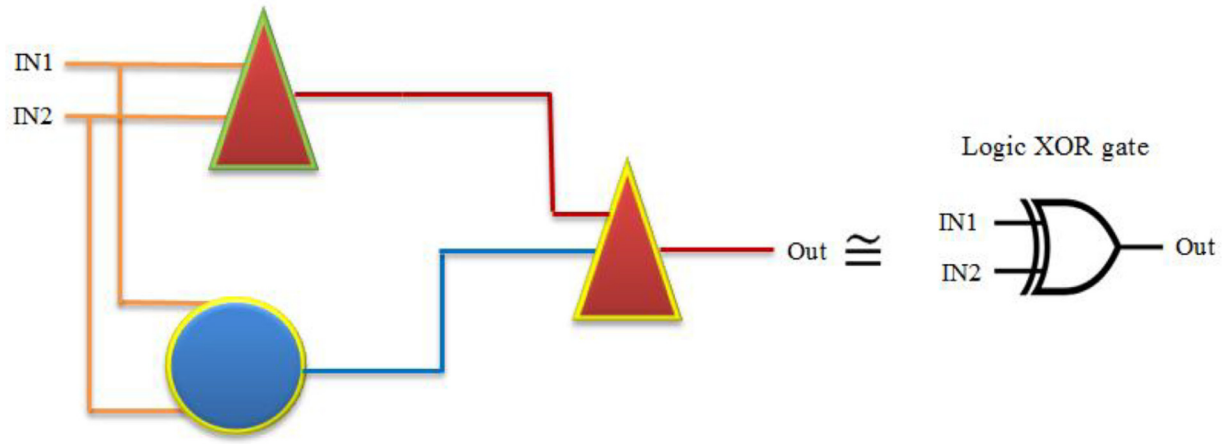


Fig. 7. Spiking XOR gate emulates the operation of logic XOR gate through spike coding.

Table 3
Input spike trains drive the spiking full adder to omit spike train corresponding to the result of Boolean full adder.

Full-adder	Frequency of input spike train c_i	Frequency of input spike train A	Frequency of input spike train B	Frequency of output spike train s	Frequency of output spike train c_0
	2 Hz (Boolean value 0)	1 Hz (Boolean value 0)	2 Hz (Boolean value 0)	1.5 Hz spike train through AMPA synapses	2.6 Hz spike train through AMPA synapses
	2 Hz (Boolean value 0)	3 Hz (Boolean value 0)	7 Hz (Boolean value 1)	7.8 Hz spike train through AMPA synapses	4 Hz spike train through AMPA synapses
	2 Hz (Boolean value 0)	8 Hz (Boolean value 1)	4 Hz (Boolean value 0)	8 Hz spike train through AMPA synapses	3.8 Hz spike train through AMPA synapses
	2 Hz (Boolean value 0)	9 Hz (Boolean value 1)	10 Hz (Boolean value 1)	1 Hz spike train through AMPA synapses	10 Hz spike train through AMPA synapses
	7 Hz (Boolean value 1)	1 Hz (Boolean value 0)	2 Hz (Boolean value 0)	7 Hz spike train through AMPA synapses	3.5 Hz spike train through AMPA synapses
	7 Hz (Boolean value 1)	3 Hz (Boolean value 0)	7 Hz (Boolean value 1)	2.1 Hz spike train through AMPA synapses	9.7 Hz spike train through AMPA synapses
	7 Hz (Boolean value 1)	8 Hz (Boolean value 1)	4 Hz (Boolean value 0)	2.4 Hz spike train through AMPA synapses	8.9 Hz spike train through AMPA synapses
	7 Hz (Boolean value 1)	9 Hz (Boolean value 1)	10 Hz (Boolean value 1)	8.5 Hz spike train through AMPA synapses	11 Hz spike train through AMPA synapses

spiking XOR gate when the spiking activity of input synapses correspond to the logic values 00, 01, 10, and 11, respectively. As is evident, the frequency of output fluctuations confirms the correct operation of this gate.

A combination of SFGs can be used to construct spiking circuits for engineering applications, which can provide a profound understanding of the coding mechanism of the brain. Spiking circuits can also guide us in exploring the mechanism of human decision making and reasoning.

4. Spiking circuits using SFGs

Boolean circuits are considered as the formal models in designing digital circuits with the logic combination. A full adder (FA) is a popular digital circuit that adds three one-bit binary numbers, two operands and a carry bit. Full adders are implemented with a combination of logic gates XOR, AND, OR in hardware. The connected full adders can add an arbitrary length of bits, such as 32 or 64 bits.

Also, a multiplexer or mux 2–1 is a combinational circuits that selects input signals and forwards the selected input into a single output line. This logic circuit can be designed by a combination of logic gates AND, OR, NOT and it can be extended to Mux4-1 and so on. By combining the designed neural-like logic gates in Section 3, two instances of spiking circuits full-adder and Mux are developed, which imitate the performance of the corresponding Boolean circuits by spike coding. In the following, the proposed spiking gates in Section 3 are applied to design corresponding spiking circuits of Boolean full adder and multiplexer in Fig. 8. The spiking circuits shown in Fig. 8 are called spiking full adder and multiplexer. It can be easily investigated that the constructed homogenous spiking circuits in Fig. 8 can mimic the computational process and result of Boolean circuits full adder and multiplexer. Tables 3 and 4 show that these spiking circuits can imitate the performance of their Boolean counterpart with spike coding.

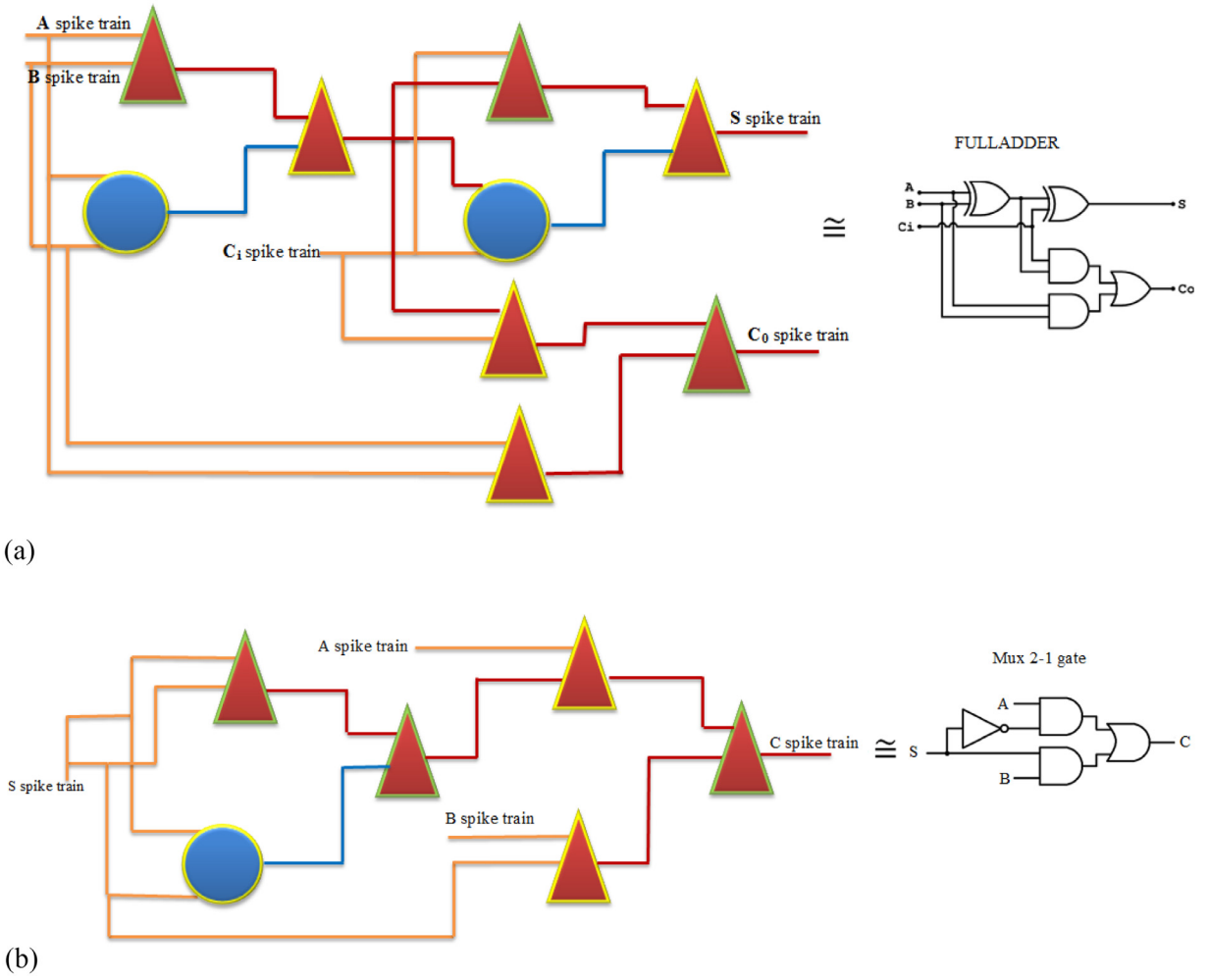


Fig. 8. Spiking full adder (a) and multiplexer 2–1 (b). Each spiking circuits has been designed by a combination of spiking frequency gates, which imitates the operation of their counterpart Boolean circuits through spike coding.

Table 4
Input spike trains drive the spiking Mux to generate the spike train corresponding to the result of Boolean Mux.

Mux	Frequency of input spike train s	Frequency of input spike train A	Frequency of input spike train B	Frequency of output spike train c
	2 Hz (Boolean value 0)	1 Hz (Boolean value 0)	2 Hz (Boolean value 0)	3.4 Hz spike train through AMPA synapses
	2 Hz (Boolean value 0)	3 Hz (Boolean value 0)	7 Hz (Boolean value 1)	3 Hz spike train through AMPA synapses
	2 Hz (Boolean value 0)	8 Hz (Boolean value 1)	4 Hz (Boolean value 0)	9.1 Hz spike train through AMPA synapses
	2 Hz (Boolean value 0)	9 Hz (Boolean value 1)	10 Hz (Boolean value 1)	11.5 Hz spike train through AMPA synapses
	7 Hz (Boolean value 1)	1 Hz (Boolean value 0)	2 Hz (Boolean value 0)	2.2 Hz spike train through AMPA synapses
	7 Hz (Boolean value 1)	3 Hz (Boolean value 0)	7 Hz (Boolean value 1)	7.6 Hz spike train through AMPA synapses
	7 Hz (Boolean value 1)	8 Hz (Boolean value 1)	4 Hz (Boolean value 0)	3.4 Hz spike train through AMPA synapses
	7 Hz (Boolean value 1)	9 Hz (Boolean value 1)	10 Hz (Boolean value 1)	10.8 Hz spike train through AMPA synapses

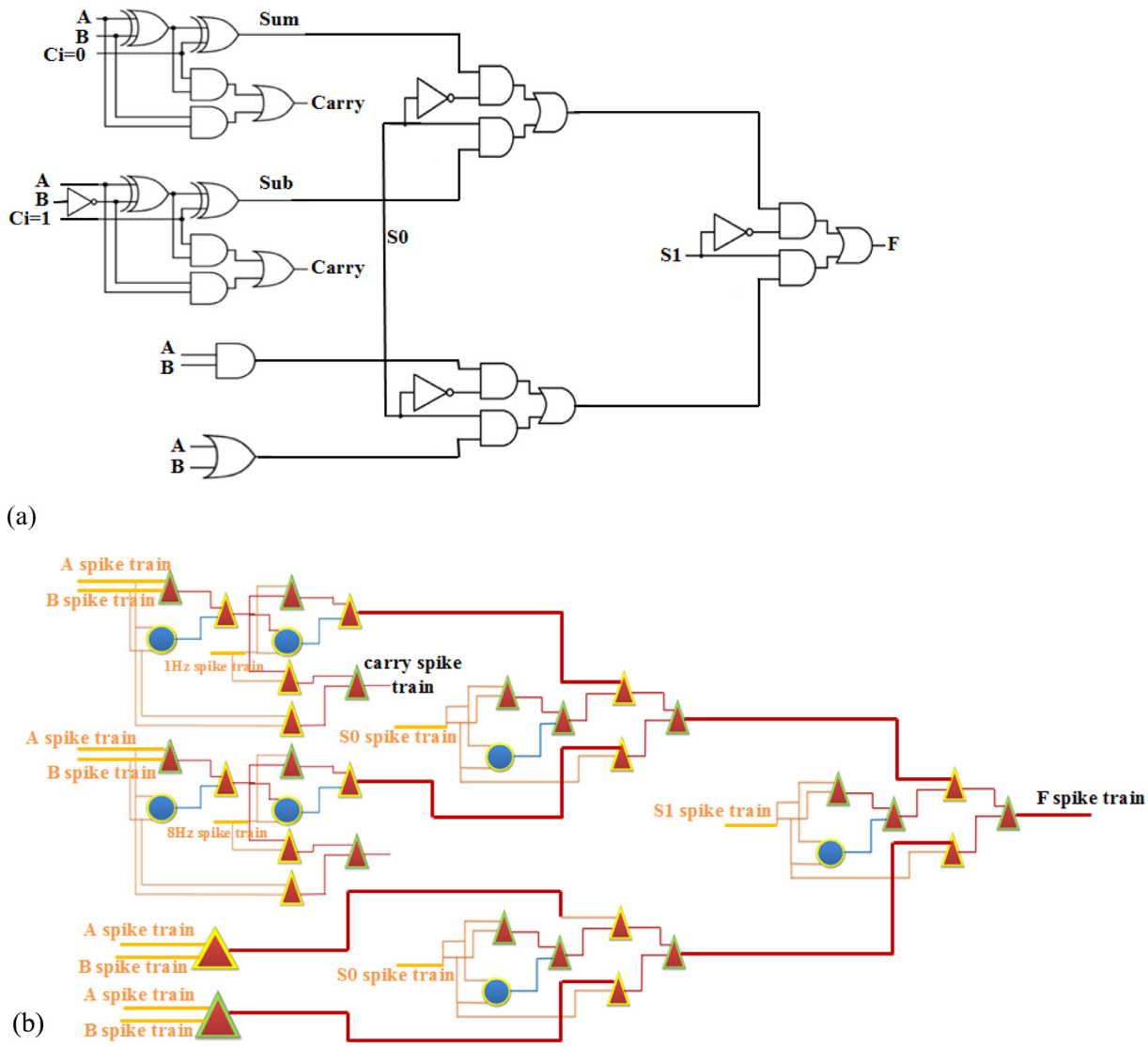


Fig. 9. (a), (b) denote Boolean and spiking ALU. Spiking circuit imitates the operation of its counterpart Boolean circuit through the rate spike coding.

Tables 3 and 4 show the firing frequency of input and output of spiking full-adder and multiplexer when the spiking activity of input synapses corresponded to the logic values 000, 001, 010, 011, 100, 101, 110, and 111 respectively. As is evident, the frequency of output fluctuations confirms the correct operation of these spiking circuits.

We proposed a new computational method in which the brain may consist of spiking frequency gates (SFGs) so that information transmission and coding of the nervous system may follow the operation of SFGs. The brain is formed by the interconnected neural networks. The proposed spiking gates can be embedded in large interconnected networks and construct a piece of the brain as the processing unit. The analysis and computational process of traditional Boolean circuits can be modified to the new systematic method based on spiking elements. The new computational platform based on spiking gates can be useful in the implementation of the brain's functionalities using conventional computers.

Logic gates and circuits have high-performance speeds while the spiking gate cannot surpass the logic gate speed due to the created constraint via the refractory time of neurons. On the other hand, the coding rule in the spiking gates is much richer than logical gates. Logical gates react only to zero and one Boolean inputs. In other words, information is encoded in the sequence of zeros and ones. While spiking gates react to spike trains with a wide range of firing frequencies, information encoding in spiking gates can be compatible with the information encryptions of the spike train in the nervous system, which is the strength of the presented computational paradigm in this article.

In order to show the application of the proposed platform in the real-life system, in Fig. 9 an arithmetic-logic-unit (ALU) was designed which performs ADDITION and SUBTRACTION in the mathematical computational part, AND & OR in the

Table 5
Corresponding to the performance of Boolean ALU, spiking ALU produces the output spike train in response to the input excitation with rate spike coding.

ALU	Selects of ALU		Inputs of ALU		Output of ALU	Operational mode of ALU
	Frequency of select spike train S0	Frequency of select spike train S1	Frequency of input spike train A	Frequency of input spike train B	Frequency of output spike train F	
	2 Hz (Boolean value 0)	1 Hz (Boolean value 0)	2 Hz (Boolean value 0)	2 Hz (Boolean value 0)	2 Hz spike train through AMPA synapses	**Addition (s1s0:00)**
	2 Hz (Boolean value 0)	1 Hz (Boolean value 0)	2 Hz (Boolean value 0)	7 Hz (Boolean value 1)	6.9 Hz spike train through AMPA synapses	
	2 Hz (Boolean value 0)	1 Hz (Boolean value 0)	8 Hz (Boolean value 1)	1 Hz (Boolean value 0)	7.2 Hz spike train through AMPA synapses	
	2 Hz (Boolean value 0)	1 Hz (Boolean value 0)	6 Hz (Boolean value 1)	9 Hz (Boolean value 1)	4 Hz spike train through AMPA synapses	
	2 Hz (Boolean value 0)	8 Hz (Boolean value 1)	2 Hz (Boolean value 0)	2 Hz (Boolean value 0)	1 Hz spike train through AMPA synapses	**Subtract (s1s0:01)**
	2 Hz (Boolean value 0)	9 Hz (Boolean value 1)	2 Hz (Boolean value 0)	7 Hz (Boolean value 1)	1.5 Hz spike train through AMPA synapses	
	2 Hz (Boolean value 0)	8 Hz (Boolean value 1)	8 Hz (Boolean value 1)	1 Hz (Boolean value 0)	7.8 Hz spike train through AMPA synapses	
	2 Hz (Boolean value 0)	9 Hz (Boolean value 1)	6 Hz (Boolean value 1)	9 Hz (Boolean value 1)	3.5 Hz spike train through AMPA synapses	
	7 Hz (Boolean value 1)	1 Hz (Boolean value 0)	2 Hz (Boolean value 0)	2 Hz (Boolean value 0)	1.6 Hz spike train through AMPA synapses	**AND (s1s0:10)**
	7 Hz (Boolean value 1)	1 Hz (Boolean value 0)	2 Hz (Boolean value 0)	7 Hz (Boolean value 1)	2.6 Hz spike train through AMPA synapses	
	7 Hz (Boolean value 1)	1 Hz (Boolean value 0)	8 Hz (Boolean value 1)	1 Hz (Boolean value 0)	2.9 Hz spike train through AMPA synapses	
	7 Hz (Boolean value 1)	1 Hz (Boolean value 0)	6 Hz (Boolean value 1)	9 Hz (Boolean value 1)	8.7 Hz spike train through AMPA synapses	
	7 Hz (Boolean value 1)	8 Hz (Boolean value 1)	2 Hz (Boolean value 0)	2 Hz (Boolean value 0)	3.3 Hz spike train through AMPA synapses	**OR (s1s0:11)**
	7 Hz (Boolean value 1)	8 Hz (Boolean value 1)	2 Hz (Boolean value 0)	7 Hz (Boolean value 1)	10 Hz spike train through AMPA synapses	
	7 Hz (Boolean value 1)	8 Hz (Boolean value 1)	8 Hz (Boolean value 1)	1 Hz (Boolean value 0)	9.2 Hz spike train through AMPA synapses	
	7 Hz (Boolean value 1)	8 Hz (Boolean value 1)	6 Hz (Boolean value 1)	9 Hz (Boolean value 1)	12.7 Hz spike train through AMPA synapses	

logical part. Also, Table 5 reports the spiking reaction of the ALU in response to the different input spike trains, which verifies the functionality of the proposed structure.

ALU is an essential element of the central processing unit (CPU) and the design of basic computer based on the SFGs will be considered in the future works.

In response to the essential question, an attempt was made to clarify the distinct properties of the proposed spiking frequency gates. Coding in the SFGs and spiking circuits (FA, MUX, ALU) are based on the fixed frequency of the input and output spike trains. One fundamental question that can be raised is that if the frequency of the spike train of input and output is not constant, what is the response of the spiking circuits and SFGs? As an example, in response to this question, the spiking circuit ALU was introduced as a pattern recognition platform. The pattern of capitals “X” and “O” were considered according to Fig. 10.

Spike trains form the input of the SFGs and the spiking circuits. So, in order to apply the image to the input of ALU, the image should be transformed into a spike train. According to Fig. 11, each black pixel converts to the one-second spike train

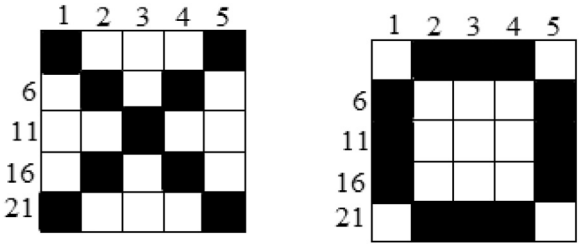


Fig. 10. Capitals "X" and "O" with 25 pixels per image.

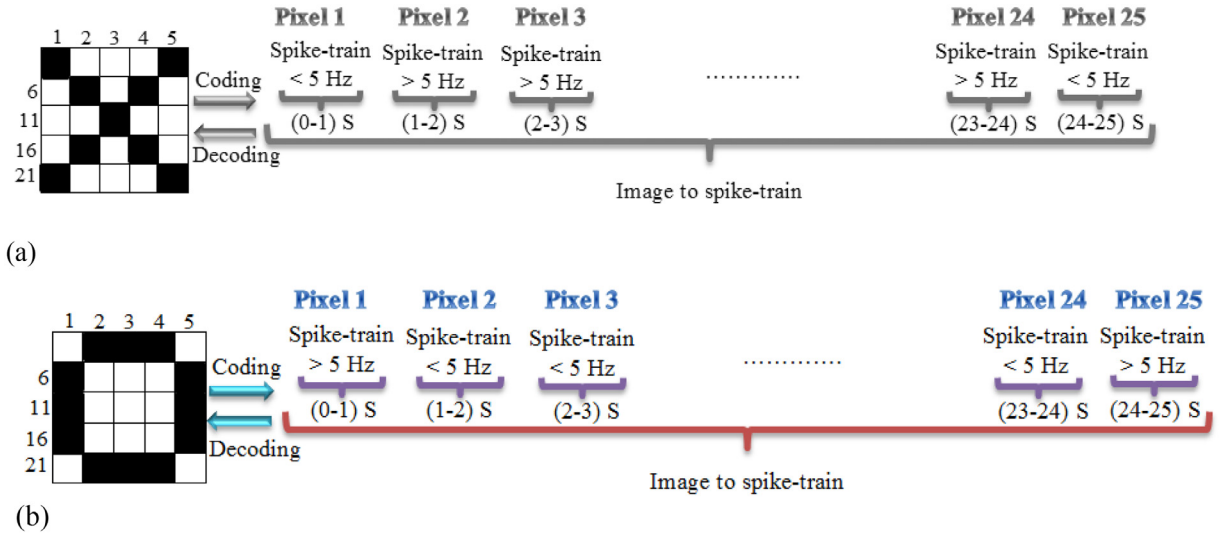


Fig. 11. Image to spike train converter for the image of capital "X" and capital "O".

with a frequency below 5 Hz and each white pixel also transforms to the spike train with a frequency higher than 5 Hz. Finally, the sequence of these spike trains from pixel 1 to pixel 25 was considered as the corresponding spike train of the input image.

In this case, the image converts to the spike train, which, unlike the previous modes, does not have a constant frequency, and includes a set of 25 different frequencies. Now, if the spike train corresponding to "X" and "O" patterns are applied to the ALU, by decoding the spike response of the output neuron, the patterns of Fig. 12 are generated.

According to Fig. 12, it can be concluded that:

The ADD operand reveals the identical pixels in the input patterns with black pixels in the generated output pattern.
The AND operand reveals the identical white pixels in the input patterns with white pixels in the generated output pattern.
The OR operand reveals the identical black pixels in the input patterns with black pixels in the generated output pattern.

Therefore, the spiking circuit of ALU can be used as a pattern recognition network, which produces the similarity and difference of input patterns in the generated output pattern. This spiking circuit can also be used to change the selective pixels of the input image as well as to reproduce the input pattern in the generated output image similar to the Auto-Encoder network [36]. In general, ALU can be a spiking circuit for calculating binary numbers if each spike train of the input has a constant frequency and can be a pattern recognition network if the spike trains of the inputs have a variable frequency. Multi-tasking has been proven in the elements of the nervous system because parts of the nervous system jointly participate in different neural activities [5,24,38]. This result confirms the effective imitation of the spiking circuit from the structure of the brain.

Humans have a unique ability in cognitive tasks such as pattern recognition. However, the mechanisms of information transmission of neuronal processes are still not well discovered. Achieving a deeper and more practical understanding of the brain function requires efforts in two contexts. First deep understanding of neural processes [33] and second the achievement of microelectronic technology such as memristor with the ability to reproduce structural (high density of synaptic connections) and functional (dynamical learning approach based on the spike timing) capabilities of the nervous system on hardware platforms such as neuromorphic systems [32].

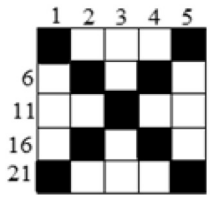
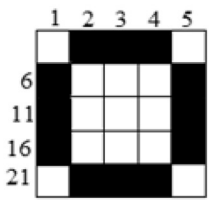
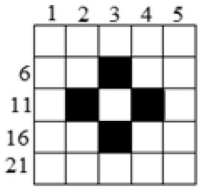
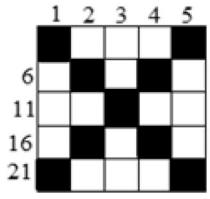
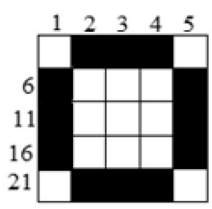
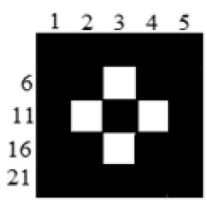
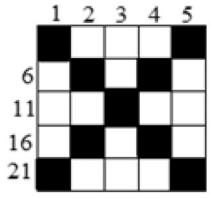
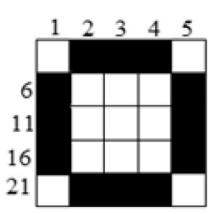
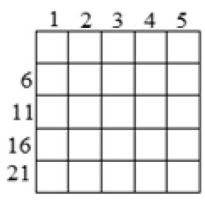
Operation mode	Input1	Input2	Output
ADD			
AND			
OR			

Fig. 12. The response of the spiking ALU to the input patterns "X" and "O".

However, the design of bio-inspired spiking pattern recognition networks with more realistic spike characteristics and the ability to be implemented in electronic platforms still remain a challenge [8]. Spiking frequency gates with the biological background, ability to be implemented in neuromorphic systems, and computational power of pattern recognition can play an important role in reproducing the unique ability of the nervous system in cognitive tasks and learning on the new generation of spiking computers. Although in this paper, SFGs have been introduced as an analysis and recognition tool for patterns, the investigation of learning of SFGs have been postponed to future works. However, the learning approach of the proposed spiking circuits for machine learning applications can be categorized as spike-based [3–4] and rate based learning. There is considerable debate on the importance of firing rate or timing of spikes. Scientists agree on the importance of both rate and spike timing in brain coding. The basis of learning based on the spike is a change in the weight of network synapses using different views of the spike-timing-dependent plasticity (STDP) [4,45]. This is while, the training rule in rate-based learning is defined based on back-propagation [41] or other rate-based learning algorithms [31].

5. Conclusion

In recent years, computer science has been moving toward the design of powerful computing devices and smart machines inspired by the processing and transmission of information in the nervous system. In general, the bio-computing device based on the dynamic neural structure is a new branch of computational tools that have attracted special attention in recent years [49,34]. In this research, we established and proposed spiking frequency gates based on DSNN to imitate logic gates AND, OR, NOT, NOR, XOR and NAND and then an attempt was made to develop spiking frequency circuits full adder, Mux and ALU. The system coding is summarized as follows: the binary number 0 was encoded by spiking frequency below 5 Hz, and the binary number 1 was represented by spiking frequency over 5 Hz. Reported results illustrate a novel way of developing the neural counterpart of logical circuits with the dynamical model of excitatory and inhibitory neurons and synapses. Using the cascade connections of the proposed spiking gates, finite computing devices can be constructed with spiking elements, which can imitate the performance of its Boolean counterpart. This work can create some potential directions in the professional design of neural circuits with engineering applications. Parallel hardware implementation of neural-like circuits can be utilized to compensate low-speed performance of spiking gates relative to the Boolean gates. The strength of spiking gates relative to their Boolean counterpart is that the coding of spiking circuits can be as powerful as the complex information coding of the nervous system. In fact, the functional complexities of the nervous system originate from strong coding in the dynamic space at a low spike rate, which we attempt to build a machine based on this structure.

As it is observed, so far spiking gates have not been provided with such computational power. The proposed spiking circuits based on the dynamic quiddity of the basic elements of the hippocampus can be effective in developing the new generation of computers with a similar ability of the nervous system in learning and cognitive processes.

Future works may contain simplification of topological structures of circuits and optimization of the number of required neurons in system configuration. This article initiates a path that requires further attention of researchers in this field. Also, the performance of SFGs with other coding strategies can be considered in future works. Computational models of astrocyte [26] can also be involved in the design of SFGs, and make the signaling of the spiking gates closer to the dynamics of the nervous system [23]. As an important point, it should be noted that the introduction of learning strategies such as the Deep learning approach [46,42] and machine learning algorithms [6] in the learning mechanism of spiking gates can attract a lot of attention.

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