Name: Thiago Gesteira **Student ID: 200431173**

I certify that I individually did the design, simulation and synthesis that lead to these solutions, did not copy the answers to this homework and did not let anyone copy my answers (sign):

Clock Period Achieved (ps): 4

Verilog design File (not test fixture – put that on the next page):

```
/*module**********************************
*
* NAME:  counter
*
* DESCRIPTION:
*  downcounter with zero flag and synchronous clear
*
* NOTES:
*
* REVISION HISTORY
*    Date     Programmer          Description
*    9/17/24  Thiago Gesteira    ece564-8-bit-down-counter
*
*/

/*=======Declarations================================*/

module counter (clock, in, latch, dec, divByTwo, zero);


/*-----------Inputs-------------------------------*/

input       clock;  /* clock */
input [7:0] in;  /* input initial count */
input       latch;  /* `latch input' */
input       dec;   /* decrement */
input       divByTwo;  /* divide by two */

/*-----------Outputs------------------------------*/

output      zero;  /* zero flag */

/*----------------Nets and Registers----------------*/
/*---(See input and output for unexplained variables)---*/

reg [7:0] value;       /* current count value */
wire      zero;
```

```
// Count Flip-flops with input multiplexor

always@(posedge clock)
  begin  // begin-end not actually need here as there is only one statement
    casex ({latch, dec, zero, divByTwo})
      4'b1???: value <= in;
      4'b010?: value <= value - 1'b1;
      4'b0001: value <= value >> 1;
      default: value <= value;
    endcase
  end

// combinational logic for zero flag
assign zero = ~|value;

endmodule /* counter */
```

Verilog test fixture:

```
module test_fixture;
        reg             clock100 = 0 ;
        reg             latch = 0;
        reg             dec = 0;
        reg             [7:0] in = 8'b01010101;
        reg             divByTwo = 0;
        wire    zero;

        initial  //following block executed only once
          begin
                //$dumpfile("count.vcd"); // waveforms in this file..
                //$dumpvars; // saves all waveforms
                #16 latch = 1;          // wait 16 ns
                #10 latch = 0;          // wait 10 ns
                #10 dec = 1;
                #9 dec = 0;
                #11 divByTwo = 1;
                #10 divByTwo = 0;
                #100 $finish;           //finished with simulation
        end
        always #5 clock100 = ~clock100;     // 10ns clock

        // instantiate modules -- call this counter u1
         counter u1(  .clock(clock100), .in(in), .latch(latch), .dec(dec),
                                        .divByTwo(divByTwo), .zero(zero));
endmodule  /*test_fixture*/
```

Min and Max Timing Reports:

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : counter
Version: T-2022.03-SP4
Date   : Wed Sep 18 18:57:58 2024
****************************************

Operating Conditions: typical   Library:
NangateOpenCellLibrary_PDKv1_2_v2008_10_typical_nldm
Wire Load Model Mode: top

  Startpoint: latch (input port clocked by clock)
  Endpoint: value_reg_7_
            (rising edge-triggered flip-flop clocked by clock)
  Path Group: clock
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clock (rise edge)                0.0000     0.0000
  clock network delay (ideal)            0.0000     0.0000
  input external delay                   0.6580     0.6580 f
  latch (in)                             0.0976     0.7556 f
  U179/ZN (NOR3_X2)                      0.2119     0.9675 r
  U167/ZN (INV_X4)                       0.0339     1.0014 f
  U154/ZN (NAND3_X2)                     0.0631     1.0645 r
  U176/ZN (OAI21_X2)                     0.0546     1.1191 f
  U180/ZN (AOI21_X2)                     0.0950     1.2141 r
  U181/ZN (OAI21_X2)                     0.0493     1.2634 f
  U129/ZN (AOI22_X2)                     0.0773     1.3407 r
  U161/ZN (INV_X4)                       0.0099     1.3505 f
  value_reg_7_/D (DFF_X2)                0.0000     1.3505 f
  data arrival time                                 1.3505

  clock clock (rise edge)                4.0000     4.0000
  clock network delay (ideal)            0.0000     4.0000
  clock uncertainty                     -0.0500     3.9500
  value_reg_7_/CK (DFF_X2)               0.0000     3.9500 r
  library setup time                    -0.0654     3.8846
  data required time                                3.8846
  -----------------------------------------------------------
  data required time                                3.8846
```

```
  data arrival time                                  -1.3505
  ---------------------------------------------------------
  slack (MET)                                         2.5341


1

****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : counter
Version: T-2022.03-SP4
Date   : Wed Sep 18 18:57:59 2024
****************************************

Operating Conditions: fast   Library:
NangateOpenCellLibrary_PDKv1_2_v2008_10_fast_nldm
Wire Load Model Mode: top

  Startpoint: value_reg_7_
              (rising edge-triggered flip-flop clocked by clock)
  Endpoint: value_reg_7_
            (rising edge-triggered flip-flop clocked by clock)
  Path Group: clock
  Path Type: min

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clock (rise edge)                0.0000     0.0000
  clock network delay (ideal)            0.0000     0.0000
  value_reg_7_/CK (DFF_X2)               0.0000     0.0000 r
  value_reg_7_/Q (DFF_X2)                0.0599     0.0599 r
  U129/ZN (AOI22_X2)                     0.0154     0.0753 f
  U161/ZN (INV_X4)                       0.0088     0.0841 r
  value_reg_7_/D (DFF_X2)                0.0000     0.0841 r
  data arrival time                                 0.0841

  clock clock (rise edge)                0.0000     0.0000
  clock network delay (ideal)            0.0000     0.0000
  clock uncertainty                      0.0500     0.0500
  value_reg_7_/CK (DFF_X2)               0.0000     0.0500 r
  library hold time                     -0.0152     0.0348
  data required time                                0.0348
  -----------------------------------------------------------
  data required time                                0.0348
```

```
  data arrival time                                  -0.0841
  ---------------------------------------------------------
  slack (MET)                                         0.0493


1

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : counter
Version: T-2022.03-SP4
Date   : Wed Sep 18 18:58:00 2024
****************************************

Operating Conditions: slow   Library:
NangateOpenCellLibrary_PDKv1_2_v2008_10_slow_nldm
Wire Load Model Mode: top

  Startpoint: value_reg_0_
              (rising edge-triggered flip-flop clocked by clock)
  Endpoint: value_reg_7_
            (rising edge-triggered flip-flop clocked by clock)
  Path Group: clock
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clock (rise edge)                0.0000     0.0000
  clock network delay (ideal)            0.0000     0.0000
  value_reg_0_/CK (DFF_X2)               0.0000     0.0000 r
  value_reg_0_/Q (DFF_X2)                0.5725     0.5725 f
  U160/ZN (NOR3_X2)                      0.4109     0.9834 r
  U159/ZN (AND3_X2)                      0.3489     1.3323 r
  U158/ZN (NAND3_X2)                     0.1155     1.4477 f
  U157/ZN (NOR2_X2)                      0.6521     2.0998 r
  U179/ZN (NOR3_X2)                      0.3105     2.4103 f
  U167/ZN (INV_X4)                       0.1964     2.6067 r
  U176/ZN (OAI21_X2)                     0.1158     2.7224 f
  U180/ZN (AOI21_X2)                     0.3499     3.0723 r
  U181/ZN (OAI21_X2)                     0.1605     3.2328 f
  U129/ZN (AOI22_X2)                     0.2918     3.5246 r
  U161/ZN (INV_X4)                       0.0419     3.5665 f
  value_reg_7_/D (DFF_X2)                0.0000     3.5665 f
  data arrival time                                 3.5665
```

```
clock clock (rise edge)                  4.0000     4.0000
clock network delay (ideal)              0.0000     4.0000
clock uncertainty                       -0.0500     3.9500
value_reg_7_/CK (DFF_X2)                 0.0000     3.9500 r
library setup time                      -0.3057     3.6443
data required time                                  3.6443
-----------------------------------------------------------
data required time                                  3.6443
data arrival time                                  -3.5665
-----------------------------------------------------------
slack (MET)                                         0.0778
```