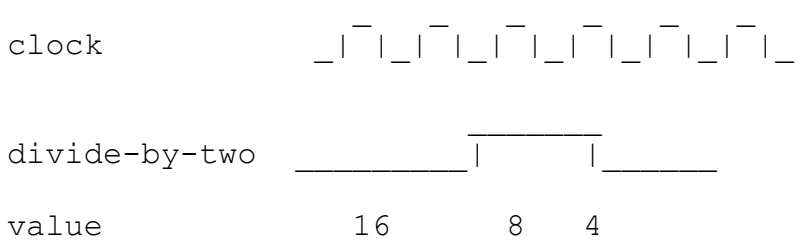
ECE 564 / ECE 464
Homework 3

Question 1
The purpose of this question is to start you using the simulation and synthesis tools. Do the tutorial listed in the resources section.

Then do the following:

(a) Redesign the module in the tutorial as an 8 bit down-counter. In addition, add the input `divide-by-two`. Whenever `divide-by-two` is high and `latch` is low and `dec` is low (both `dec` and `divide-by-two` will never be high at the same time), divide the current contents of the counter by 2 (by doing a right shift). e.g.



(b) Synthesize the fastest possible design, by taking the strategy of reducing the clock period and doing incremental compiles. e.g.

```
      /* see if the design works with a faster clock */
      create_clock -period 9 -waveform {0 4.5} clock
      compile -incremental
      report_timing
      /* if this design works, save it in case the next one did
not */
      write -f ddc -output tmp9.ddc

       /* see if the design works with a still faster clock */
      Create_clock -period 8 -waveform {0 4} clock
      compile -incremental
      report_timing
      /* if this design works, save it in case the next one did
not */

     write -f ddc -output tmp8.ddc
```

```
/* etc. */
```

You will need to iterate on this loop after your first compile but before the `Fix hold times` comment. It is best if you break the current script into 2 files; one up to the first report_timing and one after that. Enter the above commands by hand into design_analyzer or dc_shell.
When you find a clock speed that does not work, then read back in the .db file for the fastest working clock speed `(read_file -format ddc tmp?.db or read_ddc tmp?.db)` and perform the rest
of the original script.

In your solutions, please turn in the following:

- A copy of your Verilog listing (first page), as well as your test fixture (second page).
- A cut-and-paste copy of your final timing reports for both set-up and hold. Take these from the appropriate synopsys output file.

[20 points]

Use the template on the next page, as the first page of your solutions. Make sure this template is one page. Attach other documentation as needed. Please turn it in as one PDF file.

Note, This is just an exercise to get you more familiar with Synopsys and with how to squeeze the timing down in an actual design. You are not expected to do it in later exercises. It is up to you if you explore this in the project. However, in general the fastest possible design does not maximize performance/area. To explore that goal, you need to look at both timing and area (report_area).

Name: **Student ID:**

I certify that I individually did the design, simulation and synthesis that lead to these solutions, did not copy the answers to this homework and did not let anyone copy my answers (sign):

Clock Period Achieved (ps):

Verilog design File (not test fixture – put that on the next page):

Min and Max Timing Reports: