INTEGRATED CIRCUIT

An integrated circuit (IC), sometimes called chip or microchip, is a semiconductor wafer on which thousands or millions of tiny resistors, capacitors and transistors are fabricated.

In today's technology, the most popular transistor is the metaloxide-semiconductor (MOS) structure. The controlling part is called the *gate*. Smaller gate widths drive the industry by producing smaller and faster transistors and more dense circuits. Currently, the gate width is less than 20nm.

Due to reduction in gate width, the circuit density or the *integration level,* which is the number of components in a circuit, has increased. Integration levels range from small scale integration (SSI) to ultra large scale integration (ULSI). ULSI chips are sometimes referred to as very very large scale integration (VVLSI).

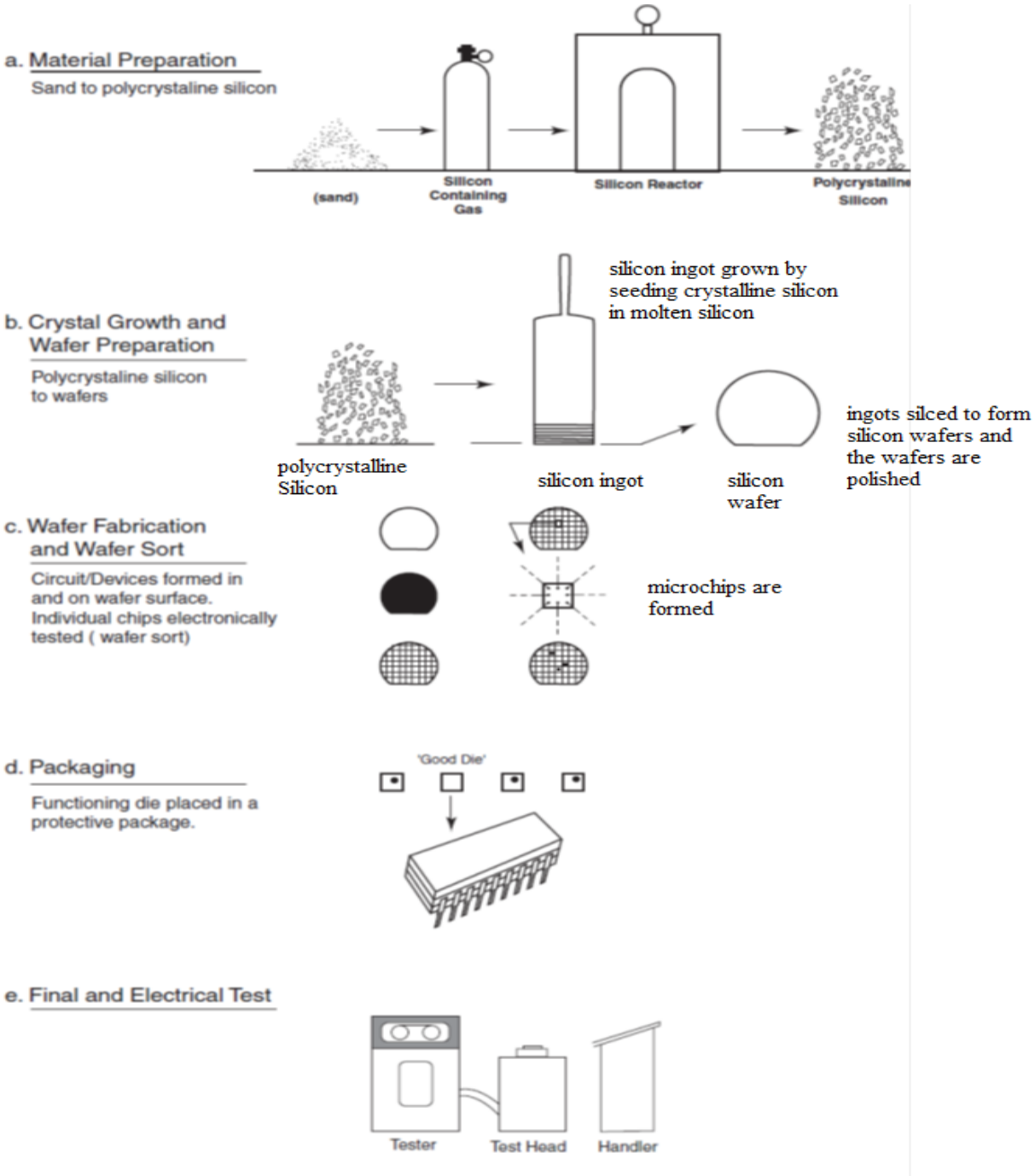
Level	Abbreviation	# Components per Chip
Small Scale Integration	SSI	2 - 50
Medium Scale Integration	MSI	50 - 5000
Large Scale Integration	LSI	5000 - 100,000
Very Large Scale Integration	VLSI	Over 100,000 - 1,000,000
Ultra Large Scale Integration	ULSI	> 1,000,000

The advancement of chip density from the SSI level to ULSI chips has driven larger chip sizes. Discrete and SSI chips average about 100 mils (0.1 in) on a side. ULSI chips are in the 500 to 1000 mil (0.5 to 1.0 in) per side, or larger, range. ICs are manufactured on thin disks of silicon called *wafers*.

STAGES OF SEMICONDUCTOR PROCESSING (MICROCHIP FABRICATION):

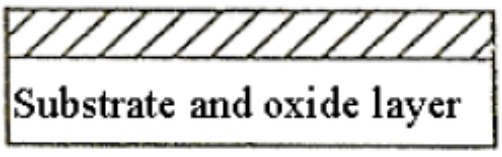
Semiconductor manufacturing involves the following stages:

1. Material preparation – sand is converted in to polycrystalline silicon
2. Crystal growth and wafer preparation – polycrystalline silicon is then melted and crystal growth is allowed to form silicon ingots. These ingots are then sliced into silicon wafers.
3. Wafer fabrication and sort – circuits or devices are formed on the wafer i.e., thousands of microchips are formed in the silicon wafer.
4. Packaging
5. Final and electrical test



MICROCHIP FABRICATION

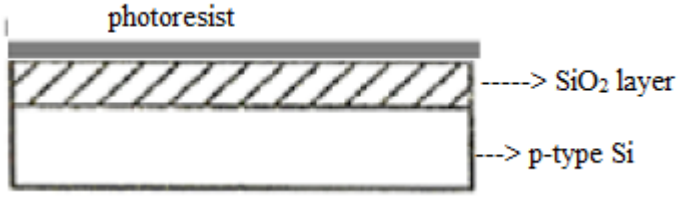
1. **Layering Operation.** The substrate is p-doped silicon. The building starts with an oxidation of the wafer surface to form a thin protective layer and to serve as a doping barrier.



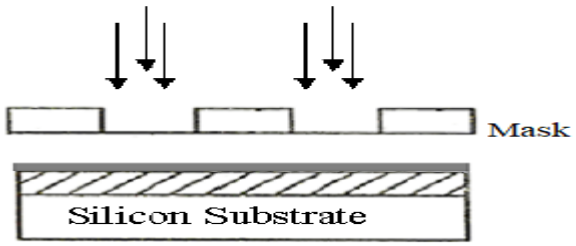
2. **Patterning Operation.** Patterning is the series of steps that results in the removal of selected portions of the added surface layers**.** The patterning process leaves a hole in the SiO_2 that defines the location of the source, gate, and drain areas of the transistor. This operation involves the following steps and is called photolithography.

Photolithography

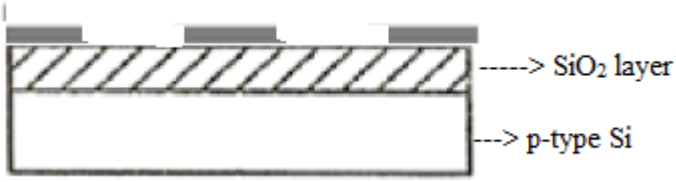
(a) A layer of positive photoresist is applied to the wafer by spin coating. The resist is soft baked to evaporate the solvent and set the edges.



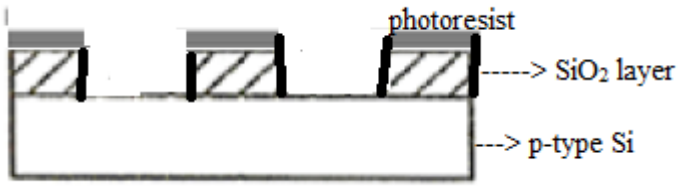
(b) A photo mask is aligned upon the wafer and exposed with light of the appropriate wavelength.



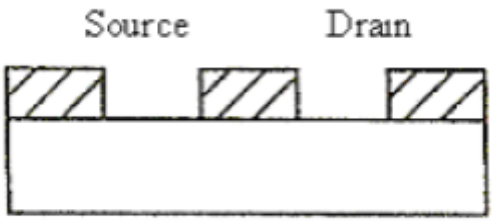
(c) The nature of the resist is such that exposed areas become more soluble in the presence of an alkaline developing solution. The wafer is developed so as to remove soluble resists. A second bake sets the pattern into the resist.



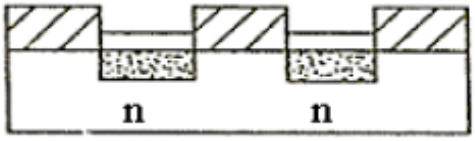
(d) An etching agent is used to remove the SiO2 in the required areas (where the drain and source of the transistor are to be formed.



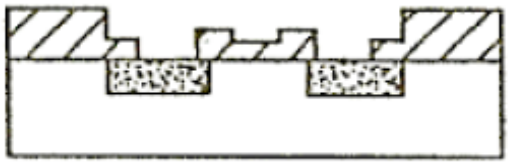
(e) Then the remaining photoresist is removed.



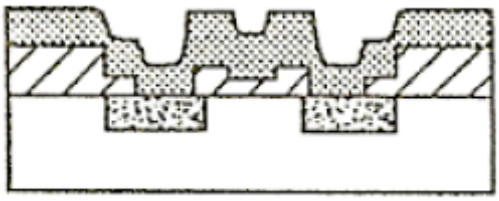
3. This is followed by ion implantation of pentavalent phosphorous atoms so as to create the n doped region and second layer of oxide is grown so as to insulate the drain / source regions.



4. Patterning and etching (steps 2, 3, 4 and 5 repeated) removes oxide in gate region: The gate material is then grown. Contact holes for metal contacts are patterned into source, drain and gate regions.



5. Conducting metal is deposited on wafer. Metal is patterned and alloyed to wafer in order to make interconnections on the chip



6. These sequence of steps are repeated to grow another layer of circuits.

CHALLENGES ENCOUNTERED IN ELECTRONICS MANUFACTURE:

(A) CHALLENGES IN FABRICATION OF ICs:

1. **Defects during fabrication:**

As feature sizes have decreased, the need for reduced defect density and defect size on the chips during manufacturing process has become critical.

Defects can arise due to particulate matter. For e.g., a 1-micron piece of dirt on a one-micron sized transistor, can become a killer defect, that can render the component inoperable. Contamination control by clean room technologies is one of the major contributors in driving the cost of building an IC manufacturing facility into the multibillion dollar range.

Patterning is another source of defect formation and is the most critical of the four basic operations in microchip fabrication. This operation sets the critical dimensions of the devices. Errors in the patterning process can cause distorted or misplaced patterns that result in changes in the electrical functioning of the device/circuit. The properties and selection of photoresists pay a major role in controlling these defects.

2. **Contamination:**

Small amount of certain electrically active contaminants in the wafer can alter device electrical characteristics. The contaminants causing these types of problems are known as *mobile ionic contaminants* (MICs). They are metal ions like Na+, K+, Ca2+, Mg2+, Fe2+ etc. Unfortunately, these metals ions are present in most chemicals and water.

A modern wafer fabrication facility may use up to several million gallons of water per day, representing a substantial investment in water processing, delivery to the process areas, and treatment and discharge of waste water. Since semiconductor devices are vulnerable to contamination, ultrapure water or electronic grade water should be used i.e., water that meets requirements as specified in The American Standards for Testing Materials(ASTM).

The acids, bases, and solvents used to etch and clean wafers and equipment have to be of the highest purity for use in a fabrication area. Electronic grade and semiconductor grade chemicals are used. Most firms purchase clean process chemicals in bulk quantities. They are decanted into smaller vessels and are distributed to the process stations from a central location by pipes or distributed directly to the process station from a mini-unit.

Special care must be maintained to ensure that piping and transfer vessels are cleaned regularly to prevent contamination.

A semiconductor wafer is also processed with many gases. For eg., gases are such as arsine and carbon tetrafluoride. Like the wet chemicals, they have to be delivered clean to the process stations and tools. Gas quality is measured in four categories:

1. Percentage of purity
2. Water vapor content
3. Particulates
4. Metallic ions

Extremely high purity is required for all process gases.

3. **Increased levels of interconnections:**

Miniaturization results in increasing the number of electronic elements in a volume unit i.e., more number of components have to be connected while at the same time they are more closely spaced. With decreasing device dimensions the number of interconnection levels have to be increased. The current 22nm technology chips have 11 levels of interconnects.

4. **Material challenges:**

Decreased device dimensions also lead to material challenges. The dielectric required is made by growing SiO_2. But there may be leakage of current in the SiO2 layer due to small dimensions. Therefore Hafnium oxide based materials are used which lead to complexities in fabrication.

(B) CHALLENGES IN ELECTRONIC PACKAGING

1. **Thermal Management:**

All electronic devices require a source of power which is partially converted into heat. This heat has to be transferred by the surrounding structures to the ambient air outside the system and/or to a heat sink. Generally, a rise in temperature from 75 °C to 125 °C can result in a five-fold increase in failure rate of a device. Thus, the heat dissipation problem is becoming a crucial barrier in miniaturization processes, and successful thermal packaging depends on a combination of proper materials and heat transfer mechanisms to stabilize the component temperature at an acceptable level.

2. **Need to replace hazardous substances:**

E-Waste is of major health and environmental concern due to the toxicity of some of the materials present in the waste stream. For eg., lead present in solder. Solder is used for joining various components in a PCB.

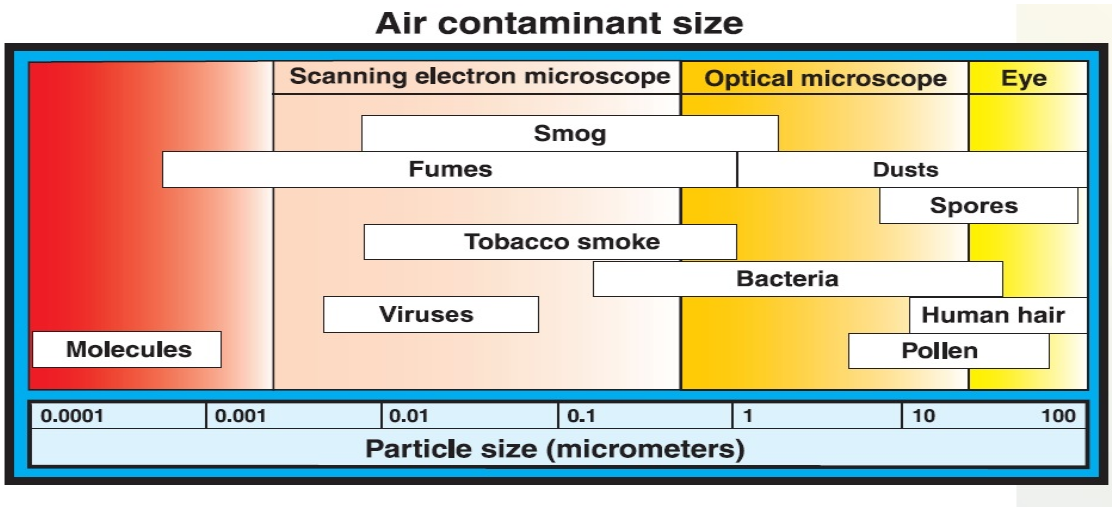
Lead in Electrical and Electronic Equipment (EEE) is of a major concern to the public due its ability to leach from landfills and contaminate the human food chain causing serious health hazards. To address this issue, European Union and countries such as China, Japan and Korea have passed legislation to remove lead from EEE which is commonly known as ‘Restriction of Hazardous Substances (RoHS)' directive.

Lead-free soldering in EEE is one of the major drivers of the legislation forcing researchers and manufacturers to find suitable lead-free substitutes for the traditional leaded solders. Despite significant investments being made on research and development of lead-free solders, to date, no perfect substitutes for lead based solders have been found.. Although, few lead-free alloys have emerged as strong candidates there are various issues such as durability and reliability surrounding these candidates and the research is on-going.

CLEAN ROOMS FOR MICROCHIP FABRICATION:

The ambient air outside in a typical urban environment might contain as many as 35,000,000 particles per cubic meter which are 0.5 um and larger in diameter.

The following figure gives an idea about the sizes of various air contaminants in the atomosphere.



CLEAN ROOMS:

Cleanrooms are specially constructed, environmentally controlled enclosed spaces where the concentration of airborne particles (contaminants) is kept within specified limits. In industry, cleanrooms are used in the manufacturing of electronic hardware such as integrated circuits (ICs) and hard drives.

According to ISO 14644-1, a **cleanroom** is “a room in which the concentration of airborne particles is controlled, and which is constructed and used in a manner to minimize the introduction, generation, and retention of particles inside the room and in which other relevant parameters, e.g. temperature, humidity, and pressure, are controlled as necessary."

Cleanrooms are classified in terms of the number and sizes of particles suspended in its atmosphere. A particle is defined as a solid or liquid object between 0.001 and 1000 microns in size. Table 1 shows the various cleanroom classes and their corresponding statistically allowable number of particles per cubic foot of air, as defined by Federal Standards 209E. To illustrate, in a Class 100 cleanroom, a cubic foot of air is only allowed to have 100 particles whose size is 0.5 micron.

Table 1. Cleanroom Classes

Class Name	0.1 micron	0.2 micron	0.3 micron	0.5 micron	5 micron
1	35	7.5	3	1	N/A
10	350	75	30	10	N/A
100	N/A	750	300	100	N/A
1000	N/A	N/A	N/A	1000	7
10000	N/A	N/A	N/A	10000	70
100000	N/A	N/A	N/A	100000	700

In semiconductor manufacturing, wafer fab processes usually require a sub-Class 1 to Class 10 cleanroom, while assembly processes prior to encapsulation of the die require a Class 10K cleanroom. A class 100K cleanroom is all that post-encapsulation assembly and test processes typically require.

Air Filters used in the maintaining clean rooms

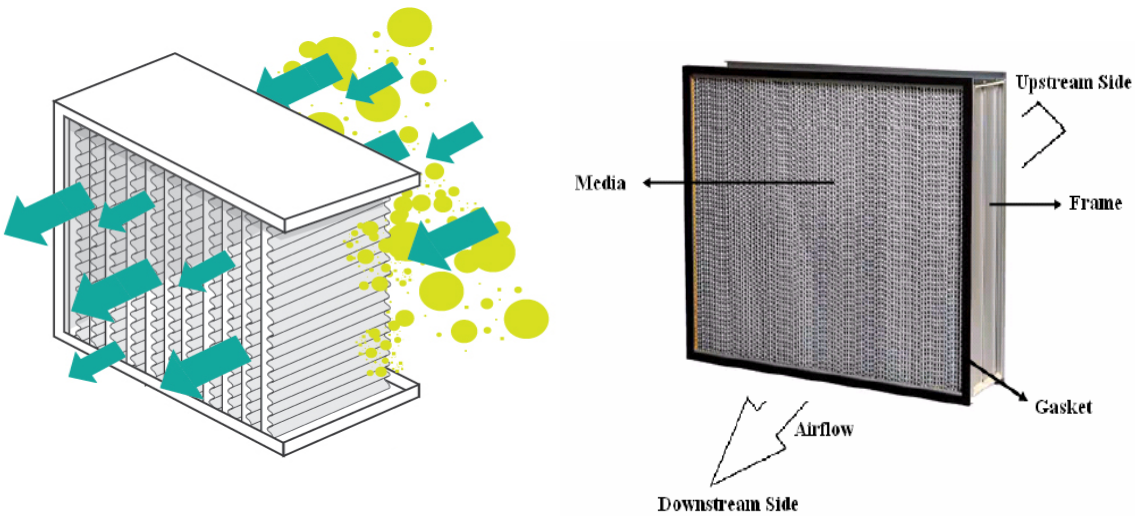
All air entering a cleanroom must be treated by one or more filters. High-efficiency particulate air (HEPA) and ultra-low penetration air (ULPA) filters are the most common filters used in cleanroom applications. They trap particulate matter when air is passed through them. In a microchip fabrication facility almost 5 million cubic meters of air are exchanged per hour to maintain clean rooms.

For a filter to be classified as a HEPA (High Efficiency Particulate Air) filter, it should remove 99.97% of particulates of size greater than or equal to 0.3 μm.

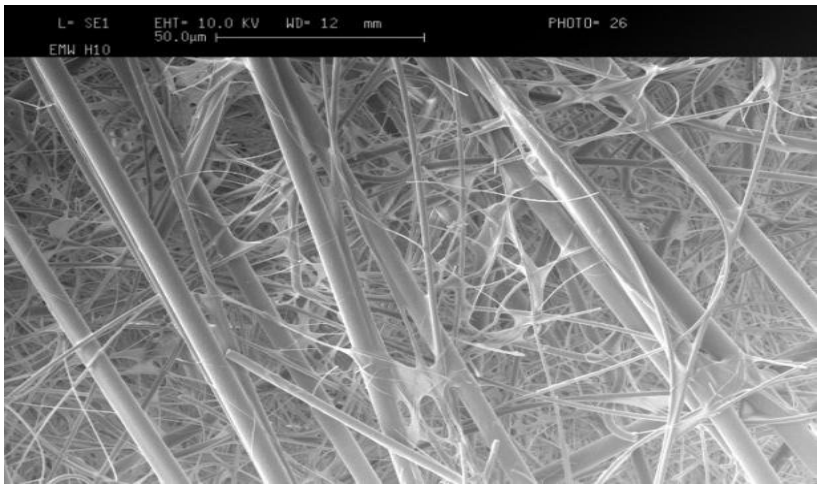
A ULPA (Ultra Low Particulate Air (filter) is a step further than HEPA. For a filter to be classified as ULPA it should remove 99.999% of particulates which are greater than or equal to 0.1 μm.

Both HEPA and ULPA filters are designed to trap very small particulate contaminants from an air stream by forcing air through a fine mesh.

Components of an air filter



- Filter media - The filters are made out of very fine borosilicate glass fibres with a diameter of less than 1 micron. The fine glass fibres are tangled together and compressed to form a filter mat. The open spaces in the mat are very small, generally less than 0.5 micron. HEPA filters will collect particles down to 0.3 microns in diameter. The filter may only be 0.10 in (2.5 mm) wide, it would consist of 2,500 layers of glass fibres.



Sem image of glass fibres in air filters

- Frame - this is where the filter media is inserted. It can be made from a variety of materials including aluminum, stainless steel, plastic or wood.
- Sealants - the adhesive material that creates a leak-proof seal between the filter media and the frame.
- Faceguard - this is a screen attached to the filter to protect the filter media during handling and installation.
- Gasket - this is a rubber or sponge like material used to prevent air leaks between the filter and its housing by compressing the two together.

Activated carbon in air filtration:

Air filters do not remove gases or odours: For this reason, most air purifiers are equipped with a pre- or post-filter composed of activated carbon.

Activated carbon is produced by heating a carbon source (coconut shells, old tires, bones, etc.) at very high temperatures in the absence of oxygen, a process also known as pyrolysis or destructive distillation. Pyrolysis separates the pure carbon from the other materials contained in the raw material. The pure carbon is then exposed to steam at 1,500°F(800°C). The high temperature steam activates the carbon. The activation process provides the carbon with an enormous surface area per weight—about 1,000 m^2/g.. Activated carbon is very effective at adsorbing odour producing compounds.