American International University – Bangladesh (AIUB)
Faculty of Engineering
Department of Electrical and Electronic Engineering

Final Assignment			
Course Name:	Microprocessor and Embedded Systems	**Course Code:**	EEE
Semester:	Spring 2023-2024	**Section:**	**J**
Faculty Name:	**Engr. Md Shaoran Sayem**		

Assignment No:	1F **(individual submission consisting of 30 marks)**

Submission Date:	**10/05/2024**	**Due Date:**	**10/05/2024**

Student Information:

Student Name:	**MD. SHOHANUR RAHMAN SHOHAN**											**Section:**	**J**
Student ID #:	**2**	**2**	**-**	**4**	**6**	**0**	**1**	**3**	**-**	**1**	**Assigned Date:** **25.04.2024**	**Department:**	**CSE**
	p	**q**	**-**	**a**	**b**	**c**	**d**	**e**	**-**	**r**			

Special Instruction: Questions may be copied from here through copy-paste. Online submission via TEAMS is needed. However, hardcopy must also be submitted.

Assessment Rubrics:

COs-POIs	Excellent [19-20]	Proficient [15-18]	Good [11-14]	Acceptable [6-10]	Unacceptable [1-5]	No Response [0]	Secured Marks
CO3 P.a.4.C.3	All the problems are solved correctly. The results are generated by combining all possible input patterns with appropriate outcomes. All necessary drawings and computations are shown correctly.	All the problems are solved correctly. The results are generated by combining all possible input patterns with appropriate outcomes. A few necessary drawings and computations are missing but no wrong drawing.	All the problems are solved correctly. The results are generated by combining all possible input patterns with appropriate outcomes. A few necessary drawings and computations are missing or wrong.	All the problems are not solved correctly. The results are generated by combining several wrong or less no of input patterns with in/appropriate outcomes. Some necessary drawings and computations are missing or wrong.	All the problems are not solved correctly. The results are generated by combining mostly wrong input patterns with inappropriate outcomes. Almost all the necessary drawings and computations are missing or wrong.	No responses at all or copied from others	
Comments					**Total Marks (20)**		

1. Find the baud rate for the three operating modes when the oscillator frequency, f_{OSC} = ac MHz (put side-by-side), and register data is, UBRRn = 010110101110. Calculate the baud error and comment on whether there will be any communication errors or not. Standard Baud rates are 300, 600, 1200, 2400, 4800, 9600, 14400,19200, 38400, 57600, 115200, 230400, ... bps.

2. Compute the duty cycle and sketch the waveform obtained at port D of the Arduino. Identify the modes of operation and compute the operating frequency of that mode based on the following program segment. Identify the Timer of the Arduino Microcontroller. The system clock frequency is rq MHz. Draw the relevant circuit diagram using Proteus and show its timing diagram.

```
DDRD |= (1<<PD5);
pinMode(5, OUTPUT);
OCR0A = (200+ a + b + c); // Load a value in the OCR0A register
OCR0B= (100 + d + e); // Load a value in the OCR0B register
// Configure TCCR0A and TCCR0B registers for the mode and pre-scaler
TCCR0A |= (1 << COM0B1) | (1 << COM0A0) | (1<<WGM01) | (1<<WGM00);
TCCR0B |= (1<<WGM02) | (1<<CS01) | (1<<CS00);
```

3. Compute the duty cycle and sketch the waveform obtained at port D of the Arduino. Identify the modes of operation and compute the operating frequency of that mode based on the following program segment. Identify the Timer of the Arduino Microcontroller. The system clock frequency is pq MHz.

```
DDRD |= (1<<PD5);
pinMode(5, OUTPUT);
OCR0B= (150+a+b); // Load OCR0B for setting its duty cycle
// Configure TCCR0A and TCCR0B registers for the mode and pre-scaler
TCCR0A |= (1 << COM0B1) | (1<<WGM01) | (1<<WGM00);
TCCR0B |= (1<<CS02) | (1<<CS00);
```

4. Design an ***a***-bit shifter circuit for the listed shift functions provided in Table 1. Explain its operation for variouscases of select inputs.

Table 1: Functions of control variables

Binary Code	**Functions of selection variables**					
	A	***B***	***D***	***F* with C_{in} = 0**	***F* with C_{in} = 1**	***H***
0 0 0	Input Data	Input Data	None	A-1	A	1's to the output Bus
0 0 1	R1	R1	R1	A+B	A+B+1	Shift Left with I_L = 0
0 1 0	R2	R2	R2	A-B-1	A-B	No Shift
0 1 1	R3	R3	R3	A	A+1	Circulate Left with Carry
1 0 0	R4	R4	R4	$\bar{A}$	X	0's to the output Bus
1 0 1	R5	R5	R5	AX**OR** B	X	0's & 1's to the lower and upper nibbles
1 1 0	R6	R6	R6	A **AND** B	X	Circulate-Right with Carry
1 1 1	R7	R7	R7	A **OR** B	X	Shift Right with I_R = 0

5. Design a (q + r)-bit shifter for the four shifting operations listed in the following Table:

Binary Code	**The function of selection variables**					
	A	**B**	**D**	**F with C_{in} = 0**	**F with C_{in} = 1**	**H**
0 0	Input Data	Input Data	None	A	A+1	**Shift Left with I_L=0**
0 1	R1	R1	R1	A+B	A+B+1	**Shift Right with I_R=0**
1 0	R2	R2	R2	A+B′	A+B′+1	**1's to the output Bus**
1 1	R3	R3	R3	A-1	A	**0's to the output Bus**

6. Prepare a flow chart that will count the number of 1's in a register, R4 and then store the counts in register R6.
   Determine the outputs of the R6 (in binary) and R4 (in decimal) registers as well as of the carry flag (C) after each clock cycle or timing state.

Timing States	R4								C	R6
	1	1	0	1	0	0	1	1	0	0
T1										
T2										
T3										
T4										
T5										
T6										
T7										
T8										

7. Develop the control words in binary and hexadecimal formats using the information provided in Table 1 for thefollowing micro-operations:

i.	Re←Ra+Rb	ii.	Rd←3(Re – 0)/3
iii.	Rq←SHL Rp	iv.	Output←Rc
v.	Rd←Rc	vi.	Rb←0
vii.	Rq←Input	viii.	Rq←Rp-Ra
ix.	Rr←SHR Rb	x.	Rc←CRC Rd

** If any value of a-e goes above 7 then it should be assumed as 7.*

The necessary bits for the control word are presented in Table 2.

Table 2: 16-bit control word sequence

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A			*B*			*D*			*F*			C_{in}	*H*		

One example is shown as follows:

Micro-operation	*A*	*B*	*D*	*F*	C_{in}	*H*	In Hex
R5← CRC (R3+R4)	011	100	101	001	0	110	7296h

8. Develop the control memory outputs for the sequence in Table 3 using the information listed in Table 1. To complete the memory outputs, use the microinstructions that you have developed in question no. 7.

Table 3: Control memory bit sequence

ROM Address			ROM outputs													
			Control Word									Address			Mux Select	
			1	2	3	4	5	6	7	8	9	10	11	12	13	14
0	0	0														
0	0	1														
0	1	0														
0	1	1														
1	0	0														
1	0	1														
1	1	0														
1	1	1														

Solution: 1

ID: 22-46013-1
PQ-abcde-r

f_{osc} = ac MHz
= 40 MHz
= 40×10^6 Hz

$UBBR_n$ = 010110101110 = 1454

Asynchronous Normal Mode:

Baud rate = $\frac{40 \times 10^6}{16(1454+1)}$ = 1719 bps

Error = $\frac{1200 - 1719}{1200} \times 100$

= -43.25 % > ±2 %

So, there will be a communication error

Asynchronous Double Speed Mode

Baud rate = $\frac{40 \times 10^6}{8(1454+1)}$ = 3437 bps

Error = $\frac{2400 - 3437}{2400} \times 100$ = -43.20 > ±2 %.

So, there will be a communication error

Synchronous Master mode

Baud rate = $\frac{40 \times 10^6}{2(1454+1)}$ = 13746

Error = $\frac{9600 - 13746}{9600} \times 100$ = -43.18 % > ±2 %,

So there will be a communication Error

Solution: 2

ID: 22-46013-1
Pq-abcde-r

Given,

$WGM01 = 1\ WGM00 = WGM02 = 1$

$OCROA = (200 + a+b+c) = 200+4+6+0 = 210$

$OCROB = (100 + d+e) = (100+1+3) = 114$

∴ Mode of operation is Fast PWM 7(111)

And, $CS01 = CS00 = 1$

∴ Prescaler = 64

And, $COM0B1 = 1$

∴ Non-Inverting Mode

∴ Duty Cycle for OCROA,

$$OCROA = \frac{256D}{100} - 1$$

$$D = \frac{(210+1)\,100}{256} = 82.42\%.$$

82.42% duty Cycle

For OCR0B,

$$OCR0B = \frac{256D}{100} - 1$$

$$D = \frac{(114+1) \times 100}{256} = 44.92\%$$

$$= 44.92\%$$

44.92 %

Given,

$f_{clk\_IO} = 24\ MHz = 12\ MHz$

$$\therefore f_{OCnxPWM} = \frac{f_{clk\_IO}}{N \times 256}$$

$$= \frac{12 \times 10^6}{64 \times 256}$$

$$= 732.42\ Hz$$

Operating frequency = 732.42 Hz

Solution: 3

ID: 22-46013-1
pq-abcde-r

$OCR0B = (150 + a + b)$
$= 150 + 4 + 6$
$= 160$

$WGM01 = WGM00 = 1$

∴ Mode of operation is Fast PWM Mode 3(011)

$CS01 = CS00 = 1$

∴ Prescaler = 64

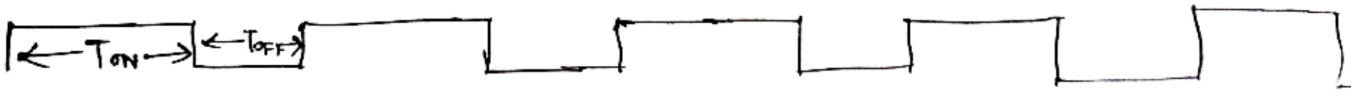
$COM0B1 = 1$

∴ No-inverting Mode

Duty cycle,

$$OCR0B = \frac{256D}{100} - 1$$

$$D = \frac{(160+1) \times 100}{256} = 62.89\%$$



$f_{clk\_IO} = 22\ MHz = 22\ MHz$

$$f_{OCnxPWM} = \frac{f_{clk\_IO}}{N \times 256} = \frac{22 \times 10^6}{64 \times 256} = 1342.77\ Hz$$

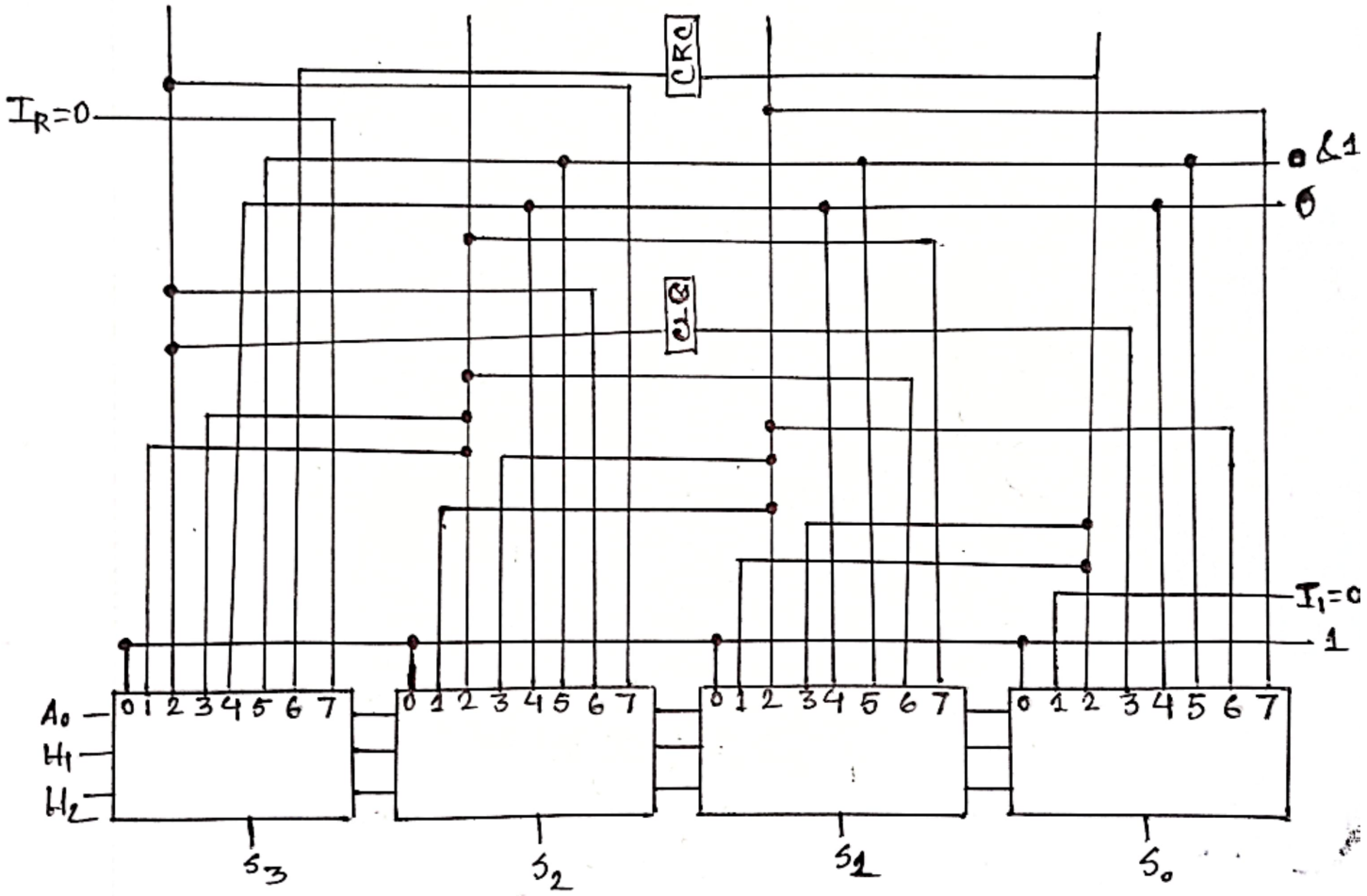
∴ Operating frequency is 1342.77Hz

solution: 4

ID: 22-46013-1

a-bit shifter

4-bit shifter

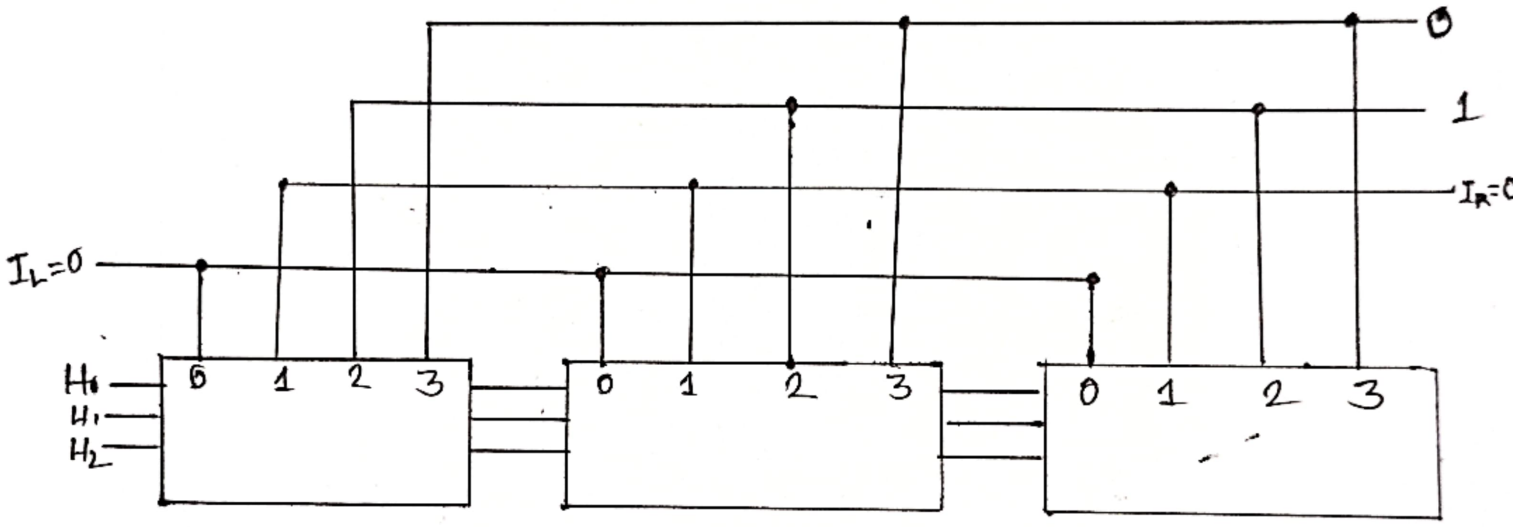


Solution: 5

ID: 22-46013-1
Par-abede-r

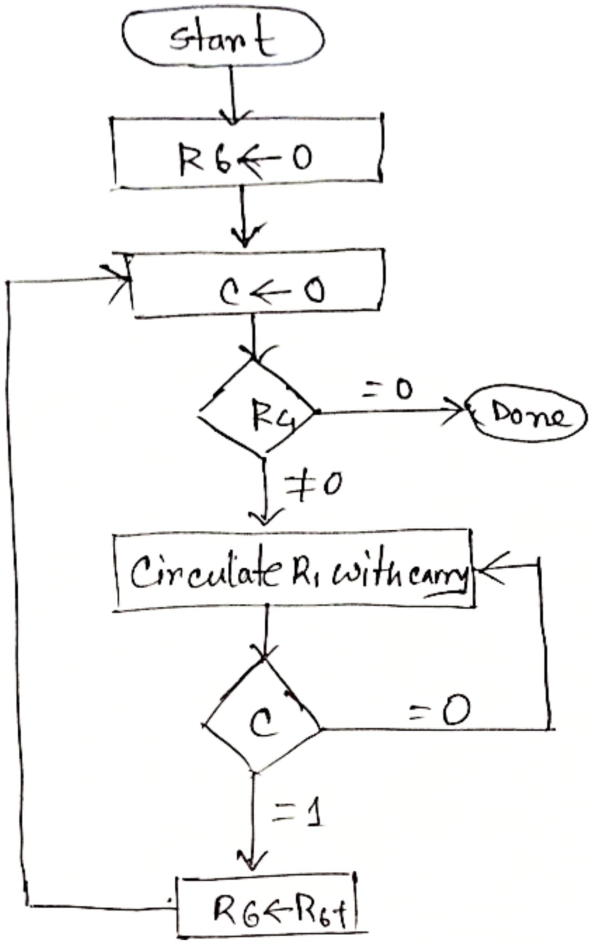
(q+r) -bit shifter

(2+1) = 3-bit shifter



Solution: 6

Flowchart:



Timing states	R_4								C	R_6
	1	1	0	1	0	0	1	1	0	0
T_1	0	1	1	0	1	0	0	1	1	1
T_2	0	0	1	1	0	1	0	0	1	2
T_3	0	0	0	1	1	0	1	0	0	2
T_4	0	0	0	0	1	1	0	1	0	2
T_5	0	0	0	0	0	1	1	0	1	3
T_6	0	0	0	0	0	0	1	1	0	3
T_7	0	0	0	0	0	0	0	1	1	4
T_8	0	0	0	0	0	0	0	0	1	5

Solution: 7

ID: 22-46013-1
Pq-abcde-n

Microoperation	A	B	D	F	Cin	H
$R_7 \leftarrow R_4 + R_7$	100	111	111	001	0	000
$R_1 \leftarrow 3(R_7 - 0)/3$	111	000	001	000	0	000
$R_2 \leftarrow SHL\ R_2$	010	010	010	100	0	010
Output $\leftarrow R_1$	001	000	000	0	0	000
$R_1 \leftarrow R_1$	001	000	001	000	0	000
$R_7 \leftarrow 0$	000	000	111	000	0	000
$R_2 \leftarrow$ Input	000	000	010	000	0	000
$R_2 \leftarrow R_2 - R_4$	010	100	010	010	1	000
$R_1 \leftarrow SHR\ R_7$	111	111	001	100	0	001
$R_1 \leftarrow CRC\ R_1$	001	001	001	100	0	101

Solution: 8

ROM Address			ROM Outputs													
			Control World								Address			Mux Select		
			1	2	3	4	5	6	7	8	10	11	12	13	14
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	1
0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0
0	1	1	0	0	0	1	0	1	0	0	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	0	1	0	1	0	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	1	1	1	0	1	0	0	1	1	1	0	1
1	1	1	0	0	0	0	1	1	0	1	0	0	0	0	1