

Arria 10 CvP Initialization and Partial Reconfiguration over PCI Express User Guide



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Configuration via Protocol (CvP) is a configuration scheme supported in Arria® V, Cyclone® V, Stratix® V, and Arria 10 device families. The CvP configuration scheme creates separate images for the periphery and core logic. You can store the periphery image in a local configuration device and the core image in the host memory, reducing system costs and increasing the security for the proprietary core image. CvP configures the FPGA fabric through the PCI Express® (PCIe) link and it is available for Endpoint variants only. CvP allows the PCIe endpoint to wake up within 200 ms.

Related Information

- [Introduction to Altera IP Cores](#)
Provides general information about all Altera IP cores, including parameterizing, generating, upgrading, and simulating IP.
- [Project Management Best Practices](#)
Guidelines for efficient management and portability of your project and IP files.

Benefits of Using CvP

The CvP configuration scheme has the following advantages:

- Reduces system costs by reducing the size of the local flash device used to store the periphery configuration data.
- Improves security for the proprietary core bitstream. CvP ensures that the PCIe host can exclusively access the FPGA core image.
- Provides a simpler software model for configuration. A smart host can use the PCIe protocol and the application topology to initialize and update the FPGA fabric.
- Facilitates hardware acceleration.

CvP System

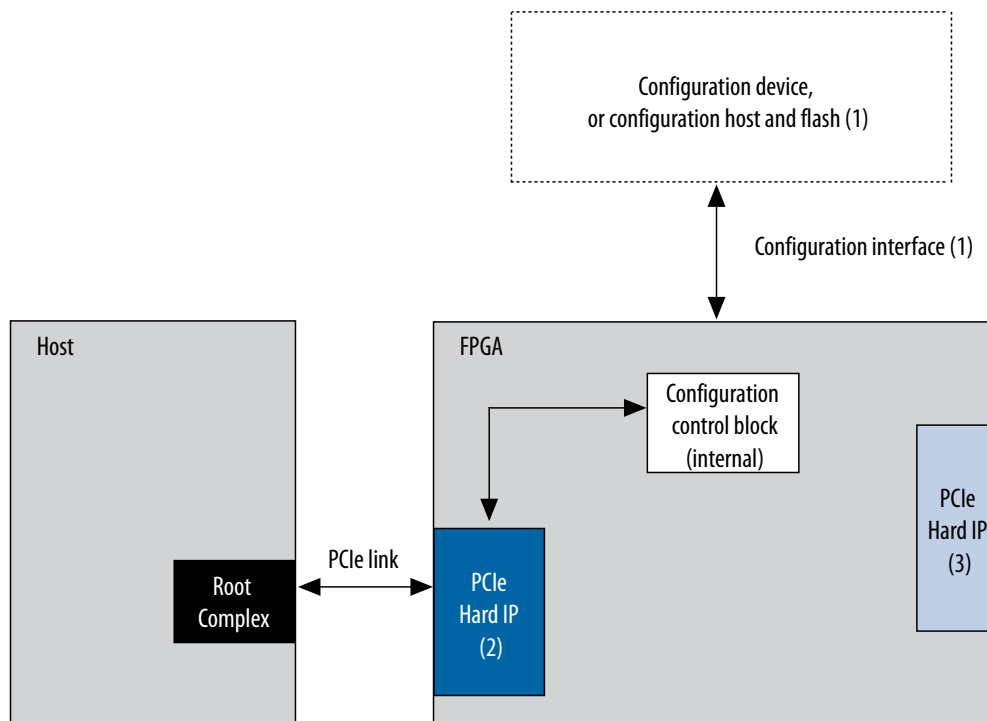
The following figure shows the required components for a CvP system.

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Figure 1-1: CvP Block Diagram



A CvP system typically consists of an FPGA, a PCIe host, and a configuration device.

1. The configuration device is connected to the FPGA using the conventional configuration interface. The configuration interface can be any of the supported schemes, such as active serial (AS), passive serial (PS), or fast passive parallel (FPP). The choice of the configuration device depends on your chosen configuration scheme.
2. PCIe Hard IP block (bottom left) for CvP and other PCIe applications.
3. PCIe Hard IP block only for PCIe applications and cannot be used for CvP.

Most Arria 10 FPGAs include more than one Hard IP block for PCI Express. The CvP configuration scheme can only utilize the bottom left PCIe Hard IP block on each device. It must be configured as an Endpoint.

CvP Support for Arria 10 Devices

Table 1-1: CvP Support for Arria 10 Devices

Device	CvP Modes Supported		
	PCIe Gen 1	PCIe Gen 2	PCIe Gen 3
Arria 10	CvP initialization	CvP initialization	CvP initialization

Note: For Arria 10 devices, use Partial Reconfiguration over Protocol instead of CvP Update. You can use the PCIe bus to perform Partial Reconfiguration.

Related Information

- **Configuration via Protocol (CvP) Implementation in V-series FPGA Devices User Guide**
Provides more information about the CvP support for Stratix V, Arria V, and Cyclone V device families.
- **Partial Reconfiguration over PCI Express in Arria 10** on page 5-1
- **Creating a Partial Reconfiguration Design**
Provides more information about the Partial Reconfiguration methodology and utilization.

CvP Initialization

This scheme configures the core of the FPGA through the PCIe link upon system power up. Initialization refers to the initial fabric configuration image loaded in the FPGA fabric after power up.

Configuration Images

In CvP, you partition your design into two images: core image and periphery image.

You use the Quartus® Prime software to generate the following images:

- Periphery image (*.periph.jic) — contains general purpose I/Os (GPIOs), I/O registers, the GCLK, QCLK, and RCLK clock networks, and logic that is implemented in hard IP such as the JTAG interface, PR block, CRC block, Oscillator block, Impedance control block, Chip ID, ASMI block, Remote update block, Temperature sensor, and Hard IP for PCI Express IP Core. These components are included in the periphery image because they are controlled by I/O periphery register bits. The entire periphery image is static and cannot be reconfigured.
- Core image (*.core.rbf) — contains logic that is programmed by configuration RAM (CRAM). This image includes LABs, DSP, and embedded memory. The single static core image may include PR reconfigurable regions.
 - Reconfigurable region — This region can be programmed in user mode while the PCIe link is up and fully enumerated. It must contain only resources that are controlled by CRAM such as LABs, embedded RAM blocks, and DSP blocks in the FPGA core image. It cannot contain any periphery components such as GPIOs, transceivers, PLL, I/O blocks, the Hard IP for PCI Express IP Core, or other components included in the periphery image.
 - Static region — This region cannot be modified.

The periphery image is stored in an external configuration device and is loaded into the FPGA through the conventional configuration scheme. The core image is stored in a host memory and loaded into the FPGA through the PCIe link. All other periphery and core resources are frozen until the FPGA enters user mode.

After the periphery image configuration is complete, the CONF_DONE signal goes high and allows the FPGA to start PCIe link training. During PCIe link training, the FPGA is not in user mode. When PCIe link training is complete, the PCIe link transitions to L0 state and then through PCIe enumeration. The PCIe host then initiates the core image configuration through the PCIe link.

After the core image configuration is complete, the CvP_CONF_DONE pin goes high, indicating the FPGA is fully configured.

After the FPGA is fully configured, the FPGA enters user mode. If the INIT_DONE signal is enabled, the INIT_DONE signal goes high after initialization is complete and the FPGA enters user mode.

In user mode, the PCIe links are available for normal PCIe applications. You can also use PR over PCI Express to change re-configurable regions within the single CvP core image.

Related Information

- [Arria 10 Core Fabric and General Purpose I/Os Handbook](#)
Provides more information about the location of the transceiver banks and I/O banks.
- [Configuration Timing Waveforms](#)
Provides more information with the timing diagrams for different configuration modes.

CvP Compression and Encryption Features

Data Compression

You can choose to compress the core image by turning on the **Generate compressed bitstream** option in the **Configuration** page of the **Device and Pin Options** dialog box in the Quartus Prime software. The periphery image cannot be compressed. Compressing the core image reduces the storage requirement.

Data Encryption

You can choose to encrypt the core image. The periphery image cannot be encrypted. To configure the FPGA with an encrypted core image, you must pre-program the FPGA with a security key. This key is then used to decrypt the incoming configuration bitstream.

A key-programmed FPGA can accept both encrypted and unencrypted bitstreams if you configure the FPGA using the AS, PS, or FPP scheme. However, if you use CvP, a key-programmed FPGA can only accept encrypted bitstreams. Use the same key to encrypt all revisions of the core image.

Table 1-2: Supported Clock Source for Encrypted Configuration Data

The following table lists the supported clock source for each conventional scheme used in a CvP system.

Key Types	Active Serial		Passive Serial	Fast Passive Parallel
	External Clock	Internal Clock	External Clock	External Clock
Volatile key	Yes	Yes	Yes	Yes
Non-volatile key	No	12.5 MHz	Yes	Yes

Related Information

- [Using the Design Security Features in Altera FPGAs](#)
- [Arria 10 Device Datasheet](#)
Provides more information about the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Arria 10 devices.

CvP Pins

The following table lists the CvP pin descriptions and connection guidelines.

Table 1-3: CvP pin descriptions and connection guidelines

Pin Name	Pin Type	Pin Description	Pin Connection
CvP_CONF_DONE	Output	<p>The <code>CvP_CONF_DONE</code> pin is driven low during configuration. When configuration via PCIe is complete, this signal is released and either actively driven high, or pulled high by an external pull-up resistor.</p> <p>During FPGA configuration in CvP initialization mode, you must observe this pin after the <code>CONF_DONE</code> pin goes high to determine if the FPGA is successfully configured.</p> <p>If you are not using the CvP modes, you can use this pin as a user I/O pin.</p>	<p>If this pin is set as dedicated output, the V_{CCPGM} power supply must meet the input voltage specification of the receiving side.</p> <p>If this pin is set as an open-drain output, connect the pin to an external 10-kΩ pull-up resistor to the V_{CCPGM} power supply or a different pull-up voltage that meets the input voltage specification of the receiving side. This gives an advantage on the voltage leveling.</p>
INIT_DONE	Output	<p>When you enable this pin, a transition from low to high at the pin indicates the device has entered user mode. If the <code>INIT_DONE</code> output is enabled, the <code>INIT_DONE</code> pin cannot be used as a user I/O pin after configuration.</p> <p>This is a dual-purpose pin and can be used as an I/O pin when not enabled as the <code>INIT_DONE</code> pin.</p>	<p>When you use the optionally open-drain output dedicated <code>INIT_DONE</code> pin, connect this pin to an external 10-kΩ pull-up resistor to V_{CCPGM}.</p> <p>When you use this pin in an AS or PS multi-device configuration mode, ensure you enable the <code>INIT_DONE</code> pin in the Quartus Prime designs. When you do not use the dedicated <code>INIT_DONE</code> optionally open-drain output, and when this pin is not used as an I/O pin, connect this pin as defined in the Quartus Prime software.</p>

Pin Name	Pin Type	Pin Description	Pin Connection
CONF_DONE	Bidirectional	<p>Dedicated configuration done pin.</p> <p>As a status output, the CONF_DONE pin drives low before and during configuration. After all configuration data is received without error and the initialization cycle starts, CONF_DONE is released.</p> <p>As a status input, the CONF_DONE pin goes high after all data is received. Then the device initializes and enters user mode. This pin is not available as a user I/O pin.</p>	<p>Connect an external 10-kΩ pull-up resistors to VCCPGM. VCCPGM must be high enough to meet the VIH specification of the I/O on the device and the external host.</p> <p>When you use passive configuration schemes, the configuration controller monitors this pin.</p>
nPERST[L,R][0:1]	Input	<p>This pin is connected to the Hard IP for PCI Express IP Core as a dedicated fundamental reset pin for PCIe usage. If the signal is low, the transceivers and dedicated PCIe Hard IP block that you use for CvP operation are in the reset mode.</p>	<p>Connect the nPERST[L,R]0/nPERST[L,R]1 to the PERST# pin of the PCIe slot. This pin is powered by 1.8V supply and must be driven by 1.8V compatible I/O standards.</p> <p>Only one nPERST pin is used per PCIe Hard IP. These pins have the following locations:</p> <ul style="list-style-type: none"> nPERSTL0 = Bottom Left PCIe HIP & CvP nPERSTL1 = Top Left PCIe Hard IP (When available) nPERSTR0 = Bottom Right PCIe Hard IP (When available) nPERSTR1 = Top Right PCIe Hard IP (When available) <p>For maximum compatibility, always use the bottom left PCIe Hard IP first, as this is the only location that supports Configuration via Protocol (CvP) using the PCIe link.</p>

Related Information

- [Pin Connection Guidelines for Arria 10 device family](#)
- [Arria 10 Device Datasheet](#)

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Designing CvP for an Open System

While designing a CvP system for an Open System where you don't control both ends of the PCIe link completely, ensure that you observe the guidelines provided in this section.

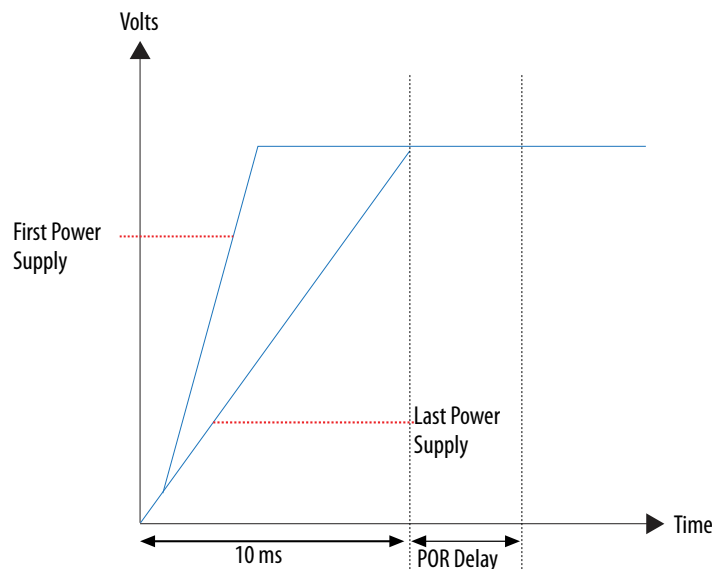
FPGA Power Supplies Ramp Time Requirement

For an open system, you must ensure that your design adheres to the FPGA power supplies ramp-up time requirement.

The power-on reset (POR) circuitry keeps the FPGA in the reset state until the power supply outputs are in the recommended operating range. A POR event occurs from when you power up the FPGA until the power supplies reach the recommended operating range within the maximum power supply ramp time, t_{RAMP} . If t_{RAMP} is not met, the device I/O pins and programming registers remain tri-stated, during which device configuration could fail.

For CvP, the total t_{RAMP} must be less than 10 ms, from the first power supply ramp-up to the last power supply ramp-up. You must select fast POR by setting the `PORSEL` pin to high. The fast POR delay time is in the range of 4–12 ms, allowing sufficient time after POR for the PCIe link to start initialization and configuration.

Figure 2-1: Power Supplies Ramp-Up Time and POR



PCIe Wake-Up Time Requirement

For an open system, you must ensure that the PCIe link meets the PCIe wake-up time requirement as defined in the *PCI Express CARD Electromechanical Specification*. The transition from power-on to the link active (L_0) state for the PCIe wake-up timing specification must be within 200 ms. The timing from FPGA power-up until the Hard IP for PCI Express IP Core in the FPGA is ready for link training must be within 120 ms.

PCIe Wake-Up Time Requirement for CvP Initialization

For CvP initialization mode, the Hard IP for PCI Express IP core is guaranteed to meet the 120 ms requirement because the periphery image configuration time is significantly less than the full FPGA configuration time. Therefore, you can choose any of the conventional configuration schemes for the periphery image configuration.

To ensure successful configuration, all POR-monitored power supplies must ramp up monotonically to the operating range within the 10 ms ramp-up time. The $\overline{\text{PERST}}\#$ signal indicates when the FPGA power supplies are within their specified voltage tolerances and the REFCLK is stable. The embedded hard reset controller triggers after the internal status signal indicates that the periphery image has been loaded. This reset does not trigger off of $\overline{\text{PERST}}\#$. For CvP initialization mode, the PCIe link supports the FPGA core image configuration and PCIe applications in user mode.

Note: For Gen 2 capable Endpoints, after loading the core **.sof**, Altera recommends that you verify that the link has been trained to the expected Gen 2 rate. If the link is not operating at Gen 2, host software can trigger the Endpoint to retrain.

Figure 2-2: PCIe Timing Sequence in CvP Initialization Mode

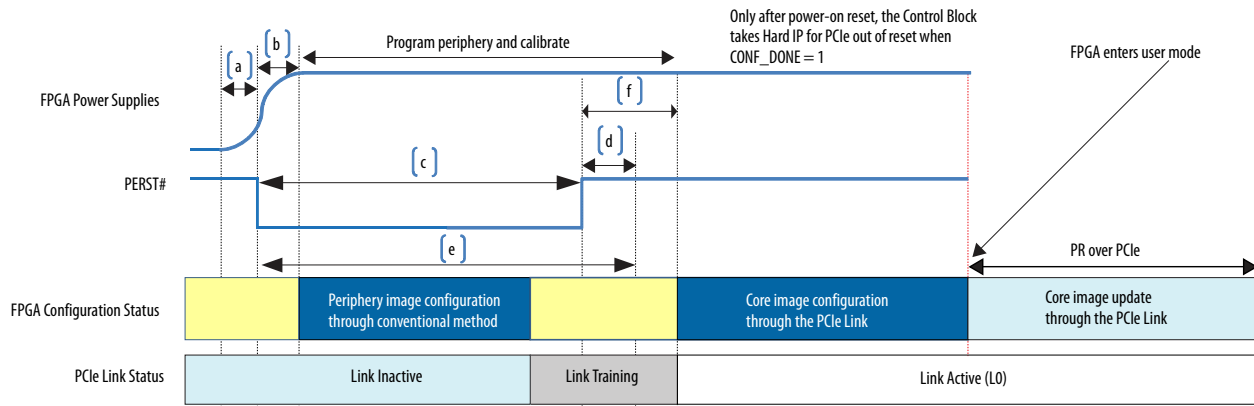


Table 2-1: Power-Up Sequence Timing in CvP Initialization Mode

Timing Sequence	Timing Range (ms)	Description
a	10	Maximum ramp-up time requirement for all POR-monitored power supplies in the FPGA to reach their respective operating range.
b	4–12	FPGA POR delay time.
c	100	Minimum PERST# signal active time from the host.
d	20	Minimum PERST# signal inactive time from the host before the PCIe link enters training state.
e	120	Maximum time from the FPGA power up to the end of periphery configuration in CvP initialization mode.
f	100	Maximum time PCIe device must enter L0 after PERST# is deasserted.

Related Information

- [Power Management in Arria 10 Devices](#)
Provides more information about the power requirements.
- [PCI Express CARD Electromechanical Specification](#)

Designing CvP for a Closed System

While designing CvP for a closed system where you control both ends of the PCIe link completely, estimate the periphery configuration time for CvP initialization. You must ensure that the estimated configuration time is within the time allowed by the PCIe host.

Understanding the Design Steps for CvP Initialization in Arria 10

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CvP initialization divides the design into periphery and core images. The periphery image is stored in a local flash device on the PCB. You can program the periphery through JTAG. The core image is stored in host memory. You must download the core image to the FPGA using the PCI Express link.

You must specify CvP initialization mode in the Quartus Prime software by selecting the CvP Settings Power up and subsequent core configuration and also turn on **Enable Configuration via Protocol** in the **Arria 10 Hard IP for PCI Express**. You might choose CvP initialization to prevent unauthorized access to the core image as well as save cost by storing the core image in the host memory.

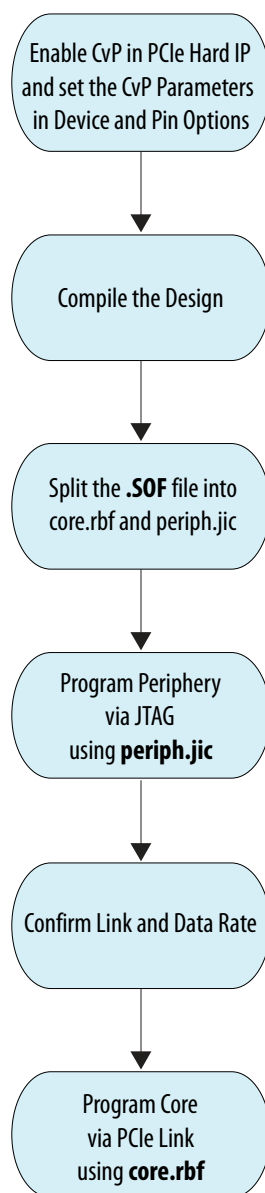
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Figure 3-1: Design Flow for CvP Initialization

The following figure provides the high-level steps for CvP Initialization.



Note: For CvP initialization, you must use the CMU PLL and the Hard Reset Controller for the PCI Express Hard IP.

The CvP initialization demonstration walkthrough includes the following steps:

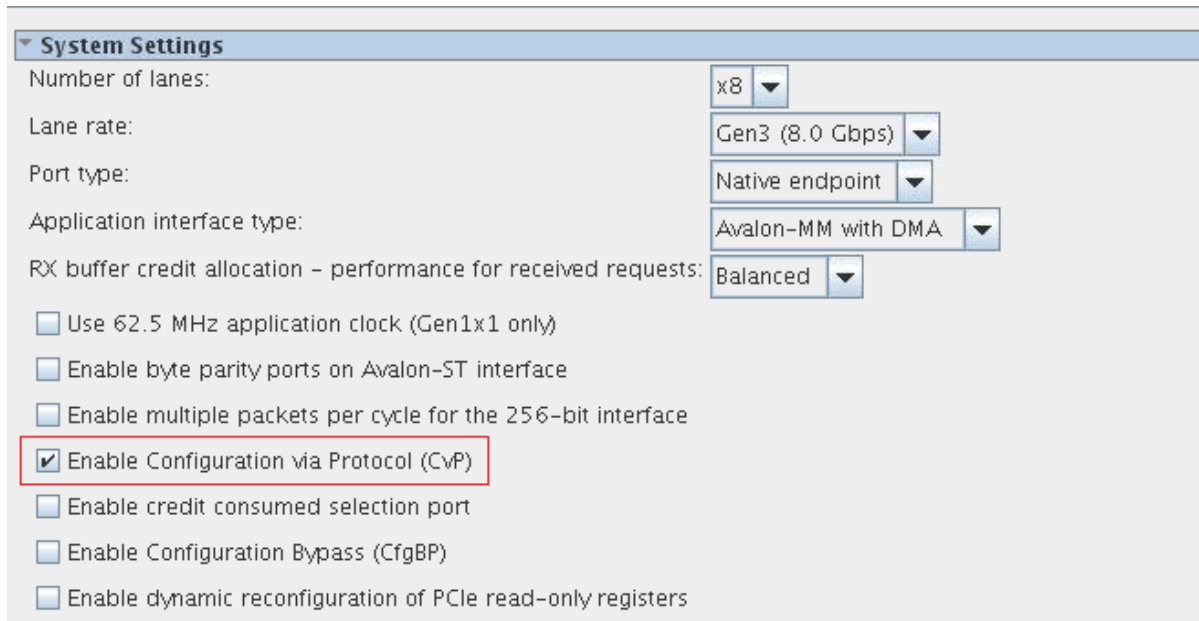
1. [Generating the Synthesis HDL Files for Arria 10 PCI Express IP Core](#) on page 3-3
2. [Setting up the CvP Parameters in Device and Pin Options](#) on page 3-3
3. [Compiling the Design](#) on page 3-4
4. [Splitting the SOF File](#) on page 3-4
5. [Bringing up the Hardware](#) on page 3-5

Generating the Synthesis HDL Files for Arria 10 PCI Express IP Core

Follow these steps to generate the synthesis HDL files with CvP enabled:

1. On the Tools menu, select **Qsys**.
2. Open **.qsys** file of the project.
3. On the **System Contents** tab, right-click **Arria 10 Hard IP for PCI Express** and select **Edit**.
4. Under System Settings, turn on **Enable Configuration via Protocol** as shown in the following figure:

Figure 3-2: Illustrating the specified option in Systems Setting dialog box



5. Click Finish.
6. On the Generation tab, specify your parameters to generate RTL. Then click Generate at the bottom of the window.

Related Information

[Arria 10 Avalon-MM Interface for PCIe Solutions User Guide](#)

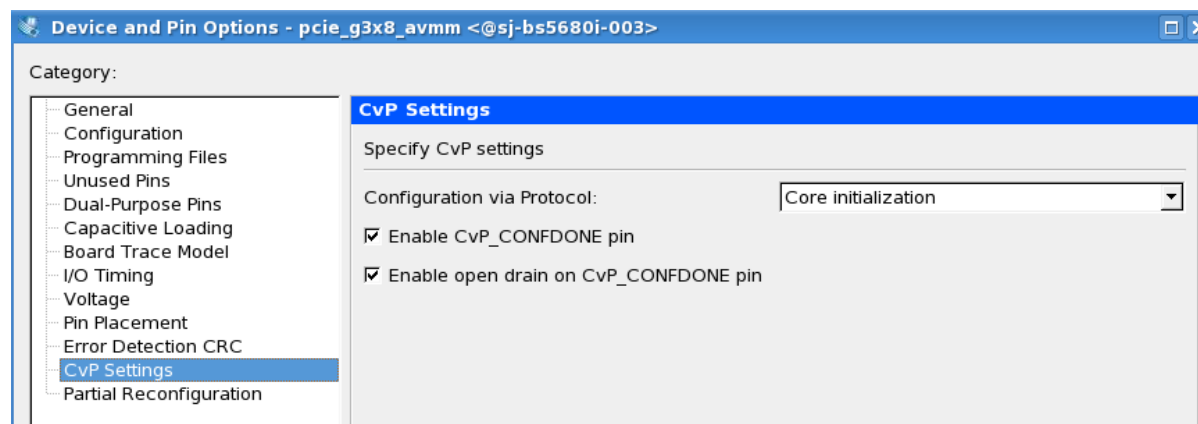
Setting up the CvP Parameters in Device and Pin Options

Follow these steps to specify CvP parameters:

1. On the Quartus Prime Assignments menu, select **Device**, and then click **Device and Pin Options**.
2. Under **Category** select **General**, and then enable the following option:
 - a. **Auto-restart configuration after error**, enable this option to allow automatic restart of configuration attempts if an error is detected. Any restarted configuration may exceed the required PCIe startup time to allow bus enumeration and prevent the use of quartus_cvp for core programming. Leave all other options disabled.
3. Under Category, select **CvP Settings**, and specify the following settings:

Parameter	Value
Configuration via Protocol	Core initialization
Enable CvP_CONFDONE pin	Turn this option on.
Enable open drain on CvP_CONFDONE pin	Turn this option on.

Figure 3-3: Illustrating the specified CvP parameters in Device and Pin options dialog box



Compiling the Design

1. To compile the design, on the Processing menu, select **Start compilation** to create the .SOF file.

Splitting the SOF File

Follow these steps to split your .SOF file into separate images for the periphery and core logic.

1. After the .SOF file is generated, under File menu, select **Convert Programming File**.
2. Under **Output programming file** section, specify the following parameters:

Parameter	Value
Programming file type	JTAG Indirect Configuration File (*.jic)
Configuration device	EPCQL1024
Mode	Active Serial
File name	*.jic
Create Memory Map File	Turn this option on.
Create CvP files	Turn this option on. This box is greyed out until you specify the SOE Data file under Input files to convert .

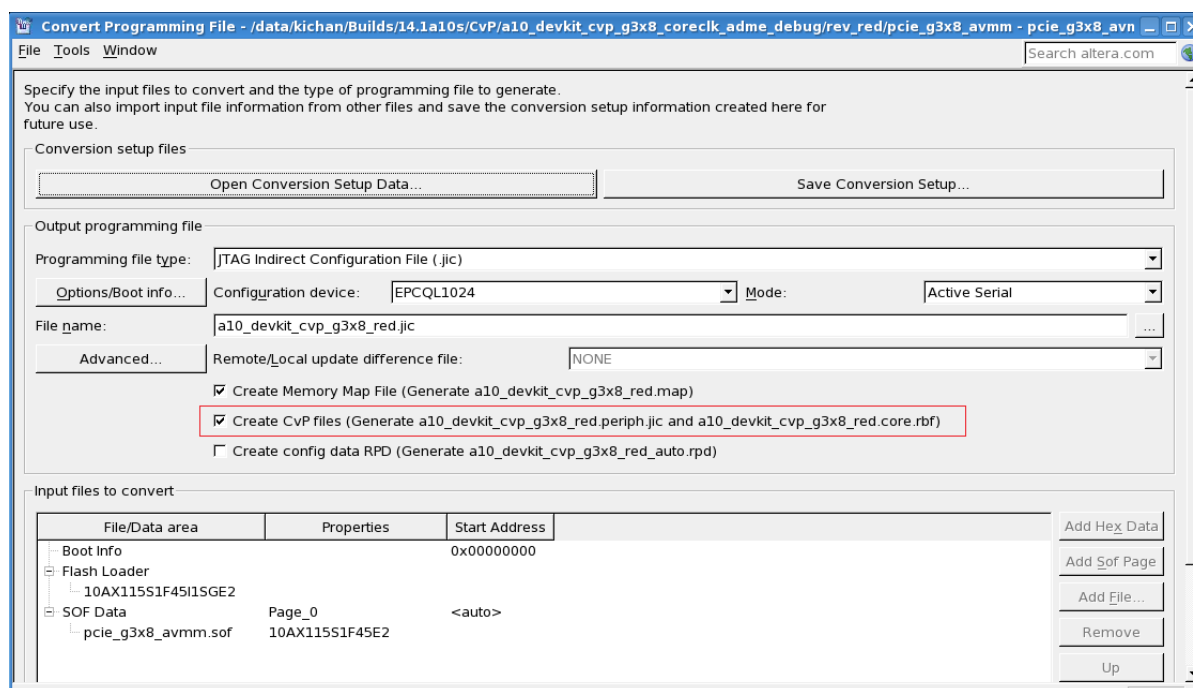
- Under Input files to convert, specify the following parameters:

Parameter	Value
Flash Loader	10AX115S1F45I1SG
SOF Data	*.sof

- Make sure to turn on the **Create CvP files**.

Note: If you do not check this box, the Quartus Prime software does not create separate files for the periphery and core images.

Figure 3-4: Illustrating the above specified options in the Convert Programming File GUI



- Click Generate to create *.periph.jic and *.core.rbf files.

Bringing up the Hardware

Before testing the design in hardware, you must install Jungo WinDriver in your DUT system. You can also install RW Utilities or other system verification tools to monitor the link status of the Endpoint and to observe traffic on the link. You can download these utilities for free from many web sites.

The test setup includes the following components:

- Arria 10 FPGA Development Kit
- USB Blaster
- A DUT PC with PCI Express slot to plug in the Arria 10 FPGA Development Kit
- A host PC running the Quartus Prime software to program the peripheral image, .sof or .pof file

Although a separate host PC is not strictly necessary, it makes testing less cumbersome.

Installing Jungo WinDriver in Windows Systems

1. Navigate to `<Quartus Prime installation path>\quartus\drivers\wdrv\windows<32 or 64>`.
2. Run the command:
 - `wdreg -inf windrvr6.inf install`
3. Copy the `wdapi1021.dll` file to the `%windir%\system32` directory.

Installing Jungo WinDriver in Linux Systems

1. Navigate to `<Quartus Prime installation path>/quartus/drivers/wdrv/linux<32 or 64>`.
2. Run the following commands:
 - a. `./configure --disable-usb-support`
 - b. `make`
 - c. `su`
 - d. `make install`
3. You can change the permissions for the device file. For example, `chmod 666 /dev/windrvr6`.
4. For 64-bit Linux systems, set the `Quartus_64BIT` environment variable before you run `quartus_cvp` using the following command:
 - `export QUARTUS_64BIT=1`
5. You can use the `quartus_cvp` command to download *core .rbf files to your FPGA. The following table lists the `quartus_cvp` commands for all modes.

Table 3-1: Syntax for quartus_cvp Commands

Mode	quartus_cvp Command
Uncompressed	<code>quartus_cvp --vid=<Vendor ID> --did=<Device ID> <Core .rbf file path></code>
Unencrypted	
Compressed	<code>quartus_cvp -c --vid=<Vendor ID> --did=<Device ID> <Core .rbf file path></code>
Encrypted	<code>quartus_cvp -e --vid=<Vendor ID> --did=<Device ID> <Core .rbf file path></code>
Compressed and encrypted	<code>quartus_cvp -c -e --vid=<Vendor ID> --did=<Device ID> <Core .rbf file path></code>

Modifying MSEL/DIP switch on Arria 10 Dev-Kit

The MSEL/DIP switch labeled **SW5** on the back of the Arria 10 FPGA Development Kit. The right position signifies logic zero and the left position signifies logic one. For example, to set the `MSEL [2:0] = 011` follow the sequence as left, left, right from top to bottom.

Table 3-2: MSEL Pin Settings for Each Configuration Scheme of Arria 10 Devices

- Do not drive the `MSEL` pins with a microprocessor or another device.
- Use PS or FPP MSEL pin setting for configuration via HPS.

Configuration Scheme	V _{CCPGM} (V)	Power-On Reset (POR) Delay	Valid MSEL[2..0]
JTAG-based configuration	—	—	Use any valid <code>MSEL</code> pin settings below
AS (x1 and x4)	1.8	Fast	010
		Standard	011
PS and FPP (x8, x16, and x32)	1.2/1.5/1.8	Fast	000
		Standard	001

Programming CvP Images

You must program the periphery image (**.periph.jic**) and then download the core image (**.core.rbf**) using the PCIe Link. You can use JTAG to load different programming files (i.e. **.sof/.jic/periph.pof**) into your selected CvP initialization enabled Arria 10 device.

After loading the periphery image via the JTAG port, the link should reach the expected data rate and link width. You can confirm the PCIe link status using the RW Utilities.

Follow these steps to program and test the CvP functionality:

1. Plug the Arria 10 FPGA Development Kit into the PCI Express slot of the DUT PC and power it ON. Altera recommends that you use the ATX power supply that the development kit includes.
2. On the host PC, open the Quartus Prime Tools menu and select **Programmer**.
3. Click **Auto Detect** to verify that the USB Blaster recognizes the Arria 10 FPGA.
4. Follow these steps to program the periphery image:
 - a. Select Arria 10 device, and then right click **None** under **File** column.
 - b. Navigate to **.periph.jic** file and click **Open**.
 - c. Under **Program/Configure** column, select the respective devices. For example, **10AX115S1E2** and **EPCQL1024**.
 - d. Click start to program the periphery image into **EPCQL1024** flash.

Figure 3-5: Illustrating the specified options to the program periphery image

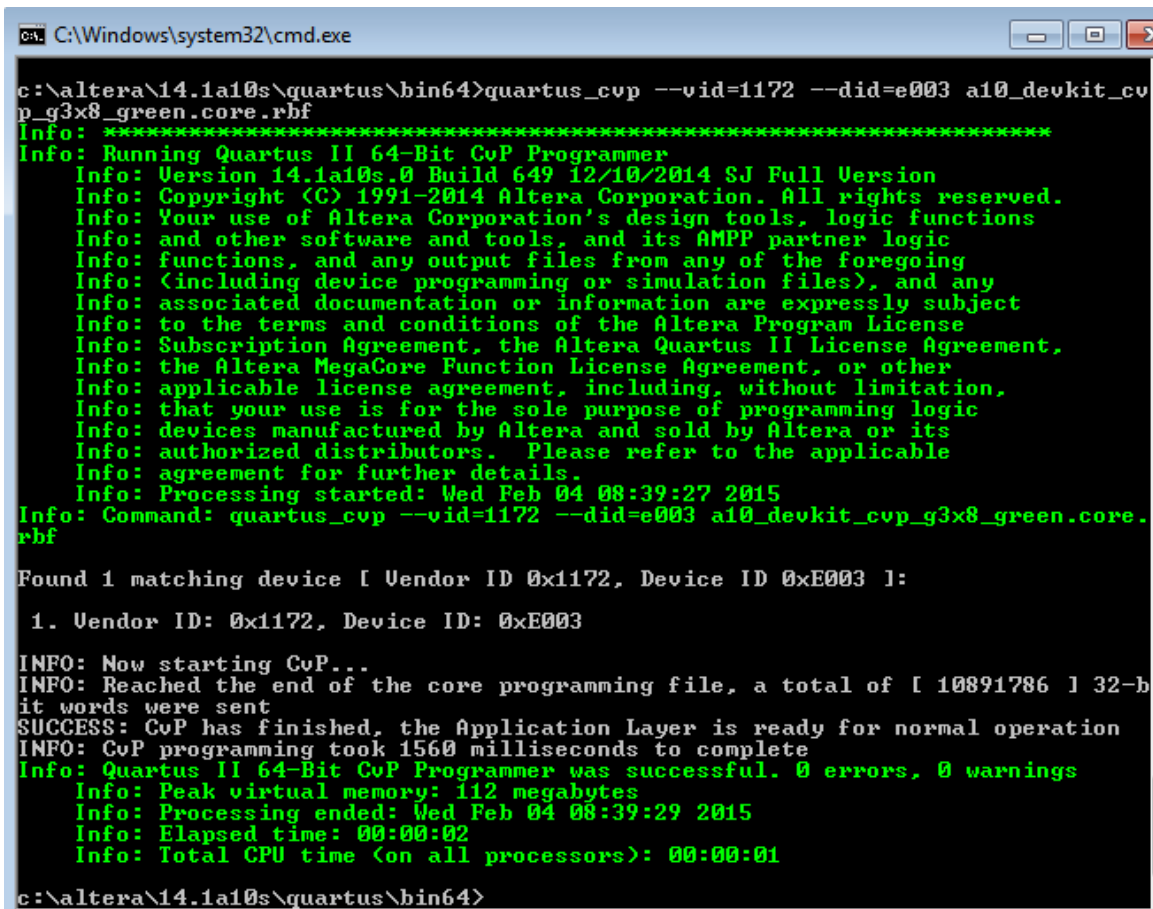
	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP
Start	Factory default SF...	10AX115S1E2	30F9C8E4	FFFFFFF	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Stop	./CvP/a10_de...	EPCQL1024	F326CDD1		<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Auto Detect	<none>	5M2210Z	00000000	00000000	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Delete	<none>	2*CFI_1Gb			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Add File...											

5. After the **.periph.jic** is programmed, the FPGA must be powered cycle to allow the new peripheral image to load from the on-board flash into the FPGA. To force the host PC to re-enumerate the link with the new image, power cycle the DUT PC and the Arria 10 FPGA Development Kit.
6. You can use RW Utilities or another system software driver to verify the link status. You can also confirm expected link speed and width.
7. Follow these steps to program the core image:
 - a. Copy the **.core.rbf** file to appropriate Quartus Prime **bin** install directory. Depending on the 32-bit or 64-bit system, the folder is `.../quartus/bin32` or `.../quartus/bin64`.
 - b. Open a **Command Prompt** in Windows, change the directory to the same mentioned above where the file is copied.
 - c. Type the following command to program the core image:


```
quartus_cvp --vid=<Vendor ID> --did=<Device ID> xxx.core.rbf
```

where the value of Vendor ID and Device ID are in hexadecimal and specified in the Hard IP for PCI Express dialog box. For example, `quartus_cvp --vid=1172 --did=e003 xxx.core.rbf`.
 - d. The figure below shows the results of a successful CvP programming.

Figure 3-6: Command Prompt Console



```
C:\Windows\system32\cmd.exe

c:\altera\14.1a10s\quartus\bin64>quartus_cvp --vid=1172 --did=e003 a10_devkit_cv
p_g3x8_green.core.rbf
Info: *****
Info: Running Quartus II 64-Bit CoP Programmer
Info: Version 14.1a10s.0 Build 649 12/10/2014 SJ Full Version
Info: Copyright (C) 1991-2014 Altera Corporation. All rights reserved.
Info: Your use of Altera Corporation's design tools, logic functions
Info: and other software and tools, and its AMPP partner logic
Info: functions, and any output files from any of the foregoing
Info: (including device programming or simulation files), and any
Info: associated documentation or information are expressly subject
Info: to the terms and conditions of the Altera Program License
Info: Subscription Agreement, the Altera Quartus II License Agreement,
Info: the Altera MegaCore Function License Agreement, or other
Info: applicable license agreement, including, without limitation,
Info: that your use is for the sole purpose of programming logic
Info: devices manufactured by Altera and sold by Altera or its
Info: authorized distributors. Please refer to the applicable
Info: agreement for further details.
Info: Processing started: Wed Feb 04 08:39:27 2015
Info: Command: quartus_cvp --vid=1172 --did=e003 a10_devkit_cv p_g3x8_green.core.
rbf

Found 1 matching device [ Vendor ID 0x1172, Device ID 0xE003 ]:

1. Vendor ID: 0x1172, Device ID: 0xE003

INFO: Now starting CoP...
INFO: Reached the end of the core programming file, a total of [ 10891786 ] 32-b
it words were sent
SUCCESS: CoP has finished, the Application Layer is ready for normal operation
INFO: CoP programming took 1560 milliseconds to complete
Info: Quartus II 64-Bit CoP Programmer was successful. 0 errors, 0 warnings
Info: Peak virtual memory: 112 megabytes
Info: Processing ended: Wed Feb 04 08:39:29 2015
Info: Elapsed time: 00:00:02
Info: Total CPU time (on all processors): 00:00:01

c:\altera\14.1a10s\quartus\bin64>
```

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CvP Driver Support

You can develop your own custom CvP driver for Linux using the sample Linux driver source code provided by Altera. The sample driver is written in C and can be downloaded from the Configuration via Protocol webpage.

You can also develop your own CvP driver using the Jungo WinDriver tool. You need to purchase a WinDriver license for this purpose.

Related Information

[Configuration via Protocol](#)

Provides more information about sample Linux device source code.

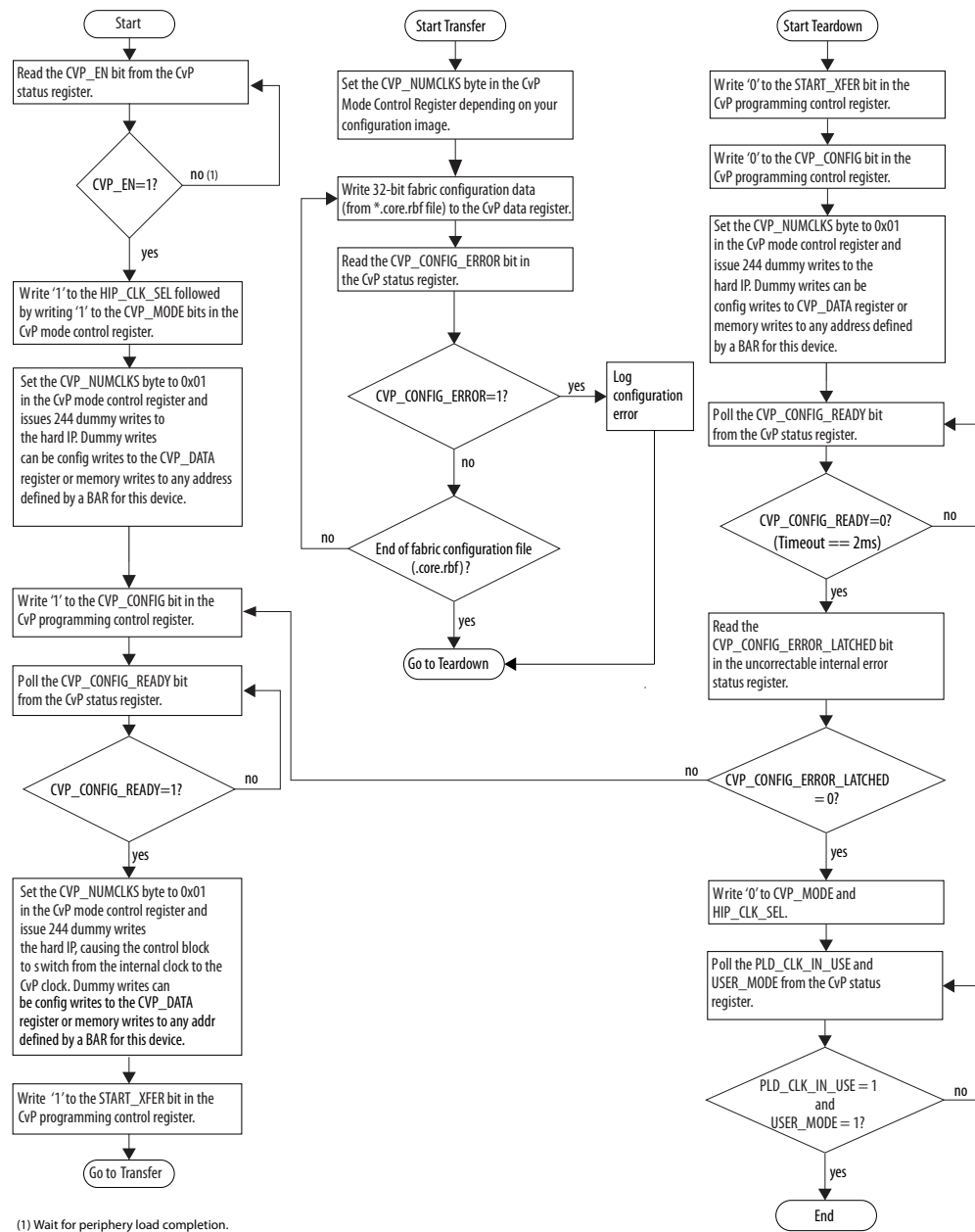
CvP Driver Flow

The following figure shows the flow of the provided CvP driver. The flow assumes that the FPGA is powered up and the control block has already configured the FPGA with the periphery image, which is indicated by the `CVP_EN` bit in the CvP status register.

As this figure indicates, the third step of the Start Teardown Flow requires 244 dummy configuration writes to the `CVP_DATA` register or 244 memory writes to an address defined by a memory space BAR for this device. Memory writes are preferred because they are higher throughput than configuration writes. The dummy writes cause a 2 ms delay, allowing the control block to complete required operations.

Figure 4-1: CvP Driver Flow

For high density devices such as Arria 10, it may be necessary to wait up to 500 ms for the CvP status register bit assertion.



VSEC Registers for CvP

The Vendor Specific Extended Capability (VSEC) registers occupy byte offset 0x200 to 0x240 in the PCIe Configuration Space. The PCIe host uses these registers to communicate with the FPGA control block. The

following table shows the VSEC register map. Subsequent tables provide the fields and descriptions of each register.

Table 4-1: VSEC Registers for CvP

Byte Offset	Register Name
0x200	Altera-defined Vendor Specific Capability Header
0x204	Altera-defined Vendor Specific Header
0x208	Altera Marker
0x20C:0x218	Reserved
0x21C	CvP Status
0x220	CvP Mode Control
0x224	CvP Data 2
0x228	CvP Data
0x22C	CvP Programming Control
0x230	Reserved
0x234	Uncorrectable Internal Error Status Register
0x238	Uncorrectable Internal Error Mask Register
0x23C	Correctable Internal Error Status Register
0x240	Correctable Internal Error Mask Register

Altera-defined Vendor Specific Capability Header Register

Table 4-2: Altera-defined Vendor Specific Capability Header Register (Byte Offset: 0x200)

Bits	Name	Reset Value	Access	Description
[15:0]	PCI Express Extended Capability ID	0x000B	RO	PCIe specification defined value for VSEC Capability ID.
[19:16]	Version	0x1	RO	PCIe specification defined value for VSEC version.
[31:20]	Next Capability Offset	Variable	RO	Starting address of the next Capability Structure implemented, if any.

Altera-defined Vendor Specific Header Register

Table 4-3: Altera-defined Vendor Specific Header Register (Byte Offset: 0x204)

Bits	Name	Reset Value	Access	Description
[15:0]	VSEC ID	0x1172	RO	A user configurable VSEC ID.
[19:16]	VSEC Revision	0	RO	A user configurable VSEC revision.
[31:20]	VSEC Length	0x044	RO	Total length of this structure in bytes.

Altera Marker Register

Table 4-4: Altera Marker Register (Byte Offset: 0x208)

Bits	Name	Reset Value	Access	Description
[31:0]	Altera Marker	Device Value	RO	An additional marker. If you use the standard Altera Programmer software to configure the device with CvP, this marker provides a value that the programming software reads to ensure that it is operating with the correct VSEC.

CvP Status Register

Table 4-5: CvP Status Register (Byte Offset: 0x21C)

Bits	Name	Reset Value	Access	Description
[31:26]	—	0x00	RO	Reserved.
[25]	PLD_CORE_READY	Variable	RO	From FPGA fabric. This status bit is provided for debug.
[24]	PLD_CLK_IN_USE	Variable	RO	From clock switch module to fabric. This status bit is provided for debug.
[23]	CVP_CONFIG_DONE	Variable	RO	Indicates that the FPGA control block has completed the device configuration via CvP and there were no errors.
[22]	—	Variable	RO	Reserved.
[21]	USERMODE	Variable	RO	Indicates if the configurable FPGA fabric is in user mode.
[20]	CVP_EN	Variable	RO	Indicates if the FPGA control block has enabled CvP mode.

Bits	Name	Reset Value	Access	Description
[19]	CVP_CONFIG_ERROR	Variable	RO	Reflects the value of this signal from the FPGA control block, checked by software to determine if there was an error during configuration.
[18]	CVP_CONFIG_READY	Variable	RO	Reflects the value of this signal from the FPGA control block, checked by software during programming algorithm.
[17:0]	—	Variable	RO	Reserved.

CvP Mode Control Register

Table 4-6: CvP Mode Control Register (Byte Offset: 0x220)

Bits	Name	Reset Value	Access	Description
[31:16]	—	0x0000	RO	Reserved.
[15:8]	CVP_NUMCLKS	0x00	RW	<p>This is the number of clocks to send for every CvP data write. This is also known as CDRATIO (clock to data ratio).</p> <p>Set this field to one of the values below depending on your configuration image:</p> <ul style="list-style-type: none"> • 0x01 for uncompressed and unencrypted images • 0x04 for uncompressed and encrypted images • 0x08 for all compressed images
[7:3]	—	0x0	RO	Reserved.
[2]	CVP_FULLCONFIG	1'b0	RW	A value of 1 indicates a request to the control block to reconfigure the entire FPGA including the Hard IP for PCI Express and bring the PCIe link down.

Bits	Name	Reset Value	Access	Description
[1]	HIP_CLK_SEL	1'b0	RW	<p>Selects between PMA and fabric clock when USER_MODE = 1 and PLD_CORE_READY = 1. The following encodings are defined:</p> <ul style="list-style-type: none"> 1: Selects internal clock from PMA which is required for CVP_MODE. 0: Selects the clock from soft logic fabric. This setting should only be used when the fabric is configured in USER_MODE with a configuration file that connects the correct clock. <p>To ensure that there is no clock switching during CvP, you should only change this value when the Hard IP for PCI Express has been idle for 10 μs and wait 10 μs after changing this value before resuming activity.</p>
[0]	CVP_MODE	1'b0	RW	<p>Controls whether the Hard IP for PCI Express is in CVP_MODE or normal mode. The following encodings are defined:</p> <ul style="list-style-type: none"> 1: CVP_MODE is active. Signals to the FPGA control block active and all TLPs are routed to the Configuration Space. This CVP_MODE cannot be enabled if CVP_EN = 0. 0: The IP core is in normal mode and TLPs are route to the FPGA fabric.

CvP Data Registers

Table 4-7: CvP Data Register (Byte Offsets: 0x224 - 0x228)

Bits	Name	Reset Value	Access	Description
[31:0]	CVP_DATA2	0x00000000	RW	Contains the upper 32 bits of a 64-bit configuration data. Software must ensure that all Bytes in both dwords are enabled. Use of 64-bit configuration data is optional.
[31:0]	CVP_DATA	0x00000000	RW	<p>Write the configuration data to this register. The data is transferred to the FPGA control block to configure the device.</p> <p>Every write to this register sets the data output to the FPGA control block and generates $\langle n \rangle$ clock cycles to the FPGA control block as specified by the CVP_NUM_CLKS field in the CvP Mode Control register. Software must ensure that all bytes in the memory write dword are enabled.</p> <p>You can access this register using configuration writes. Alternatively, when in CvP mode, this register can also be written by a memory write to any address defined by a memory space BAR for this device. Using memory writes are higher throughput than configuration writes.</p>

CvP Programming Control Register

Table 4-8: CvP Programming Control Register (Byte Offset: 0x22C)

Bits	Name	Reset Value	Access	Description
[31:2]	—	0x0000	RO	Reserved.
[1]	START_XFER	1'b0	RW	Sets the CvP output to the FPGA control block indicating the start of a transfer.
[0]	CVP_CONFIG	1'b0	RW	When set to 1, the FPGA control block begins a transfer via CvP.

Uncorrectable Internal Error Status Register

This register reports the status of the internally checked errors that are uncorrectable. When specific errors are enabled by the `Uncorrectable Internal Error Mask` register, they are handled as Uncorrectable Internal Errors as defined in the *PCI Express Base Specification 3.0*. This register is for debug only. Use this register to observe behavior, not to drive custom logic.

Table 4-9: Uncorrectable Internal Error Status Register (Byte Offset: 0x234)

Bits	Reset Value	Access	Description
[31:12]	0x00	RO	Reserved.
[11]	1'b0	RW1CS	A value of 1 indicates an RX buffer overflow condition in a posted request or Completion segment.
[10]	1'b0	RW1CS	A value of 1 indicates a parity error was detected on the R2CSEB interface.
[9]	1'b0	RW1CS	A value of 1 indicates a parity error was detected on the Configuration Space to TX bus interface.
[8]	1'b0	RW1CS	A value of 1 indicates a parity error was detected on the TX to Configuration Space bus interface.
[7]	1'b0	RW1CS	A value of 1 indicates a parity error was detected in a TX TLP and the TLP is not sent.
[6]	1'b0	RW1CS	A value of 1 indicates that the Application Layer has detected an uncorrectable internal error.
[5]	1'b0	RW1CS	A value of 1 indicates a configuration error has been detected in CvP mode which is reported as uncorrectable. This <code>CVP_CONFIG_ERROR_LATCHED</code> bit is set whenever a <code>CVP_CONFIG_ERROR</code> is asserted while in <code>CVP_MODE</code> .
[4]	1'b0	RW1CS	A value of 1 indicates a parity error was detected by the TX Data Link Layer.
[3]	1'b0	RW1CS	A value of 1 indicates a parity error has been detected on the RX to Configuration Space bus interface.
[2]	1'b0	RW1CS	A value of 1 indicates a parity error was detected at input to the RX Buffer.
[1]	1'b0	RW1CS	A value of 1 indicates a retry buffer uncorrectable ECC error.
[0]	1'b0	RW1CS	A value of 1 indicates a RX buffer uncorrectable ECC error.

Uncorrectable Internal Error Mask Register

This register controls which errors are forwarded as internal uncorrectable errors. With the exception of the configuration errors detected in CvP mode, all of the errors are severe and may place the device or PCIe link in an inconsistent state. The configuration error detected in CvP mode may be correctable depending on the design of the programming software.

Table 4-10: Uncorrectable Internal Error Mask Register (Byte Offset: 0x238)

Bits	Reset Value	Access	Description
[31:12]	0x00	RO	Reserved.
[11]	1'b1	RWS	Mask for RX buffer posted and completion overflow error.
[10]	1'b1	RWS	Mask for parity error on the R2CSEB interface.
[9]	1'b1	RWS	Mask for parity error on the Configuration Space to TX bus interface.
[8]	1'b1	RWS	Mask for parity error on the TX to Configuration Space bus interface.
[7]	1'b1	RWS	Mask for parity error in the transaction layer packet.
[6]	1'b1	RWS	Mask for parity error in the application layer.
[5]	1'b0	RWS	Mask for configuration error in CvP mode.
[4]	1'b1	RWS	Mask for data parity errors detected during TX Data Link LCRC generation.
[3]	1'b1	RWS	Mask for data parity errors detected on the RX to Configuration Space Bus interface.
[2]	1'b1	RWS	Mask for data parity error detected at the input to the RX Buffer.
[1]	1'b1	RWS	Mask for the retry buffer uncorrectable ECC error.
[0]	1'b1	RWS	Mask for the RX buffer uncorrectable ECC error.

Correctable Internal Error Status Register

This register reports the status of the internally checked errors that are correctable. When these specific errors are enabled by the `Correctable Internal Error Mask` register, they are forwarded as `Correctable Internal Errors` as defined in the *PCI Express Base Specification 3.0*. This register is for debug only. Use this register to observe behavior, not to drive custom logic.

Table 4-11: Correctable Internal Error Status Register (Byte Offset: 0x23C)

Bits	Reset Value	Access	Description
[31:7]	0x000	RO	Reserved.

Bits	Reset Value	Access	Description
[6]	1'b0	RW1CS	A value of 1 indicates that the Application Layer has detected a correctable internal error.
[5]	1'b0	RW1CS	A value of 1 indicates a configuration error has been detected in CvP mode, which is reported as correctable. This bit is set whenever a CVP_CONFIG_ERROR occurs while in CVP_MODE.
[4:2]	0x0	RO	Reserved.
[1]	1'b0	RW1CS	A value of 1 indicates a retry buffer correctable ECC error.
[0]	1'b0	RW1CS	A value of 1 indicates an RX buffer correctable ECC error.

Correctable Internal Error Mask Register

This register controls which errors are forwarded as Internal Correctable Errors. This register is for debug only.

Table 4-12: Correctable Internal Error Mask Register (Byte Offset: 0x240)

Bits	Reset Value	Access	Description
[31:7]	0x000	RO	Reserved.
[6]	1'b0	RWS	Mask for corrected internal error reported by the Application Layer.
[5]	1'b0	RWS	Mask for configuration error detected in CvP mode.
[4:2]	0x0	RO	Reserved.
[1]	1'b0	RWS	Mask for retry buffer correctable ECC error.
[0]	1'b0	RWS	Mask for RX buffer correctable ECC error.

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Partial reconfiguration (PR) is an advanced feature which allows you to reconfigure a portion of the FPGA design's core logic dynamically, whilst the remainder of the FPGA device continues to operate. Partial reconfiguration is supported in Cyclone V⁽¹⁾, Stratix V, and Arria 10 device families. Partial Reconfiguration over Protocol offers a solution for configuring the FPGA fabric through the PCI Express (PCIe) link.

Note: For Arria 10 devices, you need the Quartus Prime Pro Edition software to utilize the advanced features like partial reconfiguration.

Related Information

- [Introduction to Altera IP Cores](#)

Provides general information about all Altera IP cores, including parameterizing, generating, upgrading, and simulating IP.

- [Project Management Best Practices](#)

Guidelines for efficient management and portability of your project and IP files.

- [Creating a Partial Reconfiguration Design](#)

Provides more information about the Partial Reconfiguration methodology and utilization.

Benefits of Using PR over PCI Express

The PR over PCI Express solution has the following advantages:

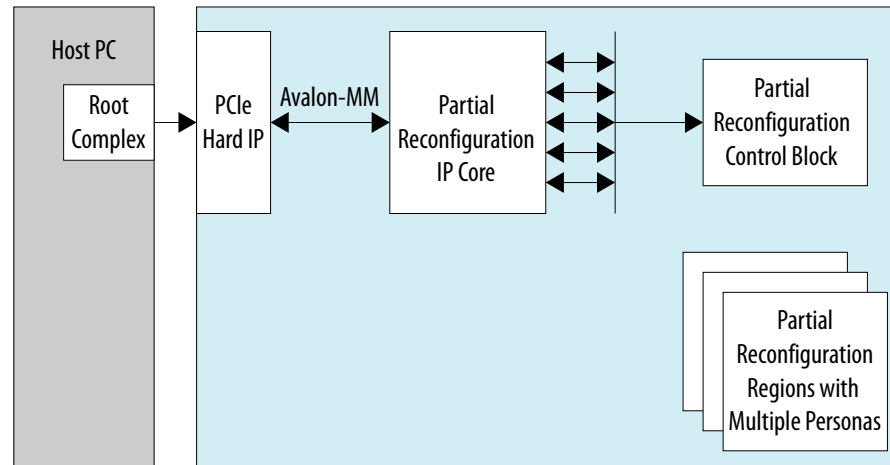
- Enables dynamic updates to portions of the FPGA design's core such as LAB, MLAB, DSP and RAM while the rest of the design continues to run.
- Facilitates hardware acceleration.
- Design protection: PR over PCIe ensures the PCIe host can exclusively access the FPGA fabric image which provides protection against unauthorized design tampering or copying.
- Image update without system down time: Allows a portion of the FPGA fabric to be updated through the PCIe link without a host reboot or FPGA full chip re-initialization.
- Unlike Configuration via Protocol (CvP) which requires the bottom left PCIe Hard IP block be used, any Hard IP for PCI Express IP Core can be used for PR over PCIe. The Hard IP Core must be configured as an Endpoint.

⁽¹⁾ The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in their part number.

PR over PCIe System

This is a generic design organization for any PR over PCIe design.

Figure 5-1: Block Diagram of PR over PCIe AVMM Design



As shown in the diagram, a PCIe card with Altera FPGA plugged in a host PC. The host PC sends the PR bit-stream to the Hard IP for PCIe in the form of packets using the application software. The packets are then received by the PR IP core through Avalon MM slave interface. The PR IP core acts as the master to the hard PR control block. It controls the flow of control and data bits to the PR control block as well as sends back the status from the PR control block to the host PC through the PCIe endpoint.

Related Information

Partial Reconfiguration Concepts

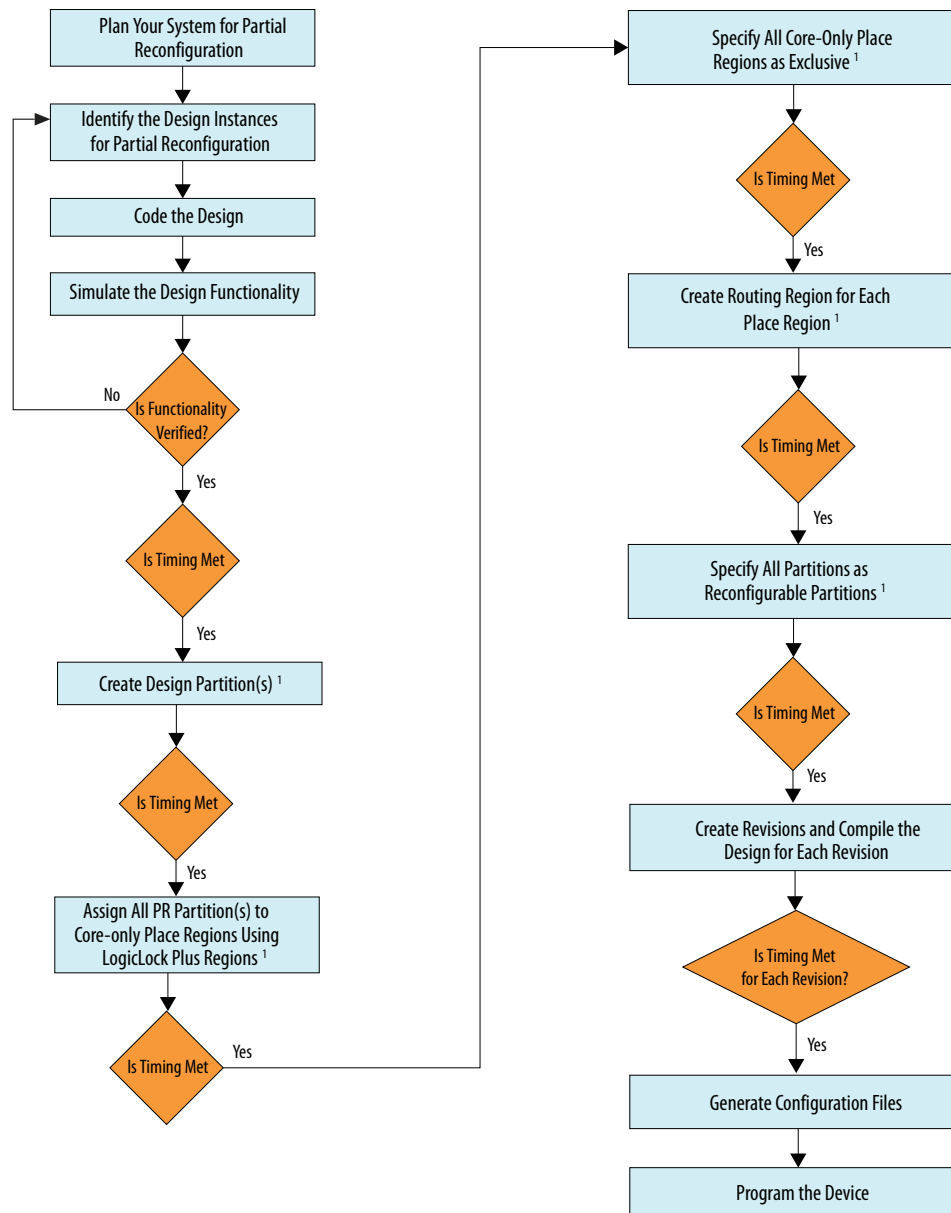
Provides more information about the commonly-used partial reconfiguration terminology.

Partial Reconfiguration Design Flow

The PR design flow requires initial planning. This planning involves setting up the design partition(s), and determining the placement assignments in the floorplan. Well-planned PR partitions improve design area utilization and performance. Your design can include the PR control block, which involves implementing the internal or external PR host.

The PR design flow uses the project revisions feature in the Quartus Prime software. Your initial design is the base revision, where you define the static region boundaries and reconfigurable regions on the FPGA. From the base revision, you create multiple revisions. These revisions contain the different implementations for the PR regions. However, all PR implementation revisions use the same top-level placement and routing results from the base revision.

Figure 5-2: Partial Reconfiguration Design Flow



(1) Recommended to compile the base revision before verifying timing closure

Related Information

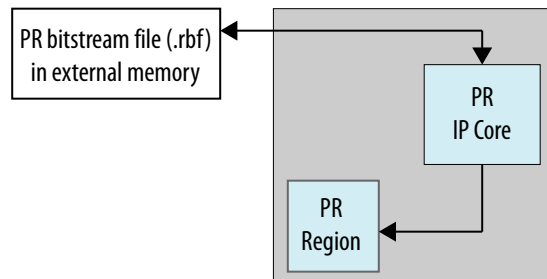
Compile the Partial Reconfiguration Design

Provides more information about the PR compilation flow for Arria 10 Devices.

Partial Reconfiguration IP Core

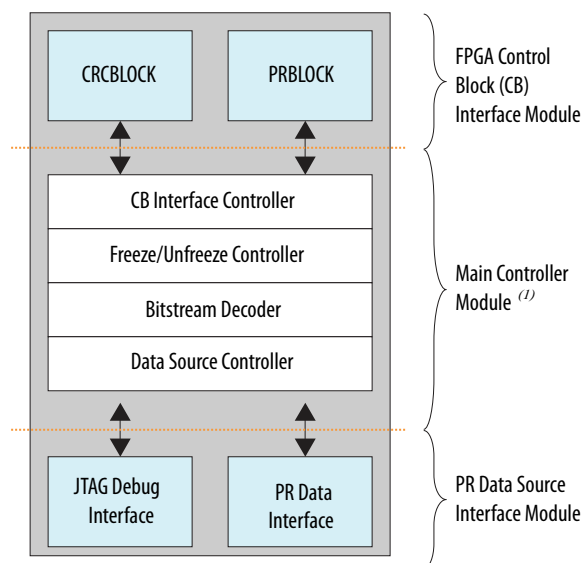
PR over PCIe is performed using the PR IP core as an internal host residing in the core logic, which will automatically instantiate the corresponding `crcblock` and `prblock` WYSIWYG atom primitives.

Figure 5-3: PR IP Core as an Internal Host



During partial reconfiguration, the PR Control Block (CB) is in Passive Parallel x16 or x32 programming mode.

Figure 5-4: PR IP Core Components



Note:

1. The main controller module handles all the handshaking signals of the CB interface and processes the incoming data, as needed, before sending to the PRBLOCK. It also handles the freeze/un-freeze PR interface.

When you instantiate the PR IP core, the Main Controller module which includes the Control Block Interface Controller, Freeze/Unfreeze Controller, and the Data Source Controller are all instantiated. A Data Source Interface module provides you with a JTAG Debug Interface and PR Data Interface.

Related Information

- **[Partial Reconfiguration IP Core User Guide](#)**
Provides more information about the PR IP Core and how to instantiate it.
- **[Instantiate Partial Reconfiguration Control Block in the Design](#)**
Provides more information about the PR IP core instantiation using the Quartus Prime software.

Understanding Design Steps for PR over PCI Express in Arria 10

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Partial reconfiguration is based on the use of revisions in the Quartus Prime Pro edition software. Your initial design is the base revision, where you define the boundaries of the static region and reconfigurable regions on the FPGA. From the base revision, you create multiple revisions, which contain the static region and describe the differences in the reconfigurable regions.

The PR design flow requires more initial planning than a standard design flow. Planning requires setting up the design logic for partitioning, and determining placement assignments to create a floorplan. You should have well-planned partitions to improve the design area utilization and performance, and make timing closure easier.

Refer to the following application notes that provides a comprehensive walkthrough using the dedicated reference designs:

- [AN784: Partial Reconfiguration over Protocol Reference Design for Arria 10 Devices](#)
- [AN770: Partially Reconfiguring a Design on Arria 10 SoC Development Board](#)

You can extend these reference designs to meet your requirements, then run your custom design on the fully functional system that enables communication over PCIe.

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Document Revision History

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Table A-1: Document Revision History

Date	Changes
2016.10.31	<ul style="list-style-type: none"> Changed the document title from 'Arria CvP Initialization and Partial Reconfiguration via Protocol User Guide' to 'Arria CvP Initialization and Partial Reconfiguration over PCI Express User Guide'. Removed the topic <i>Autonomous Mode</i>, instead refer to the <i>Arria 10 Avalon-MM/ST Interface for PCIe Solutions User Guide</i>. Added the pin descriptions for <code>INIT_DONE</code> and <code>CONF_DONE</code>. Corrected the <i>PCIe Timing Sequence</i> diagram for CvP initialization. Added the timeout value for <code>CvP_CONFIG_READY</code> in the Figure: <i>CvP Driver Flow</i>. Added the topic <i>Partial Reconfiguration Design Flow</i> to the Chapter: <i>Partial Reconfiguration over Protocol in Arria 10</i>. Removed the <i>Design Planning for PR over PCI Express in Arria 10</i> chapter. Instead refer to Creating a Partial Reconfiguration Design. Removed the following topics from Chapter: <i>Understanding Design Steps for PR over PCI Express in Arria 10</i>: <ul style="list-style-type: none"> Creating a Qsys design Creating User Logic and Top Level File Creating PR Partition Generating Base SOF/RBF Bitstreams Creating PR Revision Generating PR Bitstreams Bringing Up the Hardware Fixed assorted typos and formatting issues.
2016.05.02	Initial release

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