Partial reconfiguration (PR) offers you the ability to reconfigure part of the design's core logic such as LABs, MLABs, DSP, and RAM, while the remainder of the design continues running. The PR IP core provides a standard interface to this ability and eliminates the need to manually instantiate an interface with the PR control block. You can instantiate the PR IP core through Qsys or Qsys Pro, or via the Quartus® Prime IP Catalog. The Quartus Prime Standard Edition software supports the PR IP Core for the Stratix® V device family and Cyclone® V devices whose part number ends in "SC", for example, 5CGXFC9E6F35I8NSC.

You can perform partial reconfiguration through either an internal host residing in the core logic, or as an external host via dedicated device pins. The advantage of the internal host is that you store all the logic needed to perform PR on the device, without the need for external devices.

Figure 1: PR IP Core Components
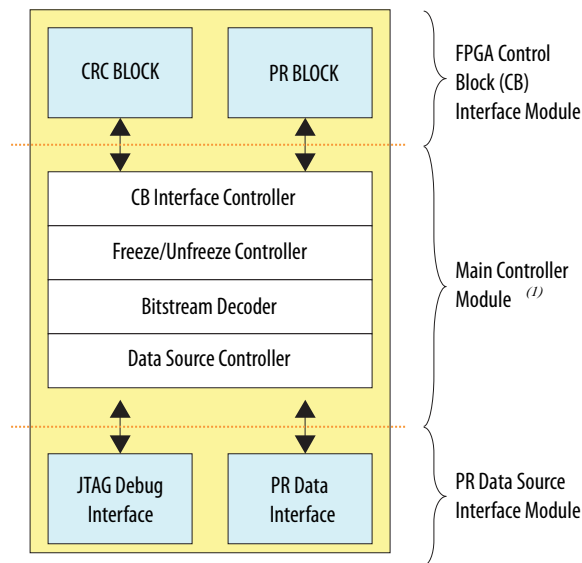
Note:

1. The main controller module handles all the handshaking signals of the CB interface and processes the incoming data, as needed, before sending to PRBLOCK. It also handles the freeze/un-freeze PR interface.

When you instantiate the PR IP core, the Main Controller module is instantiated. This module includes the Control Block (CB) Interface Controller, Freeze/Unfreeze Controller, Bitstream Decoder, and the Data Source Controller. A Data Source Interface module provides you with an optional JTAG Debug Interface

and PR Data Interface. If you choose to use the PR IP core in internal host mode, the IP core automatically instantiates the corresponding `crcblock` and `prblock` WYSIWYG atom primitives.

If used as external host (placed in another FPGA or CPLD), the PR IP core provides the required interface ports. Connect to the dedicated PR pins and `CRC_ERROR` pin on the target FPGA undergoing partial reconfiguration.

Figure 2: Managing Partial Reconfiguration with an Internal or External Host

Internal Host   **External Host**
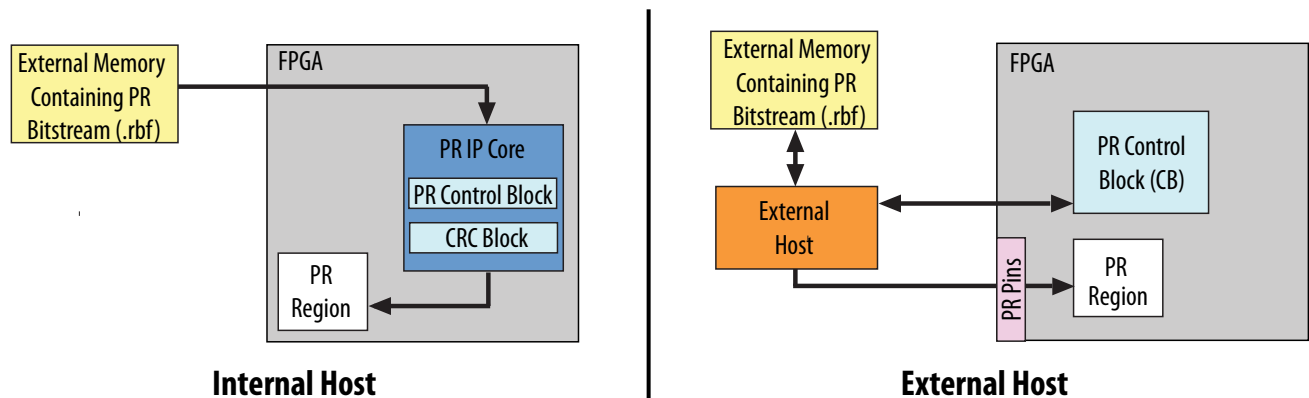
The figure shows how to connect these blocks to the PR control block (CB). In your system, you include either the external host or the internal host, but not both. During PR, the PR Control Block (CB) is in Passive Parallel x16 programming mode for 28nm devices. In external host mode, the PR control block is not instantiated in the core of the device undergoing PR, because there is a direct connection from the external PR pins to the internal control block.

You can instantiate the PR IP core as the internal host for all supported devices. When you specify it as the internal host, both `prblock` and `crcblock` WYSIWYG atom primitives are auto-instantiated as part of the design. You can instantiate the PR IP core as the external host on any supported devices, as specified in the device family list.

Related Information

- **FPGA Control Block Interface** on page 19
- **Data Source Controller** on page 22
- **Standard Partial Reconfiguration Data Interface** on page 22
- **JTAG Debug Mode for Partial Reconfiguration** on page 22

Instantiating the Partial Reconfiguration IP Core in the Qsys Interface

Partial Reconfiguration (PR) is available as a Qsys or Qsys Pro component through the Qsys interface. Instantiate the core as an internal host or an external host.

You can configure the PR IP core to use **Avalon-Streaming** and **Conduit** interfaces, or an **Avalon-MM** interface. Enable the **Avalon-MM** interface using the **Enable Avalon-MM Slave Interface** option. If you use Qsys and want PR included as a component, for example in a design with both Qsys and non-Qsyspartitions, you must instantiate the PR IP core in the Qsys interface.

To instantiate the PR IP core with Qsys:

1. Click **Tools** > **Qsys**.
2. In the **Qsys** interface **IP Catalog**, click **Basic Functions** > **Configuration and Programming** and select **Partial Reconfiguration**.
3. Configure your IP core variation using the settings appropriate to your design.

Figure 3: Partial Reconfiguration IP Core in the Qsys Interface

4. Optionally, turn on **Enable Avalon-MM slave interface** to use the Avalon Memory Map Slave interface rather than the Conduit interface.
5. Turn on **Enable enhanced decompression** to use this optional feature.
6. Select an appropriate clock-to-data ratio for your other options.
7. Click **Finish**.

Related Information

- **Enable Enhanced Decompression** on page 7
  For more information on the enhanced decompression feature.
- **Clock-to-Data Ratio (CD Ratio)** on page 9
- **Partial Reconfiguration IP Core Parameters** on page 10
- **Creating a System With Qsys**

Instantiating the Partial Reconfiguration IP Core in the Quartus Prime IP Catalog

Partial Reconfiguration (PR) is available from the **IP Catalog**. You can choose to instantiate the core as an internal host or an external host.

If you are not using PR as a component of the **Qsys** interface, then you can instantiate PR with the Quartus Prime IP Catalog.

1. Click **Tools** > **IP Catalog**.
2. Click **Installed IP** > **Library** > **Basic Functions** > **Configuration and Programming** and select **Partial Reconfiguration**.
3. In the **Save IP Variation** dialog box, type the name for your partial reconfiguration IP variation. Choose whether to use Verilog or VHDL. Click **OK** to save your variation.
4. Configure your IP core variation using the settings appropriate to your design.

Figure 4: Partial Reconfiguration IP Core in the IP Catalog

5. Optionally, turn on **Enable Avalon-MM slave interface** to use the Avalon Memory Map Slave interface rather than the Conduit interface.
6. Turn on **Enable enhanced decompression** to use this optional feature.

7. Select an appropriate clock-to-data ratio for your other options.
8. Click **Finish**.

   The IP Catalog instantiates your IP core variation and displays a completion dialog box.
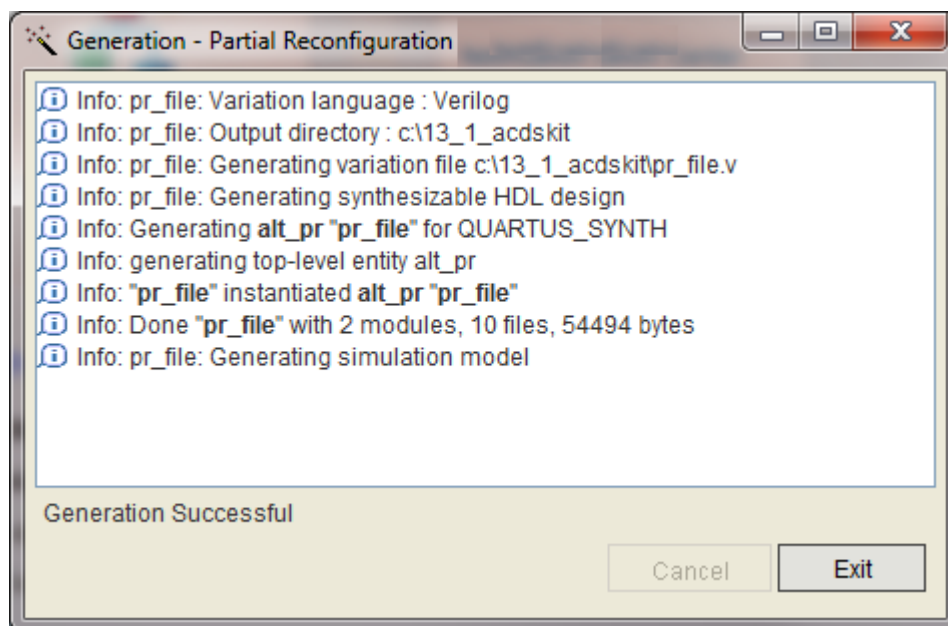
9. Click **Exit**.

Related Information

- **Enable Enhanced Decompression** on page 7

  For more information on the enhanced decompression feature.
- **Clock-to-Data Ratio (CD Ratio)** on page 9
- **Partial Reconfiguration IP Core Parameters** on page 10

Enable Compression

You can enable bitstream compression (and decompression) to reduce the size of your bitstream by specifying options during programming.

Note: The terms "standard" and "enhanced" compression only apply when using PR. Enhanced compression is only available when using the PR IP Core with supported device families.

Related Information

- **Enable Enhanced Decompression** on page 7
- **Generate PR Bitstreams**

  For more information about enabling compression duiring programming refer to the Quartus Prime Handbook.
- **Data Compression Comparison** on page 8

  For more information on comparing compression rates.
- **Clock-to-Data Ratio (CD Ratio)** on page 9

PR Bitstream Compression and Encryption

You can compress and encrypt the base bitstream and the PR bitstream for your PR project using options available in the Quartus Prime software.

Compress the base and PR programming bitstreams independently, based on your design requirements. When encrypting only the base image, specify whether or not to encrypt the PR images. The following guidelines apply to PR bitstream compression and encryption:

- You can encrypt the PR images only when the base image is encrypted.
- The Encryption Key Programming (.ekp) file generates when encrypting the base image and must be used for encrypting the PR bitstream.
- When you compress the bitstream, present each PR_DATA[15:0] word for exactly four clock cycles.

For partial reconfiguration with the PR Controller IP core, specify enhanced compression by turning on the **Enhanced compression** option when specifying the parameters in the **IP Catalog** or Qsys Pro parameter editors.

Note: You cannot use encryption with enhanced compression simultaneously.

Table 1: Partial Reconfiguration Clock Requirements for Bitstream Compression

Timing Parameters	Value (clock cycles)
PR_READY to first data	4 (exact)
PR_ERROR to last clock	80 (minimum)
PR_DONE to last clock	80 (minimum)
DONE_to_REQ_low	8 (maximum)

Generating an Encrypted PR Bitstream

To partially reconfigure your device with encrypted bitstream:

1. Create a 256-bit key file (.key).
2. To generate the key programming file (.ekp) from the Quartus Prime shell, type the following command:

   ```
   quartus_cpf --key <keyfile>:<keyid> <base_sof_file> <output_ekp_file>
   ```

   For example:

   ```
   quartus_cpf --key my_key.key:key1 base.sof key.ekp
   ```

3. To generate the encrypted PR bitstream (.rbf), run the following command:

   ```
   quartus_cpf -c <pr_pmsf_file> <pr_rbf_file>
   qcrypt -e --keyfile=<keyfile> --keyname=<keyid> -lockto=<qlk file> --
   keystore=<battery|OTP> <pr_rbf_file> <pr_encrypted_rbf_file>
   ```

   - lockto—specifies the encryption lock.
   - keystore—specifies the volatile key (battery) or the non-volatile key (OTP).

For example:

```
quartus_cpf -c top_v1.pr_region.pmsf top_v1.pr_region.rbf
qcrypt -e --keyfile=my_key.key --keyname=key1 --keystore=battery
top_v1.pr_region.rbf top_v1_encrypted.rbf
```

4. To program the key file as volatile key (default) into the device, type the following command:

```
quartus_pgm -m jtag -o P;<output_ekp_file>
```

For example:

```
quartus_pgm -m jtag -o P;key.ekp
```

5. To program the base image into the device, type the following command:

```
quartus_pgm -m jtag -o P;<base_sof_file>
```

For example:

```
quartus_pgm -m jtag -o P;base.sof
```

6. To partially reconfigure the device with the encrypted bitstream, type the following command:

```
quartus_pgm -m jtag --pr <output_encrypted_rbf_file>
```

For example:

```
quartus_pgm -m jtag --pr top_v1_encrypted.rbf
```

Related Information
Using the Design Security Features in Altera FPGAs

Enable Enhanced Decompression

Enhanced compression (and decompression) can reduce the size of your bitstream at the expense of greater resources use.

Important: Do not use enhanced compression with bitstream encryption.

Enhanced compression is available for Stratix V devices. Additionally, you can also use enhanced compression with double-compression.

You can generate a bitstream with enhanced compression in one of two ways:

- In the **Convert Programming Files** dialog box under the properties of a Partial-Masked SRAM Object File (.pmsf)
- From the command line with this command:

```
quartus_cpf -c -o enhanced_bitstream_compression=on <input_filename>.pmsf
<output_filename>.rbf
```

Note: Enhanced compression uses the same CD Ratio setting as a plain, uncompressed bitstream.

Related Information

- **Instantiating the Partial Reconfiguration IP Core in the Quartus Prime IP Catalog** on page 4

Data Compression Comparison

Standard compression results in a 30-45% decrease in RBF size. Use of the enhanced data compression algorithm results in 55-75% decrease in RBF size. The algorithm increases the compression at the expense of additional core area required to implement the compression algorithm.

The following figure shows the compression ratio comparison across PR designs with varying degrees of Logic Element (LE):

Figure 5: Compression Ratio Comparison between Standard Compression and Enhanced Compression
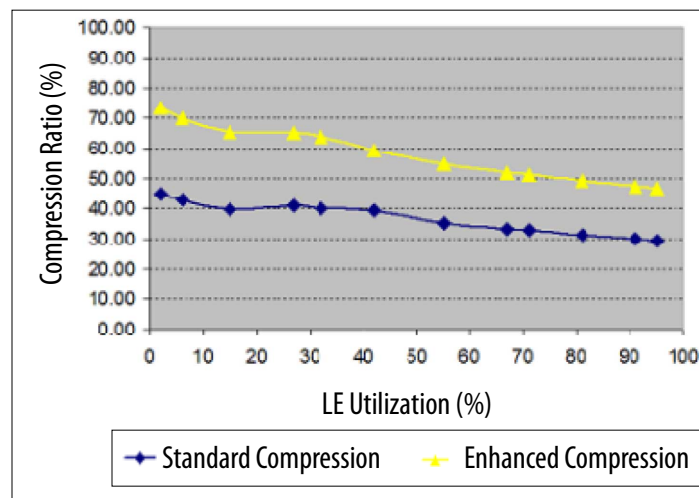
Related Information

- **Enable Enhanced Decompression** on page 7
- **Enable Compression** on page 5
- **Clock-to-Data Ratio (CD Ratio)** on page 9
- **Partial Reconfiguration Solutions IP User Guide**
  For more information about using Partial Reconfiguration in Quartus Prime Pro refer to the Partial Reconfiguration Solutions IP User Guide.

Bitstream Compatibility Check

Turn on the **Enable bitstream compatibility check** when instantiating the PR Controller IP core from either Qsys Pro or the IP Catalog for supported devices. The software then verifies the partial reconfiguration PR Bitstream file (`.rbf`). If an incompatible bitstream is detected, the PR operation aborts and the `status` output reports an error. The PR `.pof` ID encodes as the 71st word of the PR bitstream.

Figure 6: Bitstream Compatibility Check
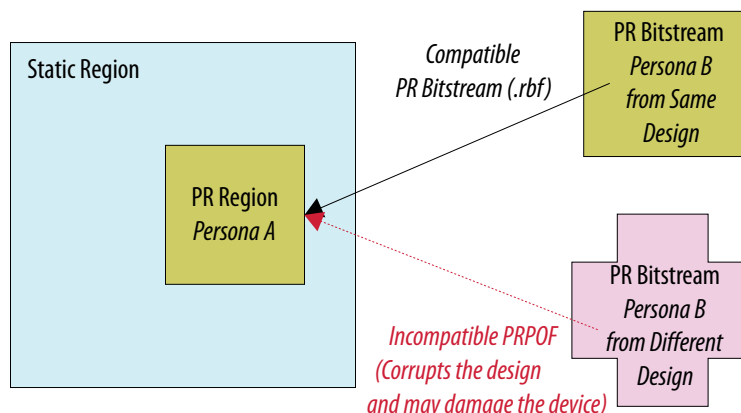
This option prevents you from accidentally corrupting the static region of your design with a bitstream from an incompatible `.rbf` and risking damage to the chip you are programming.

When you turn on **Enable bitstream compatibility check**, the PR Controller IP core creates a **PR bitstream ID** and displays the bitstream ID in the configuration dialog box.

Related Information

- **Data Compression Comparison** on page 8
  For more information on specifying PR IP Core Parameters
- **Partial Reconfiguration IP Core Parameters** on page 10
- **Partial Reconfiguration IP Core Ports** on page 12

Clock-to-Data Ratio (CD Ratio)

The proper clock-to-data ratio (CD Ratio) is critical for partial reconfiguration. A proper CD Ratio ensures that the data being processed synchronizes during the PR operation whether you are using compression, encryption, or both, or neither.

The Control Block (CB) interface receives data and sends it during a PR event with the CD Ratio you specify when you instantiate the Partial Reconfiguration IP core.

Table 2: Valid combinations and CD Ratio for Bitstream Encryption and Compression for Stratix V Devices

Compressed	Encrypted	CD Ratio
Off	Off	1

Compressed	Encrypted	CD Ratio
Off	On	2
On	Off	4
On	On	4

CD Ratio for the PR IP core in Stratix V designs must be exact for the bitstream type. CD Ratio for plain Programmer Object File (POF) must be 1. CD Ratio for compressed POF must be 2, 4 or 8, depending on the width. Do not specify the CD Ratio as the necessary minimum to support different bitstream types.

Note: Standard encryption uses the same CD Ratio setting as a plain, uncompressed bitstream.

Related Information

- **Instantiating the Partial Reconfiguration IP Core in the Quartus Prime IP Catalog** on page 4
  For more information on PR IP core instantiation in Qsys.
- **Instantiating the Partial Reconfiguration IP Core in the Qsys Interface** on page 2
  For more information on PR IP core instantiation in the IP Catalog.

Partial Reconfiguration IP Core Parameters

IP Core Option	Value	Default	Description
Use as PR internal host	On or Off	On	Turn on this option to use the PR IP core as an internal host. Both `prblock` and `crcblock` WYSIWYG atom primitives are auto-instantiated as part of your design. Disable this option to use the PR IP core as an external host in an external device. You must connect additional interface signals to the dedicated PR pins if you use the PR IP core as an external host.
Enable JTAG debug mode	On or Off	On	To perform partial reconfiguration turn on this option to access the PR IP core with the Programmer.
Enable Avalon-MM slave interface	On or Off	Off	Turn on this option to use the Avalon Memory-Mapped (Avalon-MM) slave interface.
Enable interrupt interface	On or Off	Off	Enable this option to use the interrupt interface. You can only enable this interface if you turned on the Enable Avalon-MM slave interface parameter.

IP Core Option	Value	Default	Description
Enable bitstream compatibility check	On or Off	Off	Turn on this option to check the bitstream compatibility during PR operations for external host. The bitstream compatibility check feature is always enabled for PR internal host. Specify the PR bitstream ID value if you enable this option for PR external host.
PR bitstream ID	-2147483648 to 2147483647	0	Specifies a signed 32-bit integer value of the PR bitstream ID for external host. This value must match the PR bitstream ID generated during compilation for the target PR design. You can find the PR bitstream ID value of the target PR design in the Assembler compilation report (`.asm.rpt`).
Input data width	1, 8, 16, or 32	16	Specifies the data width in bits. This option affects the `data[]` bus width.
Target device familiy for partial reconfiguration	Cyclone V, Stratix V	"Stratix V"	Select the target device family for partial reconfiguration when you use the PR IP core as external host. **Note:** This option is ignored for PR internal host.
Clock-to-Data ratio	Cyclone V or Stratix V:1, 2, or 4	1	Specifies the ratio between PR clock and PR data.
Divide error detection frequency by	1, 2, 4, 8, 16, 32, 64, 128, or 256	1	Only available when you use the IP core as an internal host. The `crcblock` WYSIWYG atom primitive is auto-instantiated as part of the design. Specifies the divide value of the internal clock, which determines the frequency of the error detection cyclic redundancy check (CRC). The divide value must be a power of two. Refer to the device handbook to find the frequency of the internal clock for the selected device.
Auto-instantiate CRC block	On or Off	On	This option is only applicable for an internal host. Disable this option to manually instantiate a CRC block.
Auto-instantiate PR block	On or Off	On	This option is only applicable for an internal host. Disable this option to manually instantiate a PR block.

IP Core Option	Value	Default	Description
Enable enhanced decompression	On or Off	Off	Enable this option is to use the enhanced decompressor. Decompress bitstreams that are compressed with the enhanced compression algorithm.

Related Information

- **Instantiating the Partial Reconfiguration IP Core in the Quartus Prime IP Catalog** on page 4
  For more information on PR IP core instantiation in Qsys.
- **Instantiating the Partial Reconfiguration IP Core in the Qsys Interface** on page 2
  For more information on PR IP core instantiation in the IP Catalog.
- **Avalon-MM Interface Partial Reconfiguration Sequence** on page 17
- **Avalon-MM Slave Interface Read and Write Transfer Timing** on page 20
  For more information on the timing specification for the Avalon Memory Mapped Slave interface.
- **Clock-to-Data Ratio (CD Ratio)** on page 9

Partial Reconfiguration IP Core Ports

I/O Port List for PR IP Core

Table 3: Clock/Reset Ports

Port Name	Width	Direction	Function
nreset	**1**	Input	Asynchronous reset for the PR IP core. Resetting the PR IP core during a partial reconfiguration operation can cause the device to lock up.
clk	**1**	Input	User input clock to the PR IP core. This signal is ignored during JTAG debug operations. The input clock must be free-running.

Note: These options are always available.

Table 4: Conduit Interface

Port Name	Width	Direction	Function
freeze	**1**	Output	Active high signal used to freeze the PR interface signals of the region undergoing partial reconfigura-tion. De-assertion of this signal indicates the end of PR operation. **Note:** Input freeze is required for Cyclone V and Stratix V devices. Refer to the *Freeze Logic for PR Regions* topic for more information.

Note: This option is always available.

Table 5: Conduit Interface

Port Name	Width	Direction	Function
pr_start	1	Input	A signal arriving at this port asserted high initiates a PR event. You must assert this signal high for a minimum of one clock cycle and de-assert it low prior to the end of the PR operation. This makes the PR IP core ready to accept the next pr_start trigger event when the freeze signal is low. The PR IP core ignores this signal during JTAG debug operations.
data[]	1, 8, 16, or 32	Input	Selectable input PR data bus width, either x1, x8, x16, or x32. Once a PR event is triggered, it is synchronous with the rising edge of the clk signal whenever the data_valid signal is high and the data_ready signal is high. The PR IP core ignores this signal during JTAG debug operations.
data_valid	1	Input	A signal arriving at this port asserted high indicates the data[] port contains valid data. The PR IP core ignores this signal during JTAG debug operations.

Port Name	Width	Direction	Function
data_ready	1	Output	A signal arriving at this port asserted high indicates the PR IP core is ready to read the valid data on the `data[]` port whenever the `data_valid` signal is asserted high. The data sender must stop sending valid data if this port is low. This signal deasserts low during JTAG debug operations.

status[2..0]	1	Output	A 3-bit error output used to indicate the status of PR event. Once an error is detected (`PR_ERROR`, `CRC_ERROR`, or incompatible bitstream error), this signal latches high and only resets at the beginning of the next PR event, when `pr_start` is high and `freeze` is low. For example:
			
			`3'b000 – power-up or nreset asserted`
			
			`3'b001 – PR_ERROR was triggered`
			
			`3'b010 – CRC_ERROR was triggered`
			
			`3'b011 – Incompatible bitstream error detected`
			
			`3'b100 – PR operation in progress`
			
			`3'b101 – PR operation passed`
			
			`3'b110 – Reserved`
			
			`3'b111 – Reserved`

double_pr	1	Input	When the `pr_start` signal is triggered, until the de-assertion of a `freeze` signal, a signal asserted high on this port indicates the PR event requires double PR cycle. A low signal on this port indicates a single PR cycle event. If your PR design targets a Stratix V device and requires the use of double PR because you have initialized RAM in the PR region, you must assert the `double_pr` input signal high. This assertion ensures that the controller handles double PR properly. If you are instantiating the PR IP in a design that is not using initialized on-chip RAMs, connect this port to 0. You must assert this signal high if the PR bitstream (`.rbf`) is generated with the **Write memory contents** option turned on. Failure to do so causes a `PR_ERROR` assertion during partial reconfiguration. The PR IP core ignores this signal during JTAG debug operations.

Note: These options are available when **Enable Avalon-MM slave interface** parameter is turned **Off**.

Table 6: Avalon-MM Slave Interface

Port Name	Width	Direction	Function
avmm_slave_address	1	Input	Avalon-MM address bus. The address bus is in the unit of Word addressing. Refer to the *Qsys Component* section for more details on the address mapping. The PR IP core ignores this signal during JTAG debug operations.
avmm_slave_read	1	Input	Avalon-MM read control. The PR IP core ignores this signal during JTAG debug operations.
avmm_slave_readdata	16 or 32	Output	Avalon-MM read data bus. The PR IP core ignores this signal during JTAG debug operations.
avmm_slave_write	1	Input	Avalon-MM write control. The PR IP core ignores this signal during JTAG debug operations.
avmm_slave_writedata	16 or 32	Input	Avalon-MM write data bus. The PR IP core ignores this signal during JTAG debug operations.
avmm_slave_waitrequest	1	Output	Asserted to indicate that the IP is busy. Also indicates that the IP core is unable to respond to a read or write request. This signal is pulled high during JTAG debug operations.

Note: These options are available when **Enable Avalon-MM Slave Interface** parameter is turned **On**.

Table 7: Interrupt Interface

Port Name	Width	Direction	Function
irq	**1**	Output	The interrupt signal.

Note: This option is available when **Enable interrupt interface** parameter is turned **On**.

Table 8: CRCBLOCK Interface

These options are available when **Use as PR Internal Host** parameter is turned **Off** or the CRCBLOCK is instantiated manually for an internal host.

Port Name	Width	Direction	Function
crc_error_ pin	**1**	Input	Available when you use the PR IP core as an External Host. Connect this port to the dedicated CRC_ERROR pin of the FPGA undergoing partial reconfiguration.

Table 9: PR Block Interface

Port Name	Width	Direction	Function
pr_ready_ pin	**1**	Input	Connect this port to the dedicated PR_READY pin of the FPGA undergoing partial reconfiguration.
pr_error_ pin	**1**	Input	Connect this port to the dedicated PR_ERROR pin of the FPGA undergoing partial reconfiguration.
pr_done_pin	**1**	Input	Connect this port to the dedicated PR_DONE pin of the FPGA undergoing partial reconfiguration.
pr_request_ pin	**1**	Output	Connect this port to the dedicated PR_REQUEST pin of the FPGA undergoing partial reconfiguration.
pr_clk_pin	**1**	Output	Connect this port to the dedicated DCLK of the FPGA undergoing partial reconfiguration.
pr_data_ pin[15..0]	**16**	Output	Connect this port to the dedicated DATA[15..0] pins of the FPGA undergoing partial reconfiguration.

Note: These options are available when **Use as PR Internal Host** parameter is turned **Off** or when the PRBLOCK is instantiated manually for an internal host.

Related Information

- **Partial Reconfiguration Controller Avalon-MM Slave Interface** on page 17
- **Freeze Logic for 28-nm PR Regions** on page 21
- **FPGA Control Block Interface** on page 19

Avalon®-MM Interface Partial Reconfiguration Sequence

Partial reconfiguration occurs through the Avalon®-MM slave interface in the following sequence:

1. Avalon-MM master component writes `0x01` (or `0x03` if the design requires double PR) to IP address offset 0x1 to trigger PR operation.
2. Avalon-MM master component writes PR bitstream to IP address offset 0x0 until all the PR bitstream is written. When enhanced decompression is on, waitrequest is activated throughout the PR operation. Ensure that your master can handle `waitrequest` from the slave interface.
3. Avalon-MM master component reads the data from IP address offset 0x1 to check the `status[2:0]` value. Optionally, the Avalon-MM master component can read the `status[2:0]` of this IP during a PR operation to detect any early failure, for example, `PR_ERROR`.

Related Information

- **Partial Reconfiguration IP Core Parameters** on page 10
  For more information on PR IP core parameters.
- **Avalon-MM Slave Interface Read and Write Transfer Timing** on page 20
  For more information on the timing specification for the Avalon Memory Mapped Slave interface.

Partial Reconfiguration Controller Avalon-MM Slave Interface

The Partial Reconfiguration Controller IP core provides an Avalon-MM slave interface to read and write to PR configuration registers.

Table 10: Data/CSR Memory Map Format

Name	Address Offset	Access	Description
PR_DATA	0x0	Write	Every data `write` to this address indicates this bitstream was sent to the IP core. Performing a `read` on this address returns all 0's.
PR_CSR	0x1	Read or Write	Control and status registers.
Version Register	0x02	Read-Only	Read-only SW version register. Register is currently 0xAA500003
PR Bitstream ID	0x03	Read-Only	Read-only PR POF ID register

Table 11: PR_CSR Control and Status Registers

Bit Offset	Description
0	Read and write control register for `pr_start` signal. Refer to *Input/Output Port List* section for more details on the `pr_start` signal. `pr_start = PR_CSR[0]` `PR_CSR[0]` is de-asserted to value "0" by the IP core automatically, one clock cycle after it is asserted. This streamlines the flow to avoid manual assertion and de-assertion of this register to control `pr_start` signal.
1	Read and write control register for `double_pr` signal. `double_pr = PR_CSR[1]`
2-4	Read-only status register for `status[2:0]` signal. `PR_CSR[4:2] = status[2:0]`
5	Read and clear bit for interrupt. If the interrupt interface is enabled, reading this bit returns the value of the `irq` signal. Writing a "1" clears the interrupt. If the interrupt interface is disabled, reading this bit always returns a value of "0".
6-15	Reserved. Depends on the Avalon-MM data bus width. When using enhanced compression, data width is limited to 16.

Related Information

- **Avalon-MM Slave Interface Read and Write Transfer Timing** on page 20
- **Partial Reconfiguration IP Core Ports** on page 12

Partial Reconfiguration Controller Interrupt Interface

If you enable the Avalon Memory Mapped Slave interface, you can use the optional interrupt interface.

The IP core asserts `irq` during the following events:

Table 12: Interrupt Interface Events

Status Code	Event
3'b001	`PR_ERROR` occurred.
3'b010	`CRC_ERROR` occurred.
3'b011	The IP core detects an incompatible bitstream.
3'b101	The result of a successful PR operation.

After `irq` asserts, the master performs one or more of the following:

- Query for the status of the PR IP core; `PR_CSR[4:2]`
- Carry out some action, such as error reporting.
- Once the interrupt is serviced, clear the interrupt by writing a "1" to `PR_CSR[5]`.

FPGA Control Block Interface

When you instantiate the PR IP core, you can choose to use it as either an internal host or external host.

- When you use the PR IP core as an internal host, it automatically instantiates the corresponding device `CRCBLOCK` and `PRBLOCK` WYSIWYG atom primitives.
- When you use the PR IP core as external host (placed in another FPGA or CPLD), the PR IP core provides the `CRCBLOCK` and `PRBLOCK` interface ports so you can connect the host to the dedicated PR pins and `CRC_ERROR` pin on the target FPGA being partially reconfigured.

Related Information
Partial Reconfiguration IP Core Ports on page 12

Partial Reconfiguration IP Core Timing Specification

The following timing diagram illustrates a successful Partial Reconfiguration IP core operation. You determine whether the operations passes or fails with the `status[2:0]` output signal.

The PR operation is initated when you assert the `pr_start` signal. Monitor the `status[]` or `freeze` signals to detect the end of the PR operation.

Figure 7: Partial Reconfiguration Timing
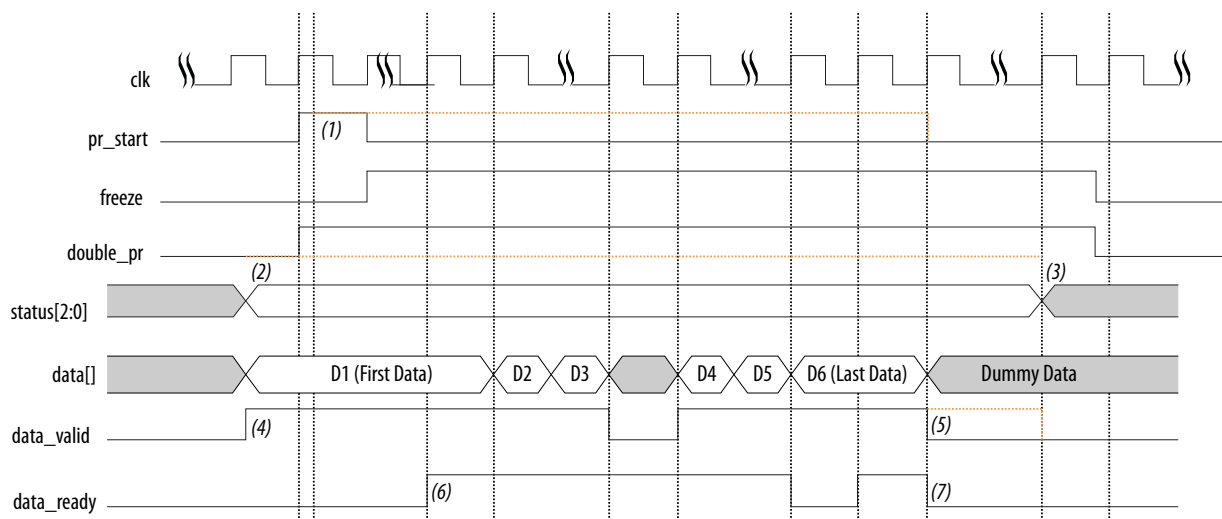
Note:

- You must assert `pr_start` signal high for a minimum of one clock cycle to initiate PR, Deassert `pr_start` before sending the last data.
- `status[]` signal is reset when `pr_start` is asserted. This signal changes during a PR operation if any error such as a `CRC_ERROR`, `PR_ERROR`, or bitstream incompatibility error is detected.
- `status[]` signal changes after a PR operation if `CRC_ERROR` is detected and no error happens during the previous PR operation.
- The `data_valid` signal is not required to be asserted at the same time as the `pr_start`. You can provide the `data[]` and assert `data_valid` when appropriate.
- You can either drive the `data_valid` signal low after sending the last data, or continue to assert `data_valid` high with dummy data on `data[]` until the end of PR, when `freeze` is driven low or `status[]` is updated.
- `data[]` is transferred only when `data_valid` and `data_ready` are asserted on the same cycle. Do not drive new data on the data bus, when both `data_valid` and `data_ready` are not high.
- The `data_ready` signal is driven low once the PR IP core receives the last data.

The `data[]`, `data_valid`, and `data_ready` signals comply with the Avalon-ST specification for Data Transfer with Backpressure. The PR IP Core acts as a sink, with `readLatency` set to `0`. For more information, refer to the *Avalon Interface Specifications*.

Important: The `PR_CLK` signal has a different nominal maximum frequency for each device. Most Stratix V devices have a nominal maximum frequency of at least 62.5 MHz.

Related Information
Avalon Interface Specifications for Data Transfer with Backpressure

Avalon-MM Slave Interface Read and Write Transfer Timing

The Avalon-MM interface supports read and write transfers with a slave-controlled `waitrequest`. You can cause the slave to stall the interconnect for as many cycles as required by asserting the `waitrequest` signal. If a slave uses `waitrequest` for either read or write transfers, it must use `waitrequest` for both.

A slave typically receives `address`, `read` or `write`, and `writedata` after the rising edge of the clock. A slave asserts `waitrequest` before the rising clock edge to hold off transfers. When the slave asserts `waitrequest`, the transfer is delayed. The address and control signals are held constant. Transfers complete on the rising edge of the first `clk` after the slave port deasserts `waitrequest`.

Figure 8: Read and Write Transfers for Avalon-MM Slave Interface
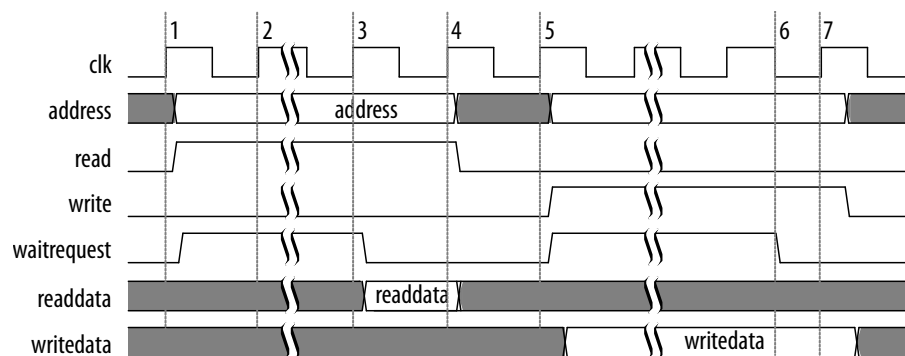
The numbers in this timing diagram, mark the following transitions:

1. `address` and `read` are asserted after the rising edge of `clk`. `waitrequest` is asserted stalling the transfer.
2. `waitrequest` is sampled. Because `waitrequest` is asserted, the cycle becomes a wait-state. `address`, `read`, and `write` remain constant.
3. The slave presents valid `readdata` and deasserts `waitrequest`.
4. `readdata` and deasserted `waitrequest` are sampled, completing the transfer.
5. `address`, `writedata`, and `write` signals are asserted. The slave responds by asserting `waitrequest` stalling the transfer.
6. Deassert the `waitrequest`.
7. The slave captures `writedata` and ends the transfer.

Freeze Logic for 28-nm PR Regions

When partially reconfiguring a design, freeze all the outputs of each PR region to a known constant value.

Freezing prevents the signal receivers in the static region from receiving undefined signals during the partial reconfiguration process. Freezing is important for control signals that you drive from the PR region. Cyclone V or Stratix V devices require that you freeze global and non-global inputs of a PR region.

Figure 9: Freezing at PR Region Boundary
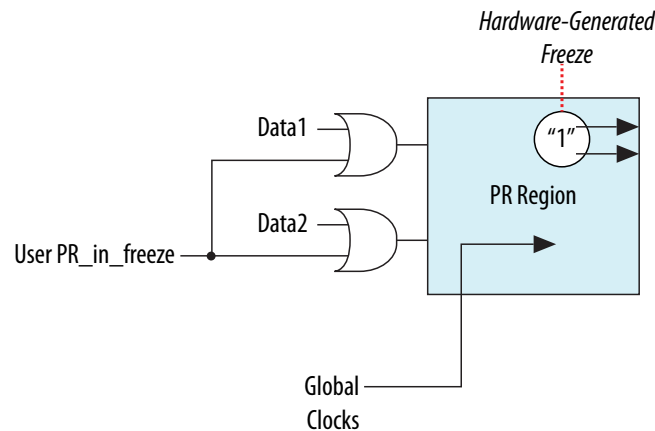
The Partial Reconfiguration IP core includes a freeze port for a single freeze signal that corresponds to the device you configure. When instantiating the IP core in your design, combine this freeze port with your system-level PR control logic to freeze the PR region output. If your design has multiple PR regions, create a decoding logic to route that freeze signal to the appropriate PR region's freeze logic. Do not route the freeze signal to the PR regions unaffected by the current partial reconfiguration.

Note: If you are not using the Partial Reconfiguration IP core in your design, include logic to generate the freeze signal that you use for freezing the PR region outputs.

The static region logic must be independent of all the outputs from the PR regions for a continuous operation. Control the outputs of the PR regions by creating an RTL wrapper around the PR region.

Data Source Controller

This controller handles the source of PR data, either from JTAG or standard data interface.

The JTAG interface takes precedence over the standard PR data interface. For example, whenever JTAG is engaged through command from Quartus Prime Programmer tool, the PR data is sourced from the JTAG interface rather than the PR data interface.

Standard Partial Reconfiguration Data Interface

The PR data interface provides you with selectable input data width; `x1`, `x8`, `x16`, and `x32`. The data interface isconnected to `ASMI_PARALLEL` as well as the Avalon interface to obtain PR data from on-chip RAM, external flash device, or PR over PCIe.

For Cyclone V and Stratix V devices, if the input data width is other than `x16`, the PR IP core includes a data upsize or downsize module so that the data output to the Data Source Controller is always `x16`.

JTAG Debug Mode for Partial Reconfiguration

The JTAG debug mode allows you to configure partial reconfiguration bitstream through the JTAG interface. Use this feature to debug PR bitstream and eventually helping you in your PR design prototyping. This feature is available for internal and external host. Using the JTAG debug mode forces the Data Source Controller to be in x16 mode.

During JTAG debug operation, the JTAG command sent from the Quartus Prime Programmer ignores and overrides most of the Partial Reconfiguration IP core interface signals (`clk`, `pr_start`, `double_pr`, `data[]`, `data_valid`, and `data_read`).

Note: The `TCK` is the main clock source for PR IP core during this operation.

You can view the status of Partial Reconfiguration operation in the messages box and the Progress bar in the Quartus Prime Programmer. The `PR_DONE`, `PR_ERROR`, and `CRC_ERROR` signals will be monitored during PR operation and reported in the Messages box at the end of the operation.

The Quartus Prime Programmer can detect the number of `PR_DONE` instruction(s) in plain or compressed PR bitstream and, therefore, can handle single or double PR cycle accordingly. However, only single PR cycle is supported for encrypted Partial Reconfiguration bitstream in JTAG debug mode (provided that the specified device is configured with the encrypted base bitstream which contains the PR IP core in the design).

Note: Configuring an incompatible PR bitstream to the specified device may corrupt your design, including the routing path and the PR IP core placed in the static region. When this issue occurs, the PR IP core stays in an undefined state, and the Quartus Prime Programmer is unable to reset

the IP core. As a result, the Quartus Prime Programmer generates the following error when you try
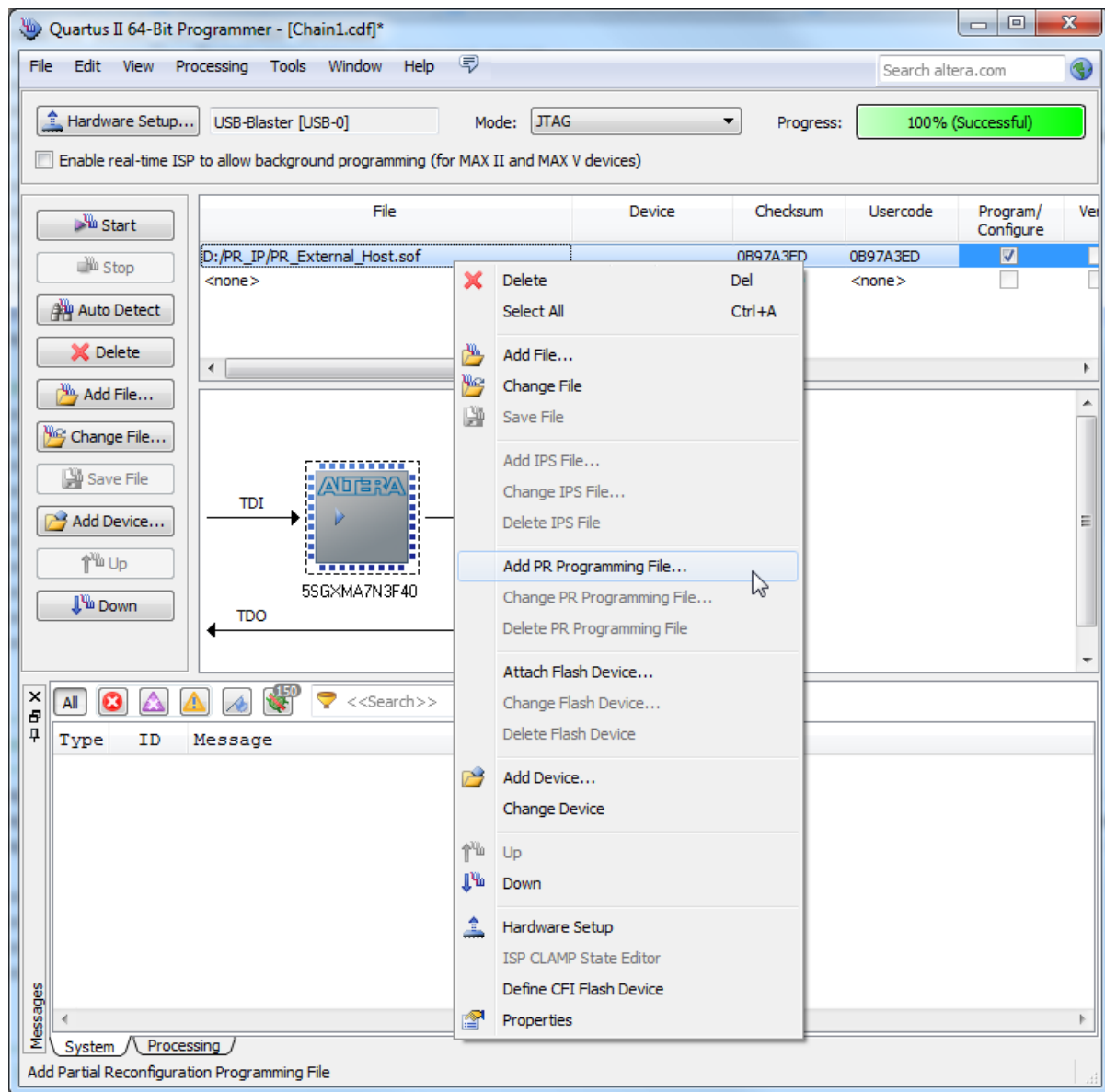to configure a new PR bitstream:

```
Error (12897): Partial Reconfiguration status: Can't reset the PR megafunction.
This issue occurred because the design was corrupted by an incompatible PR
bitstream in the previous PR operation. You must reconfigure the device with a good
design.
```

Configuring Partial Reconfiguration Bitstream in JTAG Debug Mode

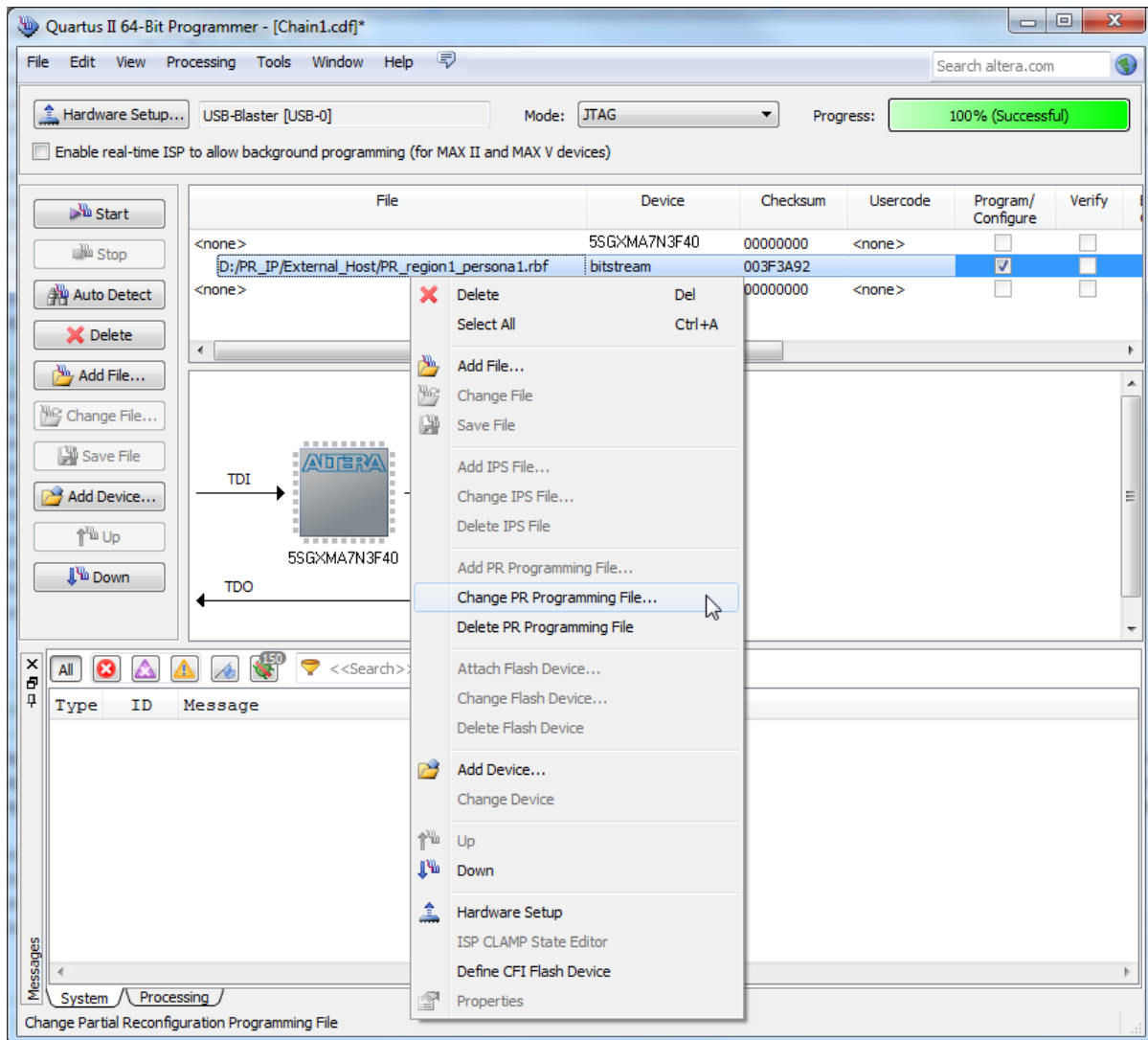To configure the Partial Reconfiguration bitstream in JTAG debug mode, follow these steps:

1. In the Quartus Prime Programmer GUI, right click a highlighted base bitstream (in `.sof`) and then
    click **Add PR Programming File** to add the PR bitstream (`.rbf`).

Figure 10: Adding PR Programming File

2. After adding the PR bitstream, you can change or delete the Partial Reconfiguration programming file by clicking **Change PR Programming File** or **Delete PR Programming File**.

**Figure 11: Change PR Programming File or Delete PR Programming File**

3. Click **Start** to configure the PR bitstream. The Quartus Prime Programmer generates an error message if the specified device does not contain the PR IP core in the design (you must instantiate the Partial Reconfiguration IP core in your design to use the JTAG debug mode).

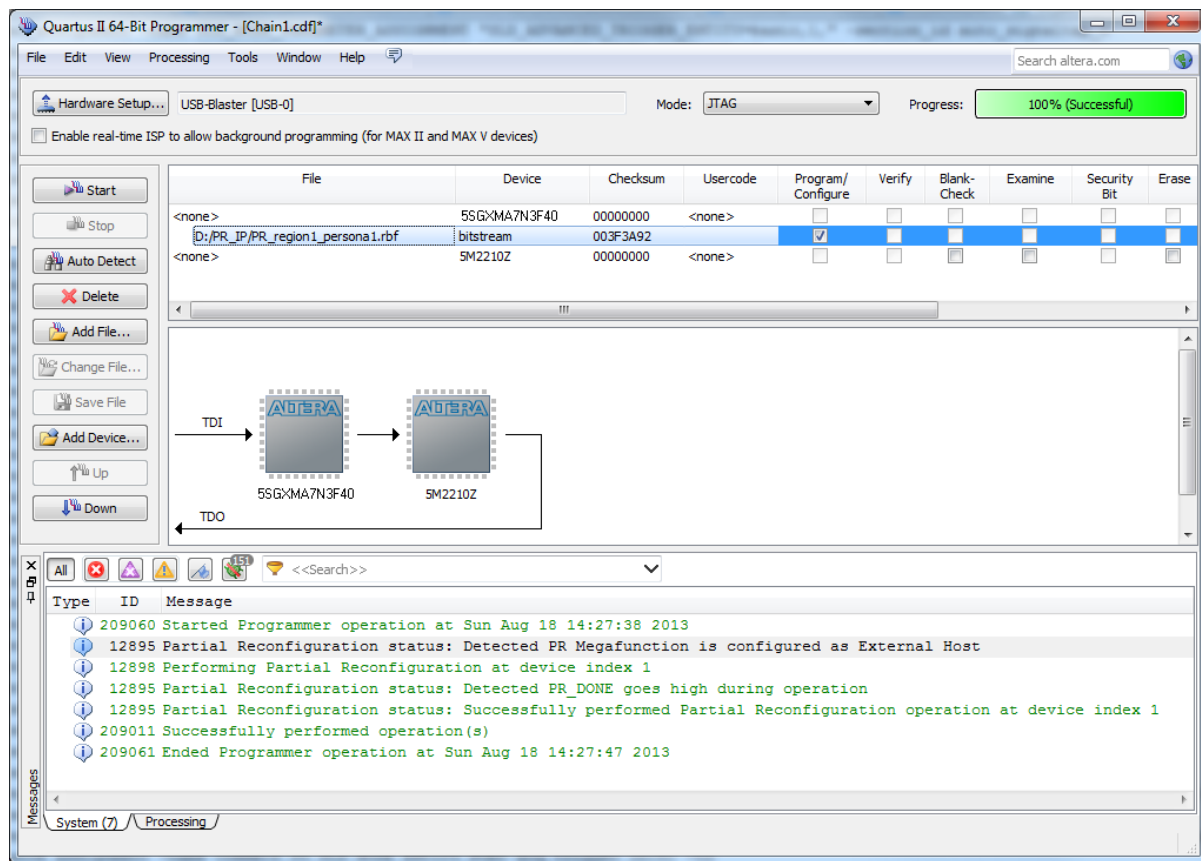**Figure 12: Starting PR Bitstream Configuration**
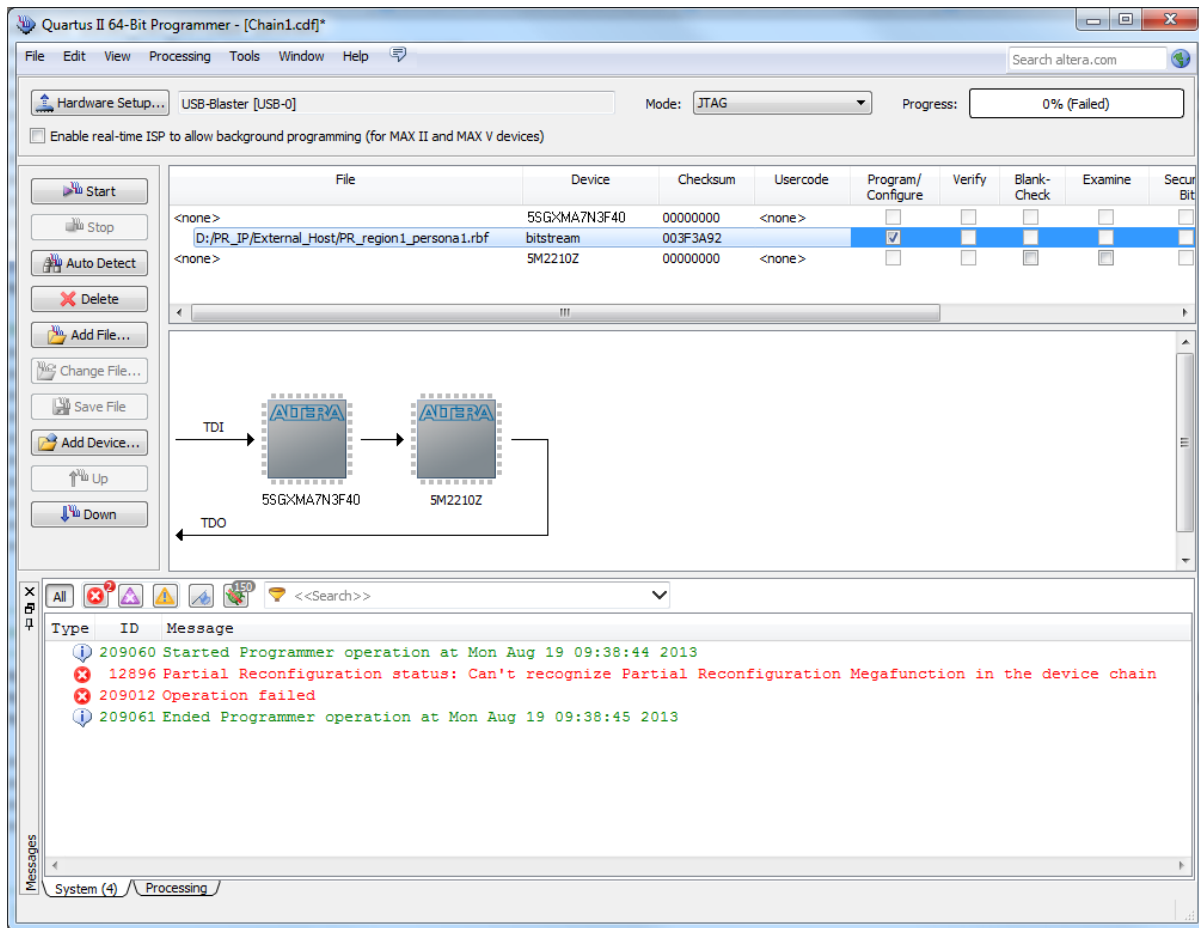
4. Configure the valid .rbf in JTAG debug mode with the Quartus Prime Programmer.
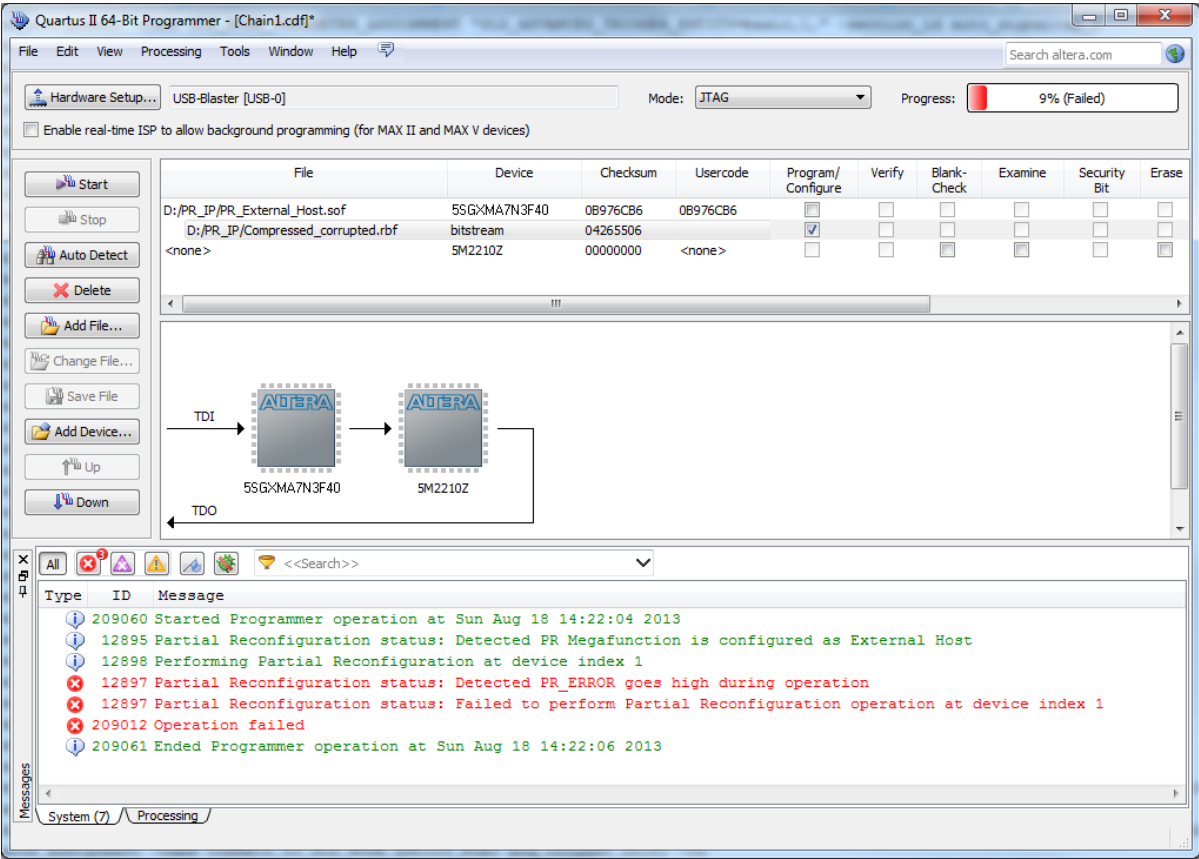
Figure 13: Configuring Valid .rbf
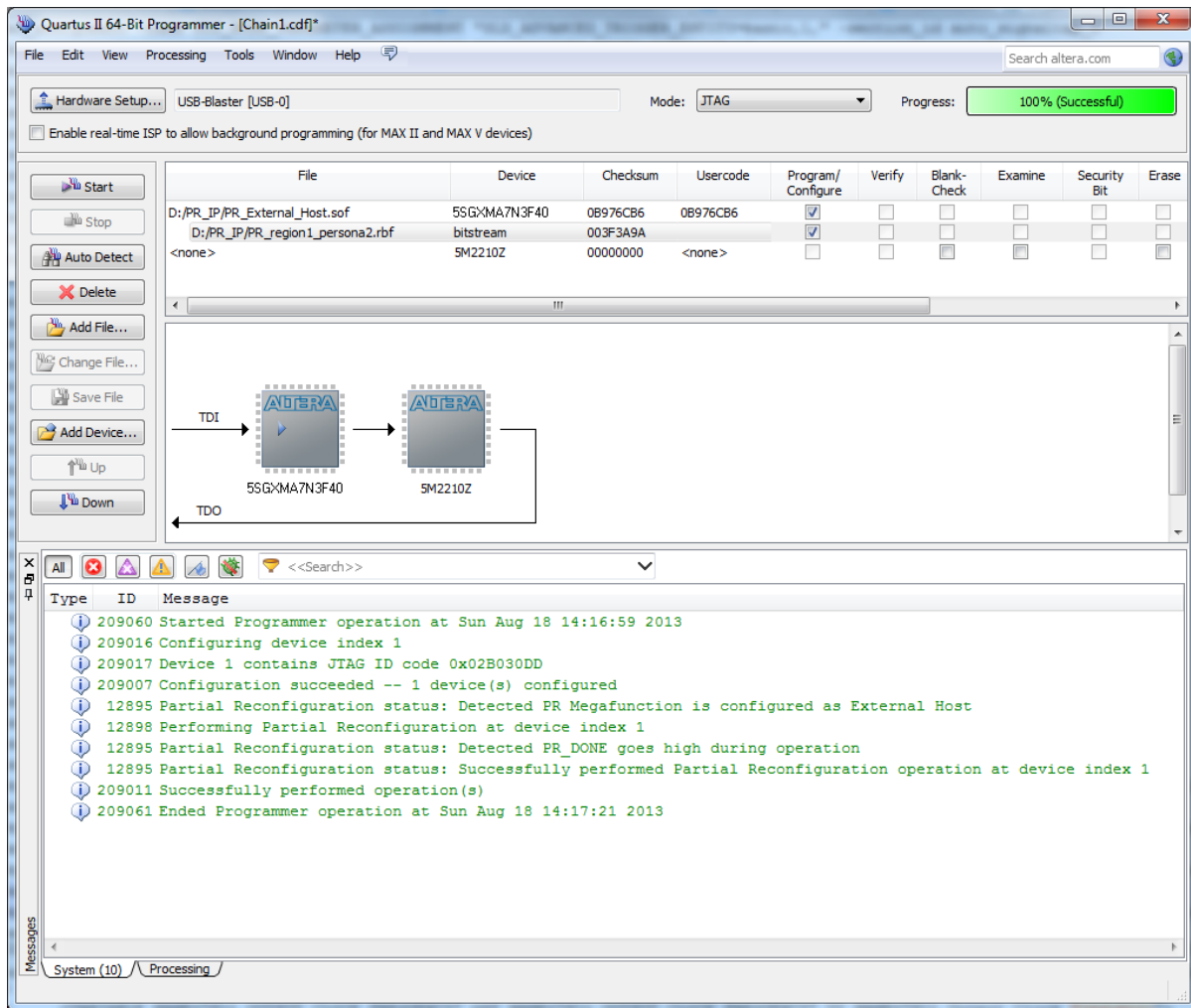
5. The JTAG debug mode is also supported if the PR IP core is pre-programmed on the specified device.

Figure 14: Partial Reconfiguration IP Core Successfully Pre-programmed

6. The Quartus Prime Programmer reports error when you try to configure the corrupted `.rbf` in JTAG debug mode.

Figure 15: Configuring Corrupted .rbf

Partial Reconfiguration IP Core User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
16.1	**Partial Reconfiguration IP Core User Guide**
16.0	**Partial Reconfiguration IP Core User Guide**
15.1	**Partial Reconfiguration IP Core User Guide**
15.0	**Partial Reconfiguration IP Core User Guide**
14.1	**Partial Reconfiguration IP Core User Guide**

Revision History

Date	Version	Changes
May 2017	2017.05.08	Removed support for Arria® 10 devices. For Arria 10 suport refer to the *Partial Reconfiguration Solutions IP User Guide*
Oct 2016	2016.10.31	Added support for Arria 10 devices. • Updated content for Clock-to-Data Ratio. • Updated the Parameters and Ports. • Updated Compression instructions for standard and enhanced compression. • Added supporting content on using PR with JTAG. • Minor edits and fixed typos
May 2016	2016.05.02	Minor changes: • Fixed a link to the Designing for Partial Reconfiguration chapter in Vol 1 of the Quartus Prime Handbook. • Fixed typos.
Nov 2015	2015.11.20	Revised the following topics: • Partial Reconfiguration IP Core Parameters—updated supported data width • Partial Reconfiguration IP Core Timing Specification—revised the timing diagram • Deprecated the Sample Partial Reconfiguration IP Core as an External Host on the Same Device topic • Added Enable Enhanced Compression topic
May 2015	2015.05.04	Revised the following topics: • Partial Reconfiguration IP Core Parameters—added new parameters for device family support • Partial Reconfiguration IP Core Ports—added new port options • Partial Reconfiguration IP Core Timing Specification—revised the timing diagram
January 2015	2015.01.29	Minor error corrections.
August 2014	2014.08.20	• Added Avalon Memory Map slave interface • Updated Ports and Parameters to support Avalon Memory Map slave interface • Added Bitstream compatibility checking • Added sample pseudo-code for creating a freeze wrapper for multiple PR regions and creating an external host on the same device.

Date	Version	Changes
November 2013	2013.11.04	Initial release