CHANNEL LINEARITY MISMATCH EFFECTS IN TIME-INTERLEAVED ADC SYSTEMS

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ABSTRACT

A time-interleaved ADC system is an effective way to implement a high-sampling-rate ADC with relatively slow circuits. In the system, several channel ADCs operate at interleaved sampling times as if they were effectively a single ADC operating at a much higher sampling rate. However, mismatches among channel ADCs degrade S/N of the ADC system as a whole, and the effects of offset, gain and bandwidth mismatches as well as timing skew of the clocks distributed to the channels have been well investigated. This paper investigates the channel *linearity mismatch* effects in the time-interleaved ADC system, which are practically very important but have not been investigated yet. We consider two cases: differential nonlinearity mismatch and integral nonlinearity mismatch cases. Our numerical simulation shows their distinct features especially in frequency domain. The derived results can be useful for calibration algorithms to compensate for the channel mismatch effects.

Keywords ADC, Interleave, Channel Mismatch, DNL, INL

1. INTRODUCTION

Electronic devices are continuously getting faster and accordingly the need for instruments such as digitizing oscilloscopes and LSI testers to measure their performance is growing. A/D converters (ADCs) incorporated in such instruments have to operate at very high sampling rate. This paper studies theoretical issues of a time-interleaved ADC system where several channel ADCs operate at interleaved sampling times as if they were effectively a single ADC operating at a much higher sampling rate [3, 4, 5, 6]. Fig.1 shows such an ADC system where each M channel ADCs $(ADC_1, ADC_2, ..., ADC_M)$ operates with one of M phase clocks $(CK_1, CK_2, ..., CK_M)$ respectively. The sampling rate of the ADC as a whole is M times the channel sampling rate. This time-interleaved ADC system is an effective way to implement a high-sampling-rate ADC with relatively slow circuits, and is widely used. Ideally characteristics of channel ADCs should be identical and clock skew should be zero. However, in reality there are mismatches such as offset, gain mismatches among channel ADCs as well as timing skew of the clocks distributed to them, which cause so-called *pattern noise* and significantly degrade S/N (effective bits) of the ADC system as a whole. Hence calibration often has to be incorporated to ensure uniformity among the characteristics of the channels. It is important to clarify the issues of the interleaved ADC architecture for designing the system.

In previous studies, the effects of offset, gain, timing and bandwidth mismatches have been intensively investigated [1, 5, 6, 7, 8, 9]. In this paper, we will investigate the *linearity mismatch* effect, which is rather a new concept but a very important and complicated problem in practical applications. We will consider two cases (i.e., differential nonlinearity (DNL) mismatch and integral nonlinearity (INL) mismatch cases), and our numerical simulations show interesting results especially in frequency domain. To our knowledge, this is the first paper that discusses the linearity mismatch effects.

Hereafter, we will use following notations:
M: number of channel ADCs in the ADC system,
f_{in}: input frequency applied to the ADC system,
f_s: sampling frequency of the ADC system,
f_s/M: sampling frequency of each channel ADC.

2. DNL MISMATCH EFFECTS

Suppose that DNLs and INLs of all channel ADCs are less than 1LSB and 0.5LSB respectively, but their DNLs (and also INLs) have mismatches. We will call this case *DNL mismatch*. Fig.2 (a) explains DNL of a nonideal ADC, and Fig.2 (b) shows simulated 8-channel interleaved ADC output for a sinusoidal input when its channel ADCs have DNL mismatches. We see that so-called "1 LSB noise" is observed. Fig,2 (c) shows simulated power spectrum of 8-channel interleaved ADC output when its channel ADCs have DNL mismatches, where no distinct error power spectrum due to DNL mismatches seems not to be recognized. However we will characterize the error power spectrum due to DNL mismatches as the quantization noise power spectrum distribution.

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For a sinusoidal input, we re-arrange the ADC output waveform to reconstruct a waveform of one period using modulo time plot [2] (which is a similar technique to the equivalent-time sampling, see Fig.3 (a)). Since the output is reconstructed as a sine wave of one period, after its DFT, the signal power spectrum has peak at the frequency of the first bin (Fig.3 (b)). Also note that some power spectrum skirt of quantization noise is observed around the signal power spectrum as shown in Fig.3 (b). We remark that the quantization noise of even an ideal ADC is not *white* for a sinusoidal input and has similar power spectrum to Fig.3 (b); it can be analyzed using Chebysev polynomials [10]. Now let us consider the DNL mismatch case. Fig.3 (c) shows simulated power spectrum with DNL mismatches after modulo time plot for an 8-channel interleaved ADC, and we can recognize the quantization noise power peaks around 0, $f_s/8$, $2f_s/8$, $3f_s/8$ and $4f_s/8$. In general for an M-channel interleaved ADC, the quantization noise power has peaks around kf_s/M, $(k = 0, 1, ..., M-1)$; we claim that this is the frequency domain feature of a time-interleaved ADC with DNL mismatches.

Note that the relationship between the frequency bins of k (before modulo time plot) and l (after modulo time plot) is given as $k = mod_N(nl)$, where N is the number of output points (DFT points) and $f_{in}/f_s = n/N$.

Regarding to the total SNR of a time-interleaved ADC with DNL mismatches, our simulation results show that SNR of the whole interleaved ADC is almost equal to (slightly below)

For a DC input, our simulation shows that pattern noises whose power spectrum are at kf_s/M, $(k = 0, 1, ..., M-1)$ are caused, and this effect is similar to the offset mismatch case [1].

3. INL MISMATCH EFFECTS

Next let us consider the case that channel ADCs have considerable amount of INLs (not necessarily less than 0.5LSB) and also their INLs can mismatch. We will call this case *INL mismatch*. Fig.4 (a) explains INL of a nonideal ADC, and Fig.4 (b) shows simulated 8-channel interleaved ADC output for a sinusoidal input when its channel ADCs have INL mismatches, where a pattern noise is observed. Fig,5 (a) shows simulated power spectrum of an interleaved ADC output with INL (but without INL mismatches), and due to the INL, harmonics powers at kf_{in} $(k = 0, 2, 3, 4...)$ are observed. On the other hand, Fig.5 (b) shows simulated power spectrum of an 8-channel interleaved ADC output with INL mismatches, and we see that error power peaks are at frequencies of $k \times f_s/8 \pm nf_{in}$ $(k = 0, 1, 2, 3; n = 0, 1, 2, 3, ...)$. In general for an M-channel interleaved ADC, the error power has peaks at $kf_s/M \pm nf_{in}$ $(k = 0, 1, 2, .., M-1; n = 0, 1, 2, 3, ...)$, and for a given k, the powers at $kf_s/M + nf_{in}$ and $k \times f_s/M - nf_{in}$ are equal. We claim that these are the frequency domain features of a time-interleaved ADC with INL mismatches.

Regarding to the total SNR of a time-interleaved ADC with INL mismatches, our simulation results show that SNR of the whole ADC is *far* below the average of SNRs among channel ADCs, even though it is better than the worst channel ADC SNR. Recall that in DNL mismatch case, SNR of the whole ADC is *slightly* below the average of channel SNRs. This difference would be due to the fact that nonlinearities of channel ADCs are much larger in INL mismatch case than those in DNL mismatch case.

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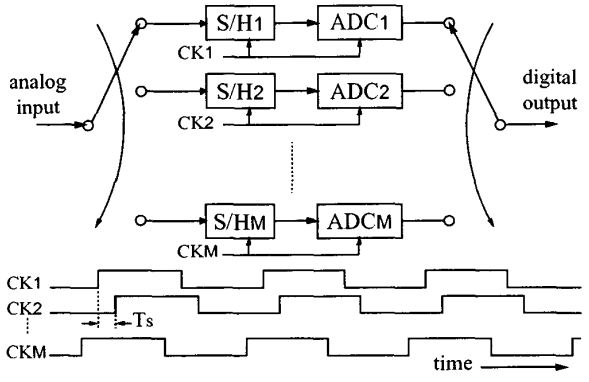

Fig. 1: Time-interleaved ADC system.

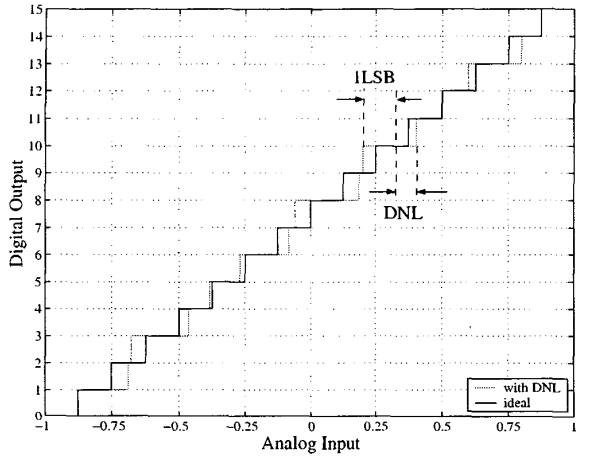

Fig. 2(a): Ideal ADC characteristics and DNL.

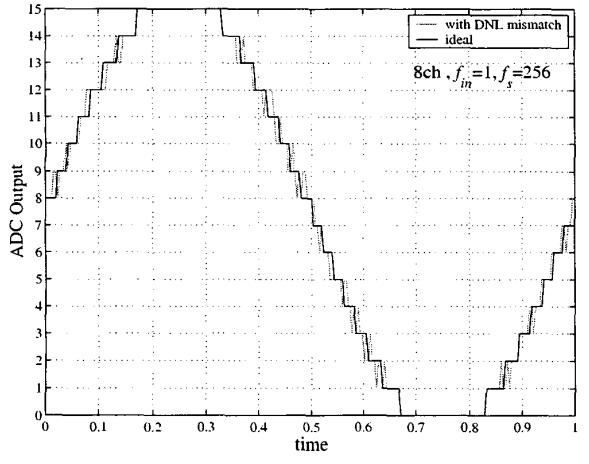

Fig. 2(b): 8-channel interleaved ADC output for a sinusoidal input when its channel ADCs have DNL mismatches.

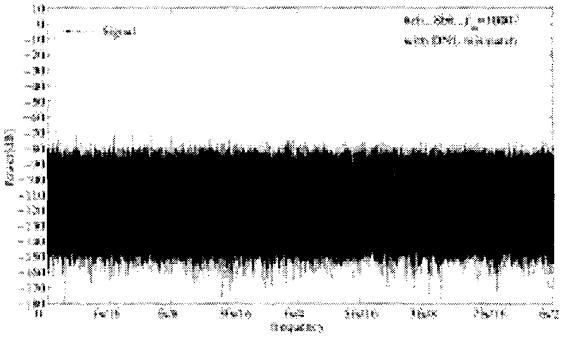

Fig. 2(c): Power spectrum of 8-channel interleaved ADC output when its channel ADCs have DNL mismatches.

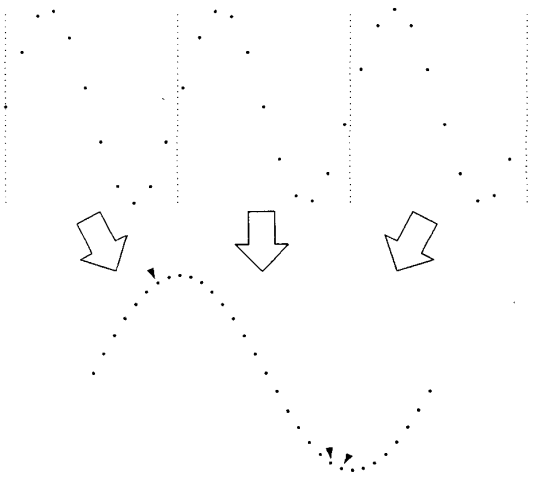

Fig. 3(a): ADC output waveform reconstruction for a sinusoidal input (modulo time plot).

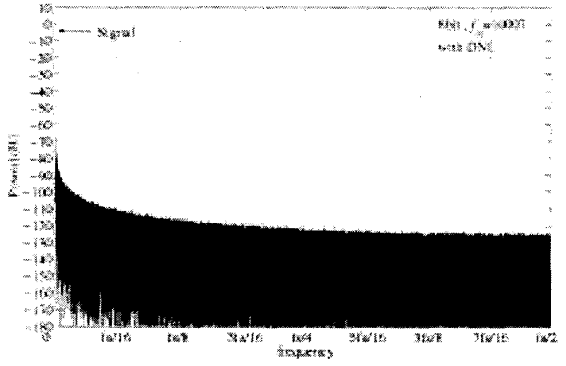

Fig. 3(b): Power spectrum without DNL mismatches after modulo time plot.

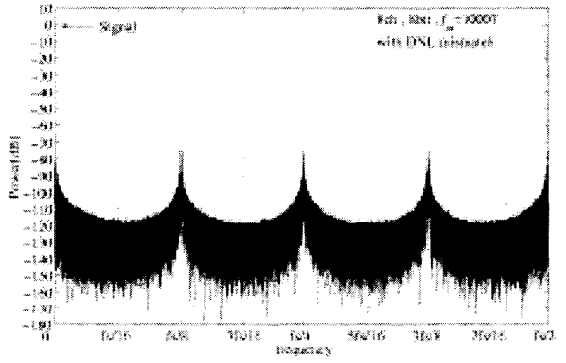

Fig. 3(c): Power spectrum with DNL mismatches after modulo time plot (8-channel case).

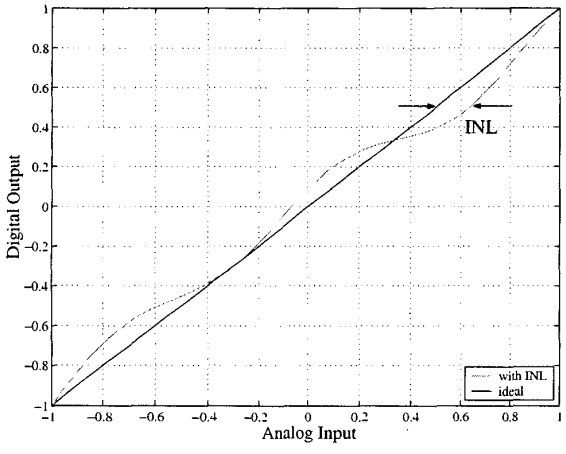

Fig. 4(a): Ideal ADC characteristics and INL.

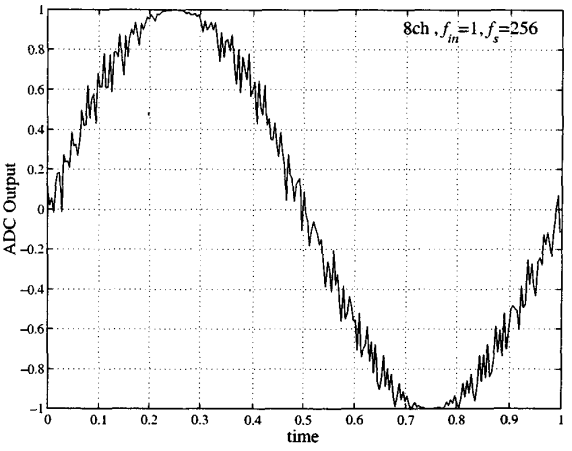

Fig. 4(b): 8-channel interleaved ADC output for a sinusoidal input when its channel ADCs have INL mismatches.

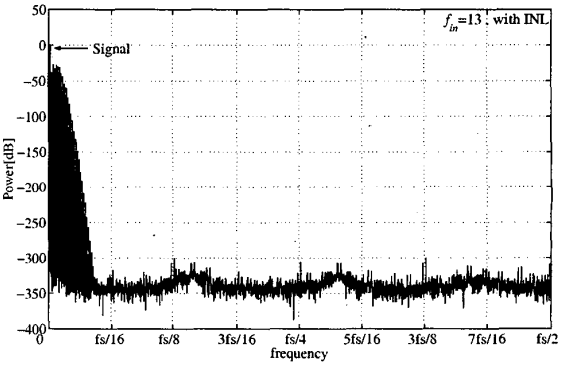

Fig. 5(a): Power spectrum for a sinusoidal input with INL but without INL mismatches.

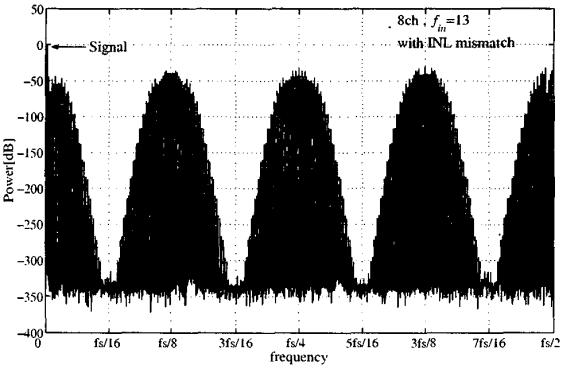

Fig. 5(b): Power spectrum with INL mismatches (8-channel case).