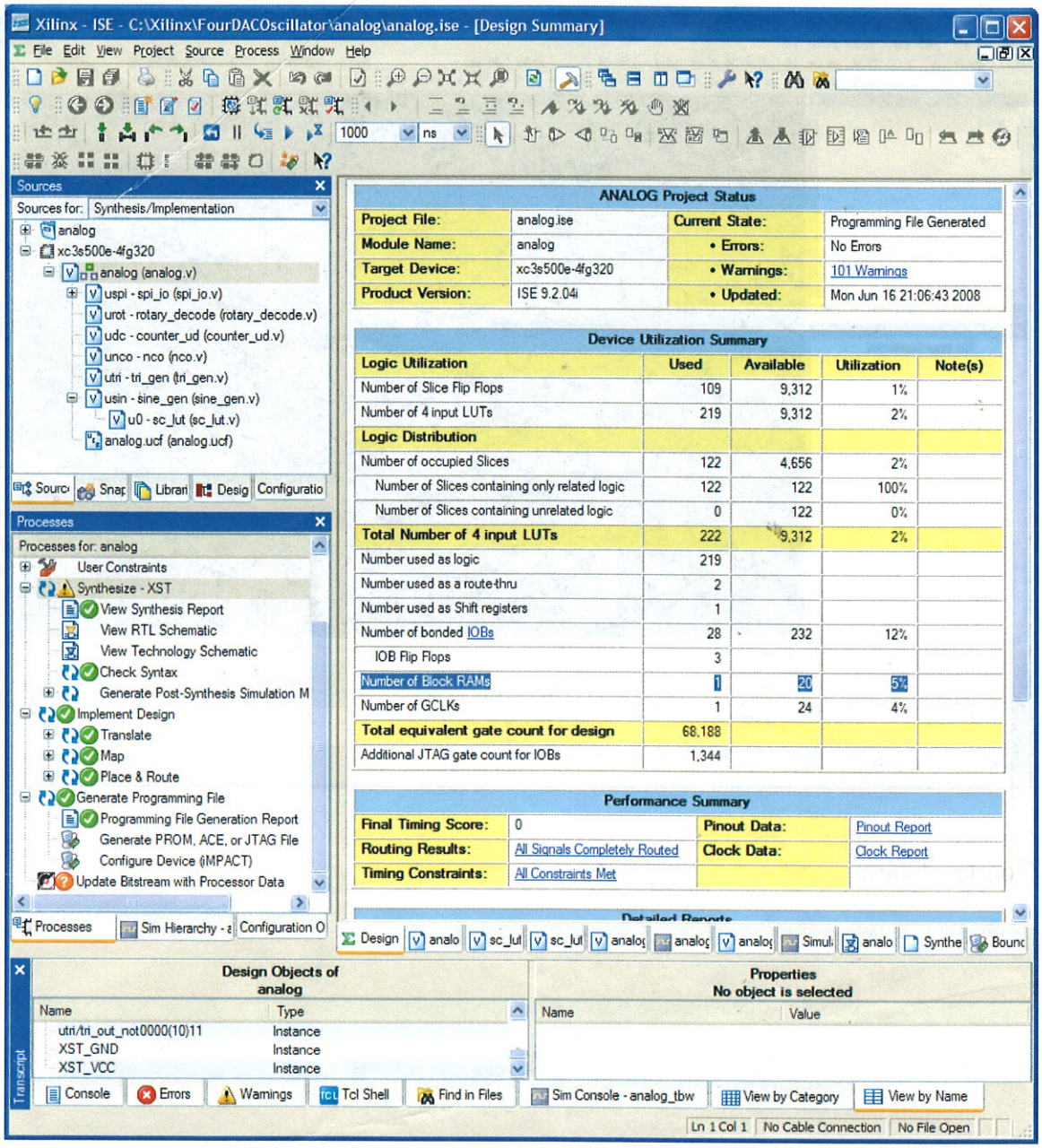
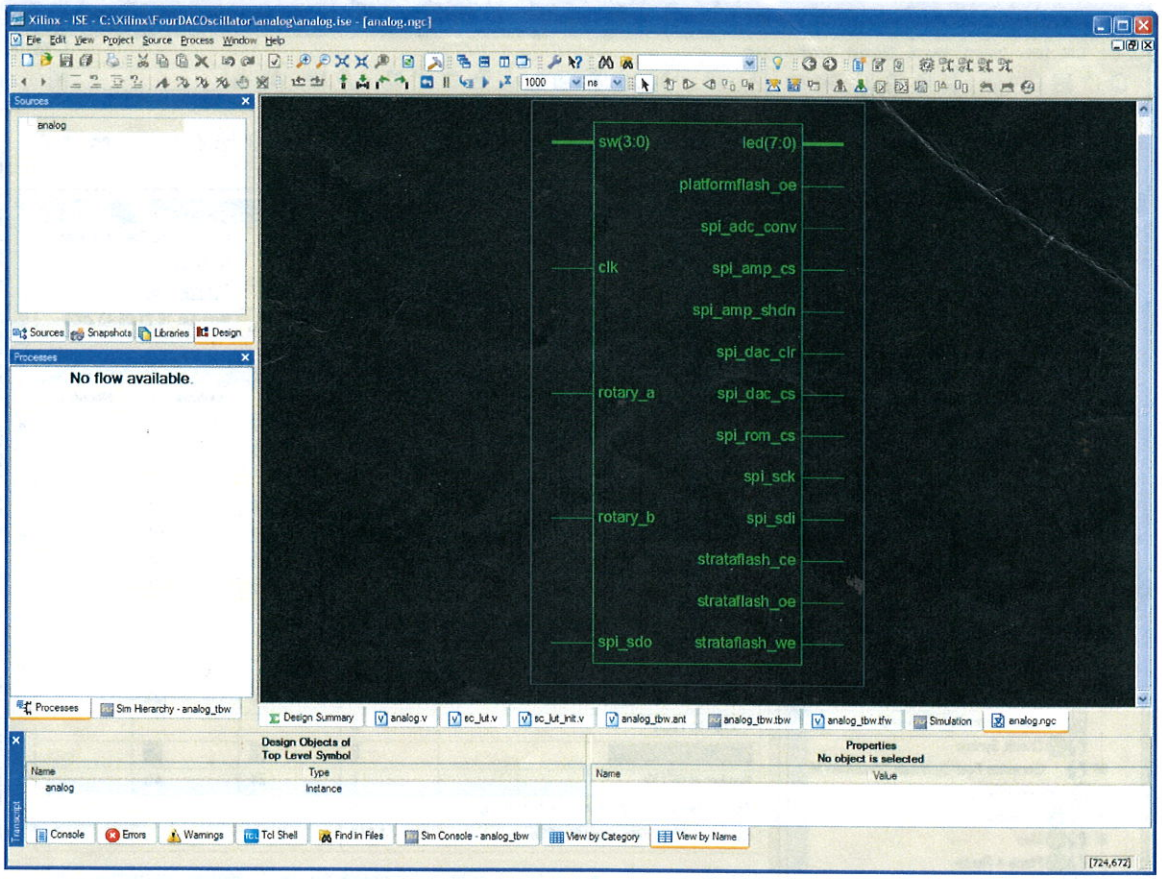
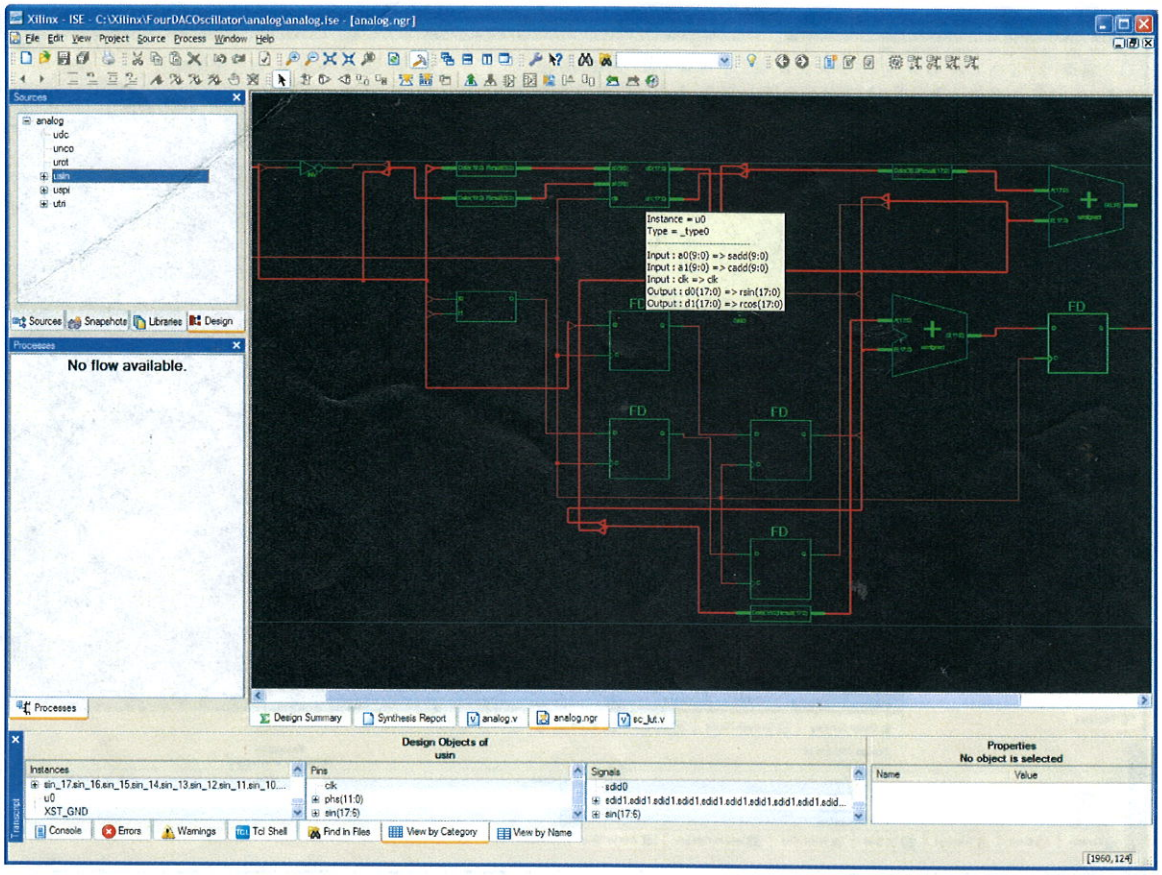
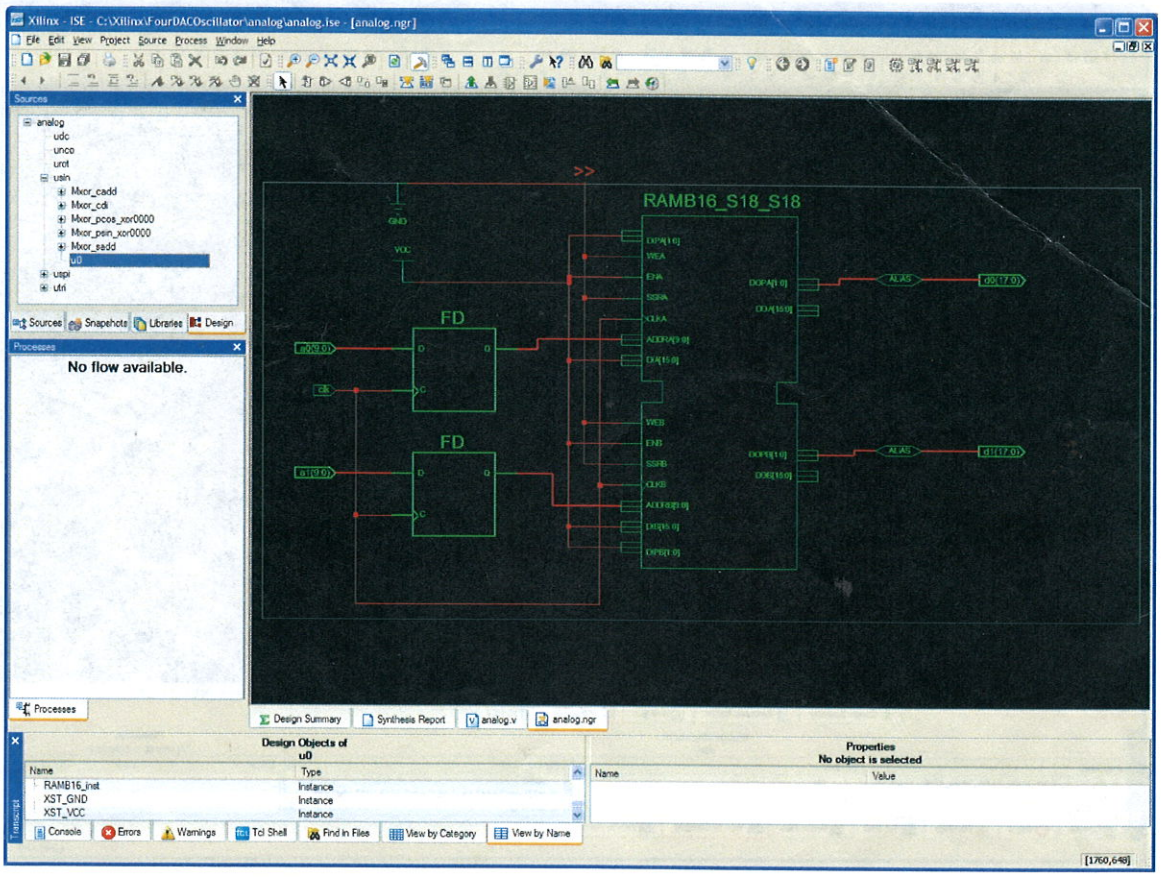

Xilinx - ISE - C:\Xilinx\FourDACOscillator\analog\analog.ise - [Design Summary]
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Implementation
analog
xc3s500e-4fg320
analog (analog.v)
uspi - spi_io (spi_io.v)
urot - rotary_decode (rotary_decode.v)
udc - counter_ud (counter_ud.v)
unco - nco (nco.v)
utri - tri_gen (tri_gen.v)
usin - sine_gen (sine_gen.v)
u0 - sc_lut (sc_lut.v)
analog.ucf (analog.ucf)
Processes
Processes for: analog
User Constraints
Synthesize - XST
View Synthesis Report
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simulation M
Implement Design
Translate
Map
Place & Route
Generate Programming File
Programming File Generation Report
Generate PROM, ACE, or JTAG File
Configure Device (iMPACT)
Update Bitstream with Processor Data
ANALOG Project Status
Project File: analog.ise
Current State: Programming File Generated
Module Name: analog
• Errors: No Errors
Target Device: xc3s500e-4fg320
• Warnings: 101 Warnings
Product Version: ISE 9.2.04i
• Updated: Mon Jun 16 21:06:43 2008
Device Utilization Summary
Logic Utilization | Used | Available | Utilization | Note(s)
Number of Slice Flip Flops | 109 | 9,312 | 1%
Number of 4 input LUTs | 219 | 9,312 | 2%
Logic Distribution
Number of occupied Slices | 122 | 4,656 | 2%
Number of Slices containing only related logic | 122 | 122 | 100%
Number of Slices containing unrelated logic | 0 | 122 | 0%
Total Number of 4 input LUTs | 222 | 9,312 | 2%
Number used as logic | 219
Number used as a route-thru | 2
Number used as Shift registers | 1
Number of bonded IOBs | 28 | 232 | 12%
IOB Flip Flops | 3
Number of Block RAMs | 1 | 20 | 5%
Number of GCLKs | 1 | 24 | 4%
Total equivalent gate count for design | 68,188
Additional JTAG gate count for IOBs | 1,344
Performance Summary
Final Timing Score: 0
Pinout Data: Pinout Report
Routing Results: All Signals Completely Routed
Clock Data: Clock Report
Timing Constraints: All Constraints Met
Design Objects of analog
Name | Type
utri/tri_out_not0000(10)11 | Instance
XST_GND | Instance
XST_VCC | Instance
Properties
No object is selected
Name | Value
Console
Errors
Warnings
Tcl Shell
Find in Files
Sim Console - analog_tbw
View by Category
View by Name
Ln 1 Col 1
No Cable Connection
No File Open



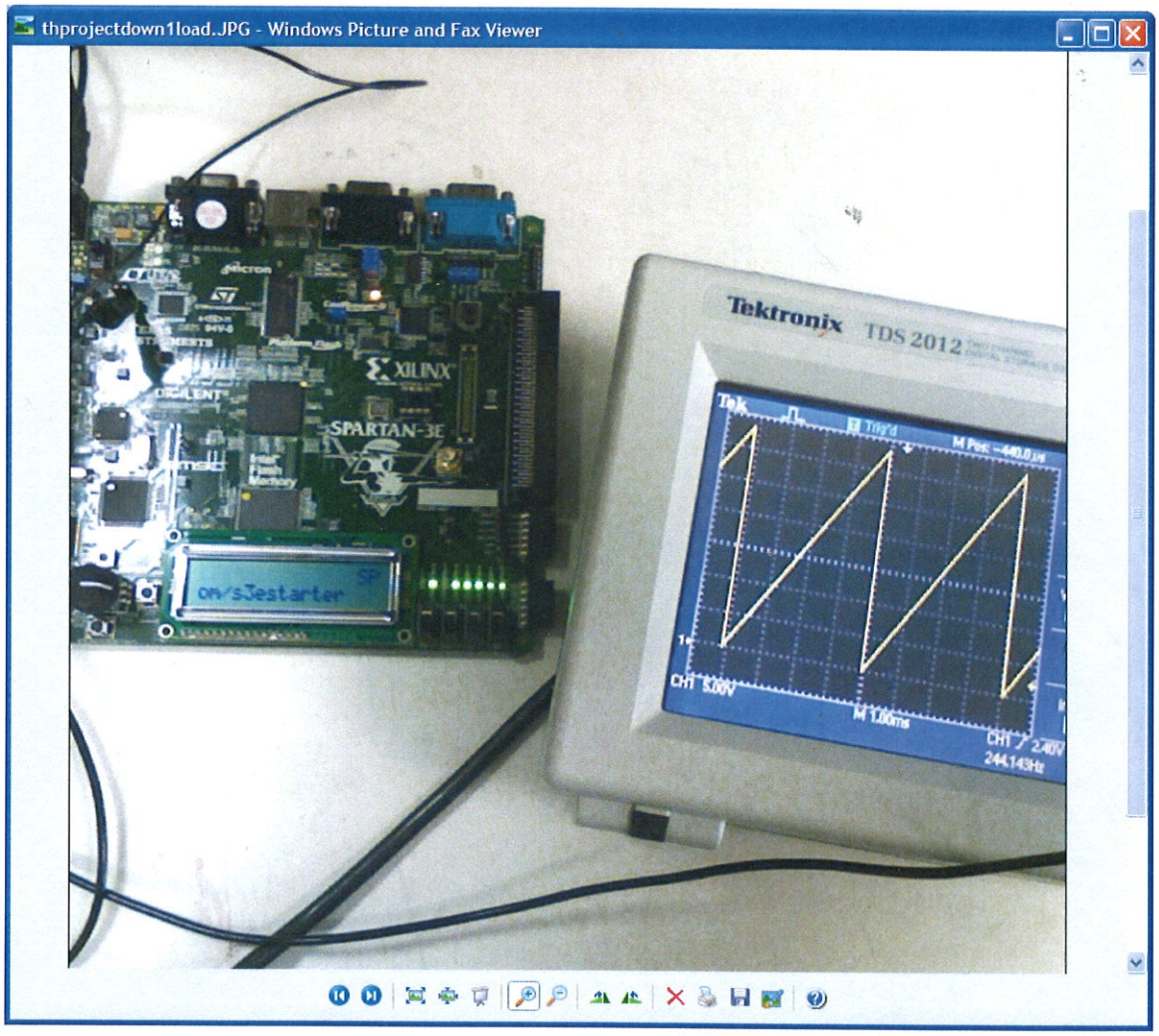
Top-level view

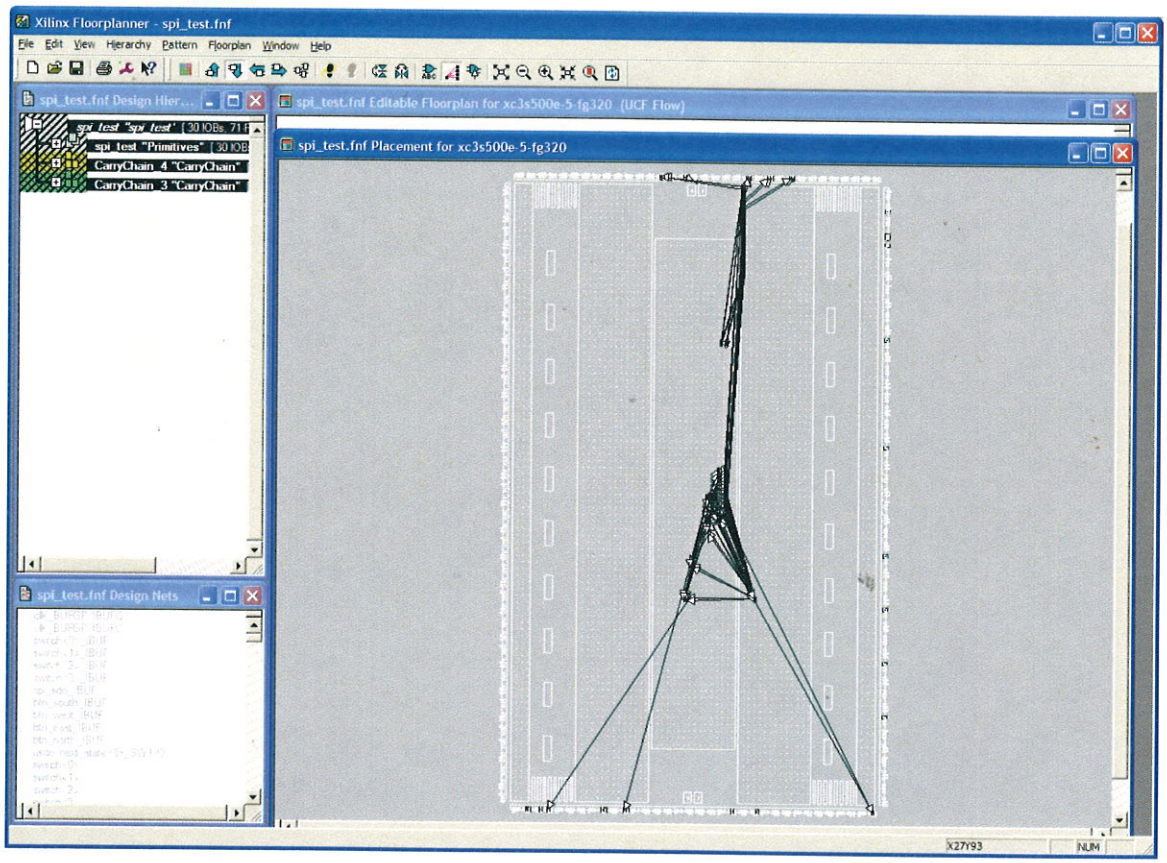


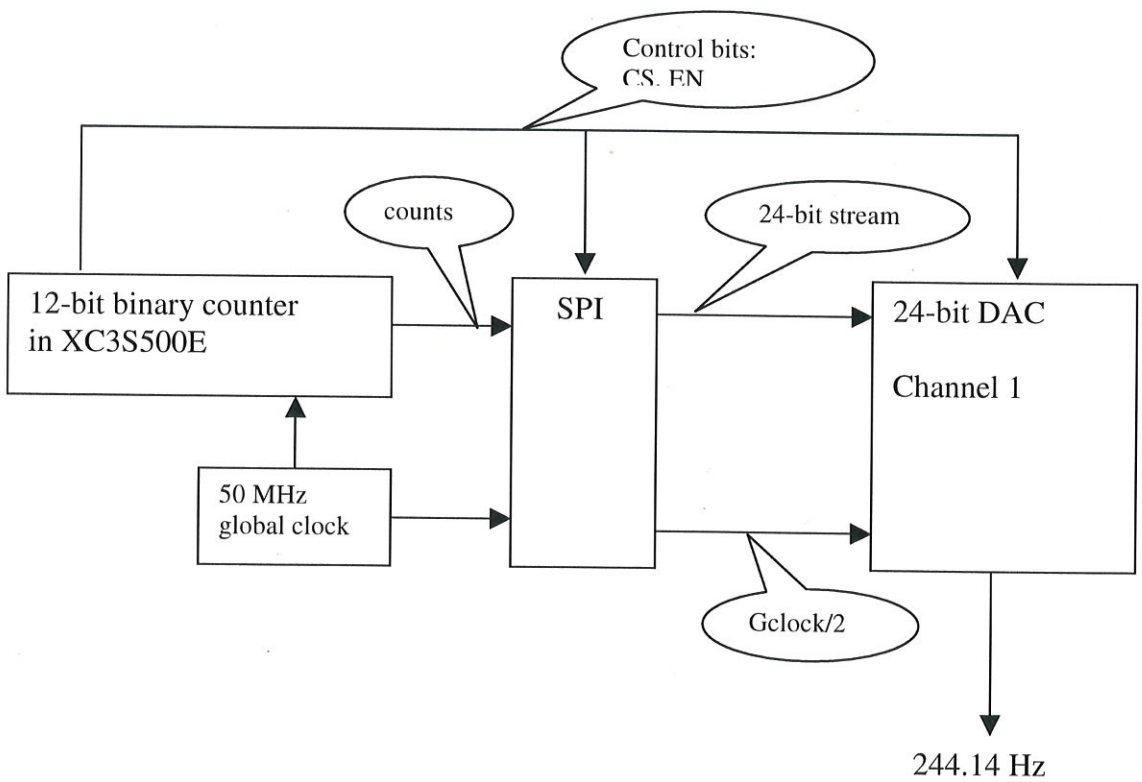
The Block RAM is connected other logic in the sine generator module



The Block RAM is configured as a ROM


thprojectdown1load.JPG - Windows Picture and Fax Viewer
Tektronix
TDS 2012
XILINX
SPARTAN-3E
OM/sJestarter


Xilinx Floorplanner - spi_test.fnf
File Edit View Hierarchy Pattern Floorplan Window Help
spi_test.fnf Design Hier...
spi_test "spi_test" 30 IOBs 71
spi_test "Primitives" 30 IOB
CarryChain_4 "CarryChain"
CarryChain_3 "CarryChain"
spi_test.fnf Design Nets
spi_test.fnf Editable Floorplan for xc3s500e-5-fg320 (UCF Flow)
spi_test.fnf Placement for xc3s500e-5-fg320
X27Y93
NUM


Control bits:
CS, EN
counts
24-bit stream
12-bit binary counter
in XC3S500E
SPI
24-bit DAC
Channel 1
50 MHz
global clock
Gclock/2
244.14 Hz