ĐẠI HỌC QUỐC GIA THÀNH PHỐ HỒ CHÍ MINH

TRƯỜNG ĐẠI HỌC BÁCH KHOA

KHOA ĐIỆN – ĐIỆN TỬ

BÁO CÁO THÍ NGHIỆM THIẾT KẾ VI MẠCH
MINI PROJECT 1

LỚP: L01 ---- NHÓM: 01

STT	Sinh viên thực hiện	Mã số sinh viên
1	Lê Quốc Thái	2114764
2	Nguyễn Khánh Huy	2113510
3	Nguyễn Thành Phát	2114378
4	Nguyễn Ngọc Kiều Duyên	2113053
5	Huỳnh Thịnh Phát	2114369

Thành phố Hồ Chí Minh – 2024

DANH SÁCH THÀNH VIÊN

STT	Sinh viên thực hiện	Mã số sinh viên	Đóng góp
1	Lê Quốc Thái	2114764	100%
2	Nguyễn Khánh Huy	2113510	100%
3	Nguyễn Thành Phát	2114378	100%
4	Nguyễn Ngọc Kiều Duyên	2113053	100%
5	Huỳnh Thịnh Phát	2114369	100%

MỤC LỤC

EXPERIMENT 3

Objective: Design a combinational circuit - a 1-bit Full Adder.

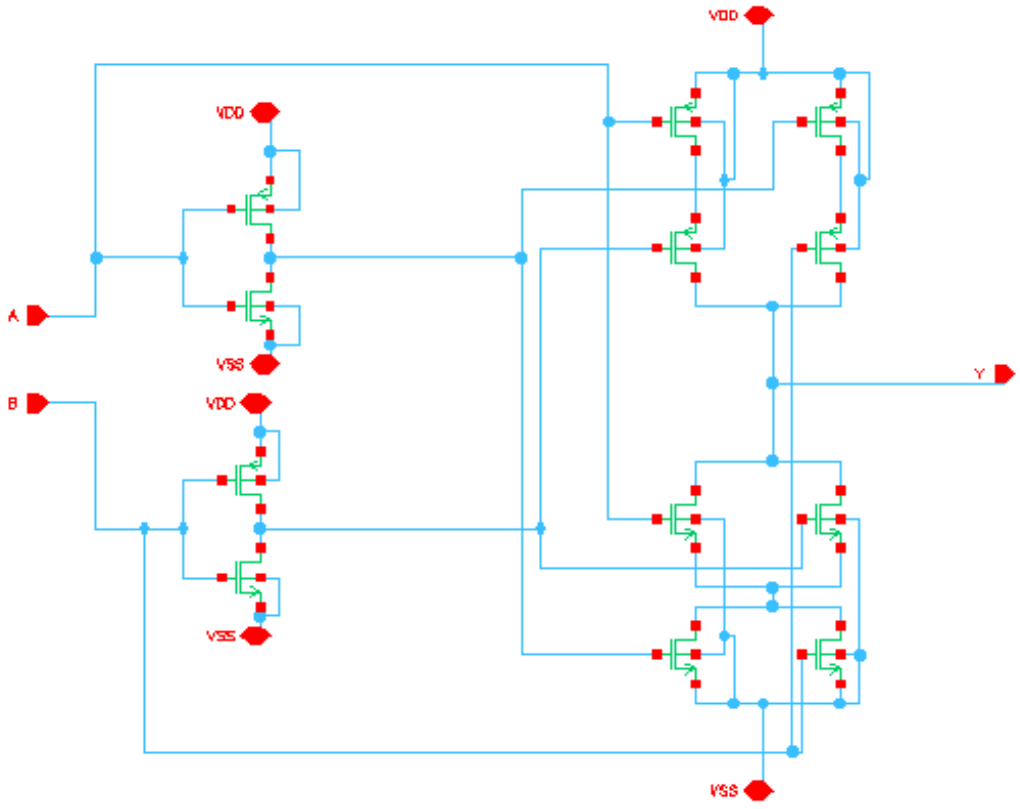
I. XOR

1. Truth table, schematic, symbol

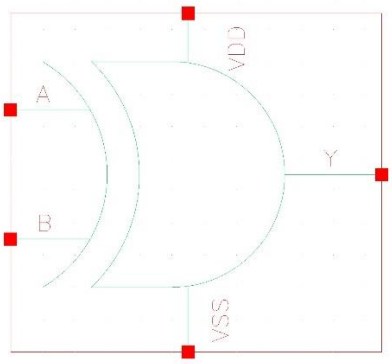
- XOR truth table:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

- XOR schematic:

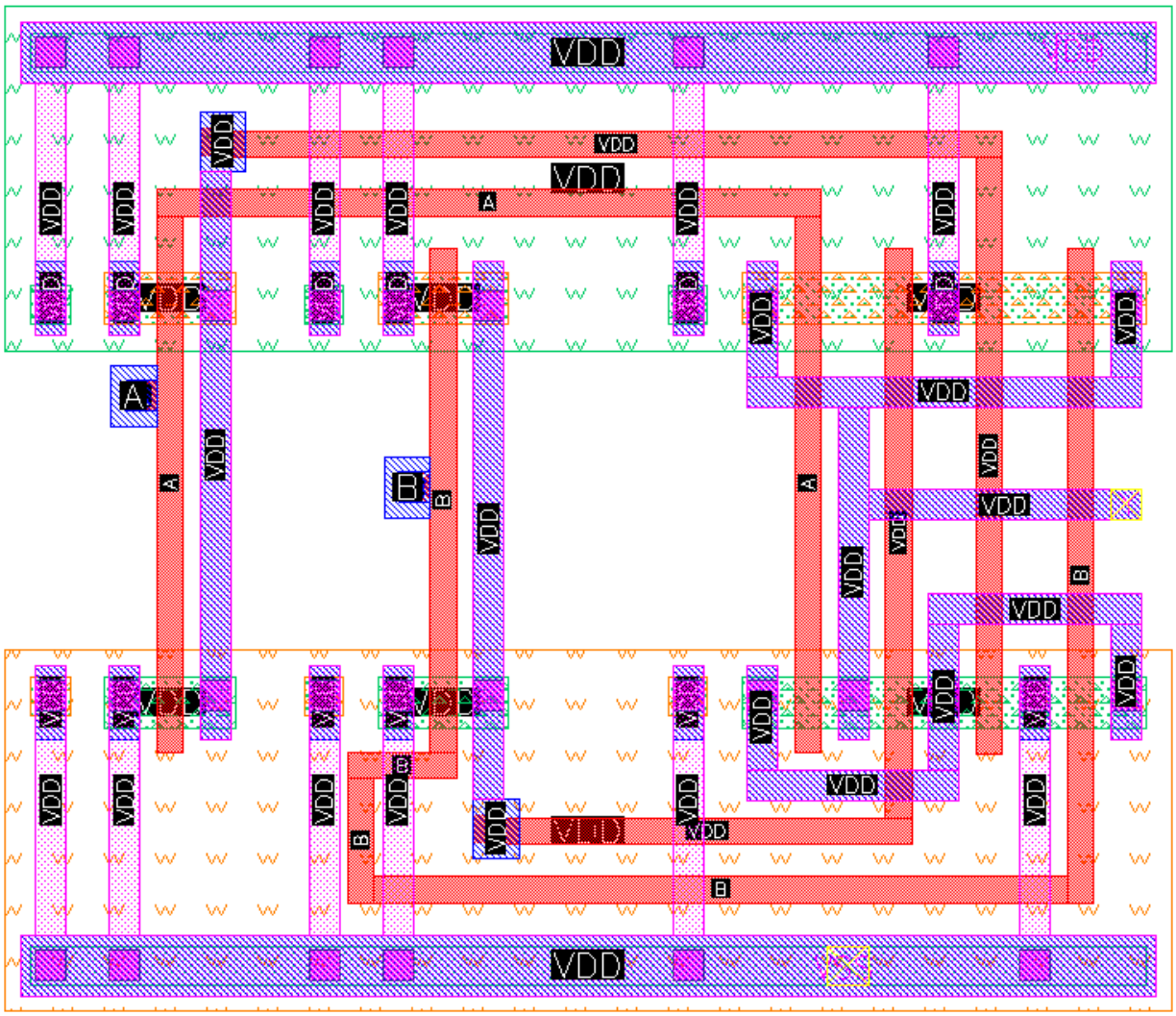


- XOR symbol:

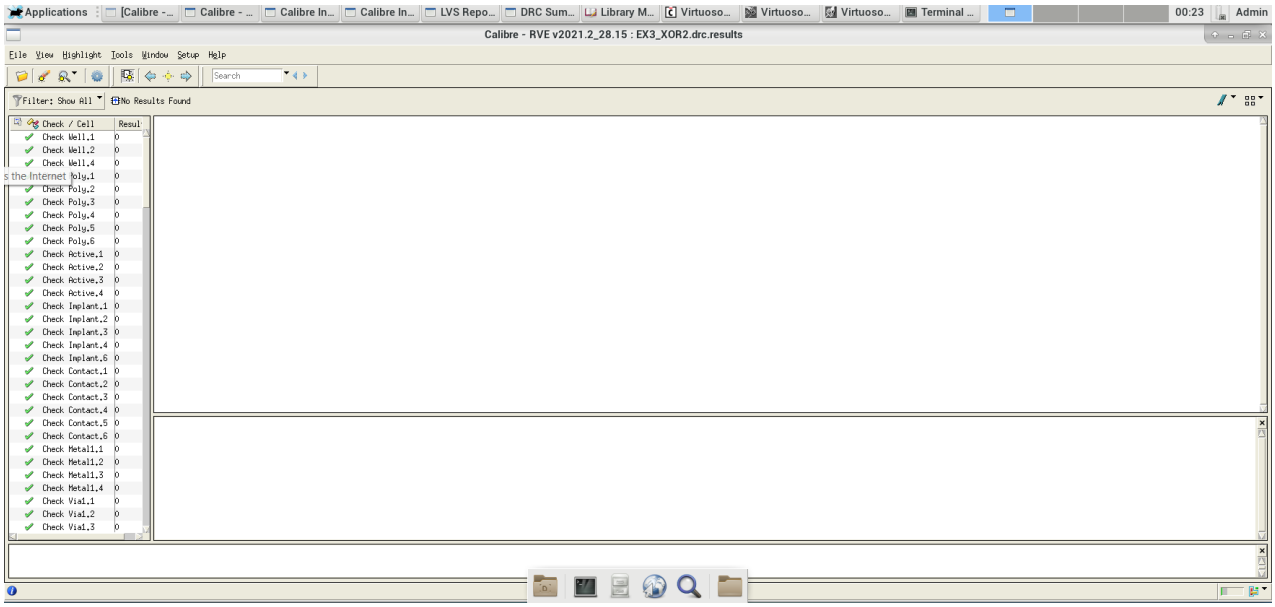


2. Layout

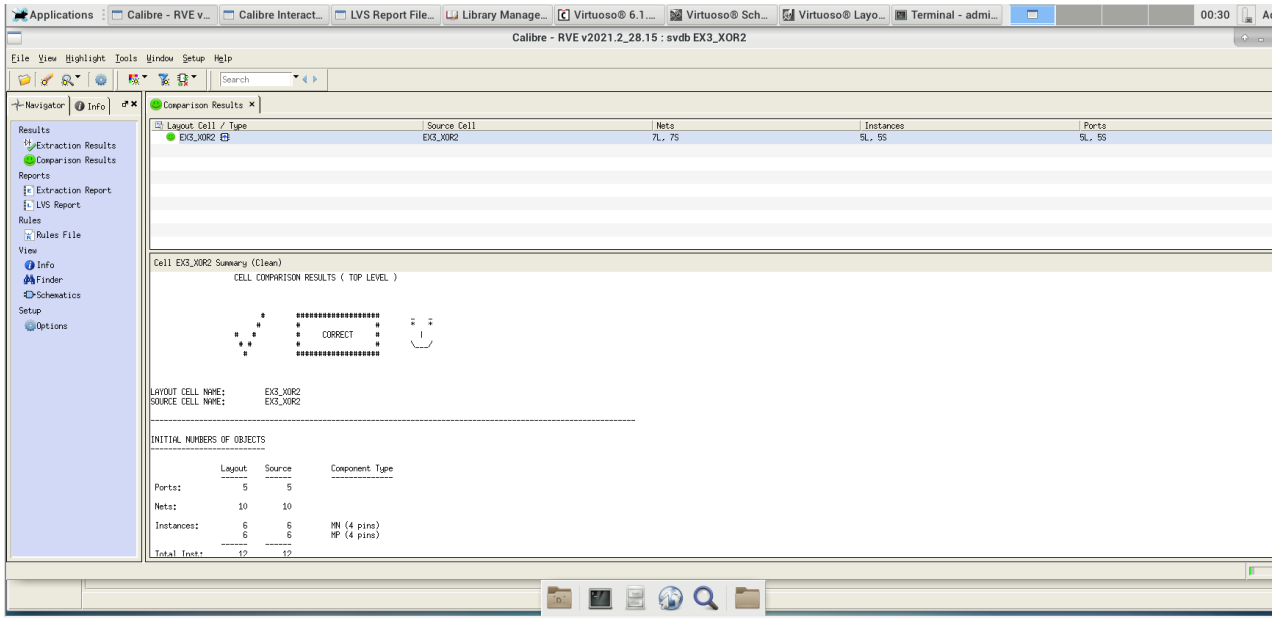
- XOR layout:



- XOR DRC:



- XOR LVS:



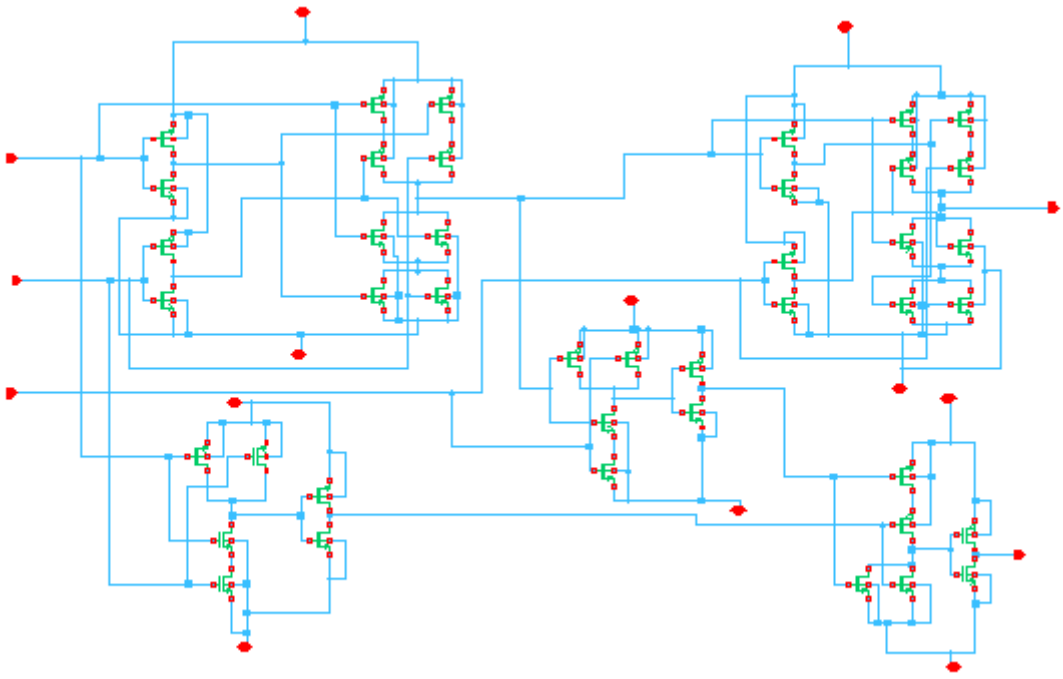
II. FULL ADDER 1-BIT

1. Truth table, schematic, symbol

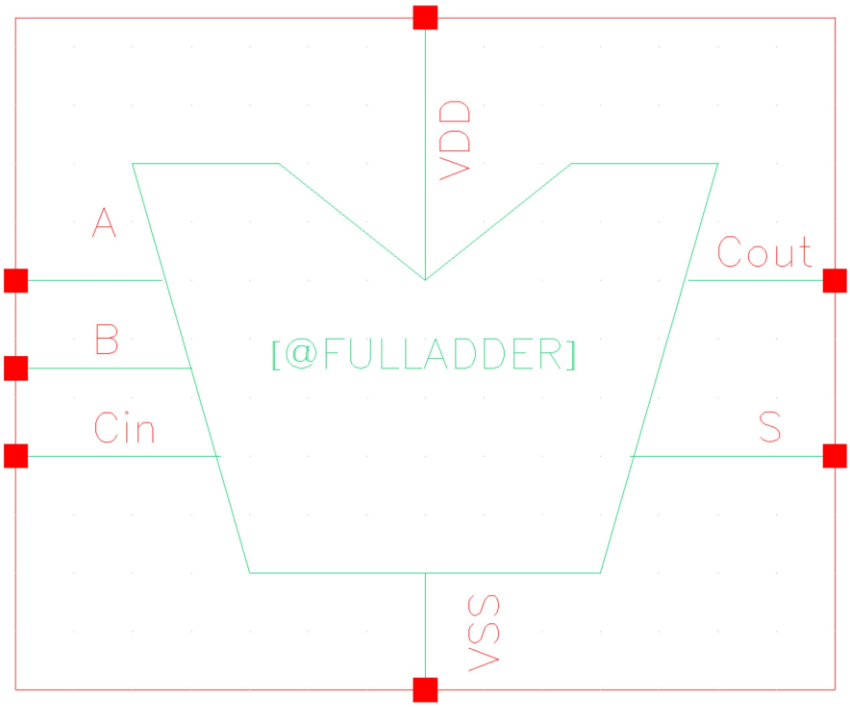
- Full adder 1-bit truth table:

Input			Ouput	
A	**B**	**Cin**	**Sum**	**Cout**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

- Full adder 1-bit schematic:

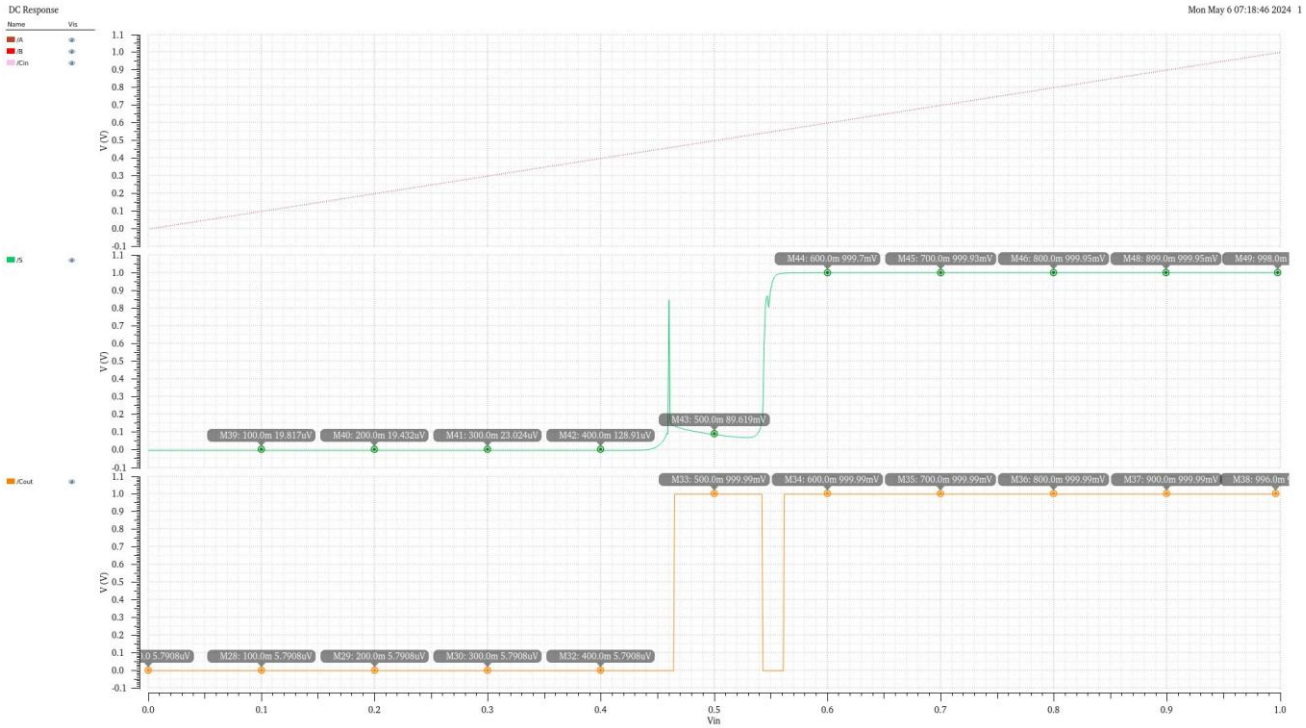


- Full adder 1-bit Symbol:

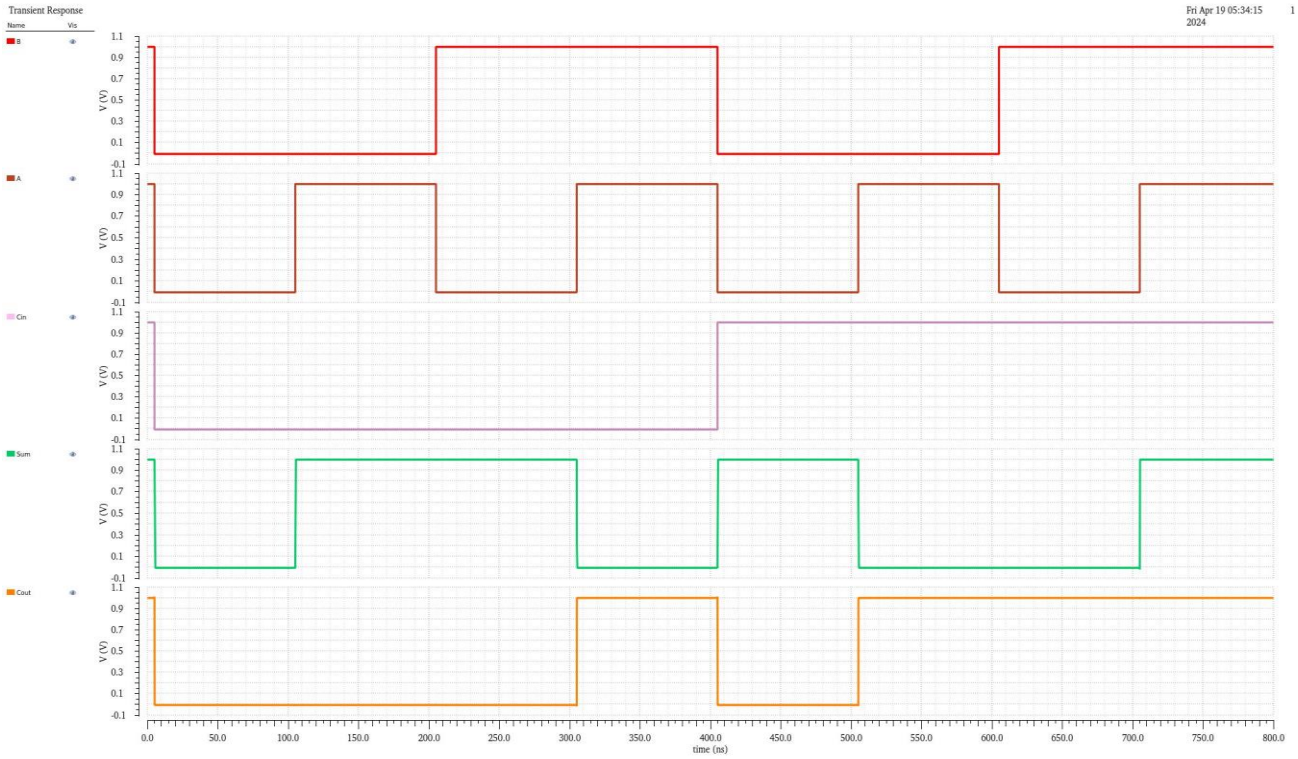


2. DC analysis, transient simulation

- Full adder 1-bit DC analysis:

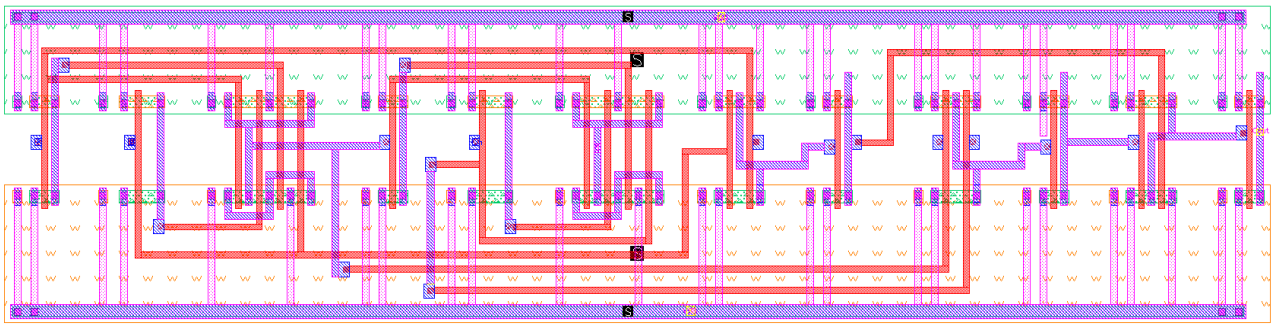


- Transient simulation

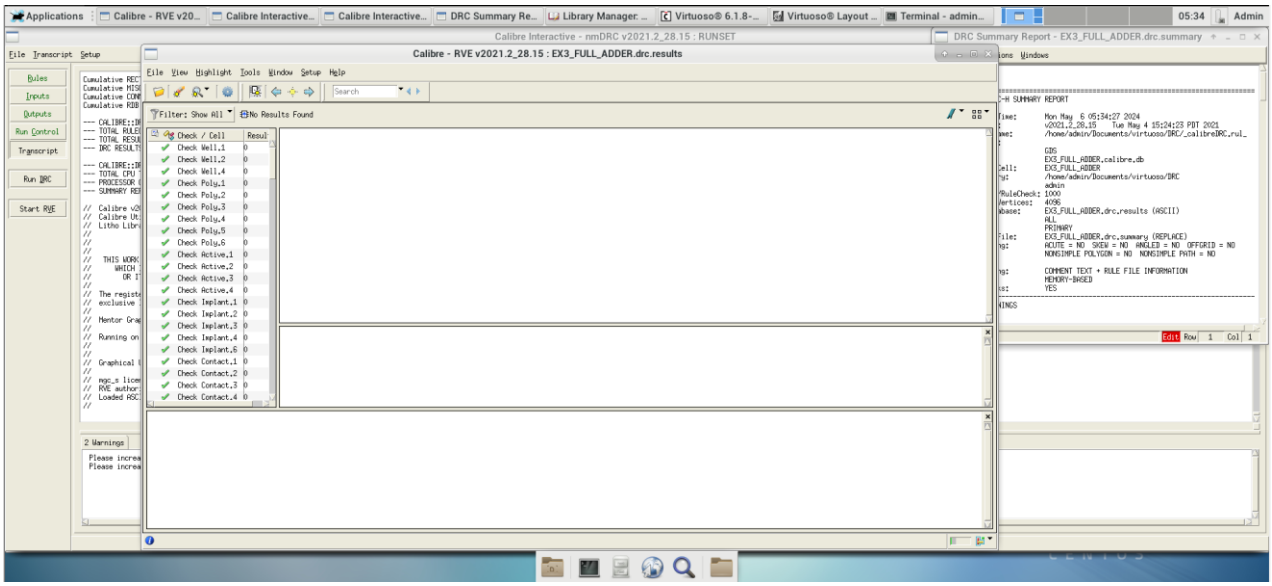


3. Layout

- Full adder 1-bit layout



- Full adder 1-bit check DRC



- Full adder 1-bit check LVS