ĐẠI HỌC QUỐC GIA THÀNH PHỐ HỒ CHÍ MINH
TRƯỜNG ĐẠI HỌC BÁCH KHOA
KHOA ĐIỆN – ĐIỆN TỬ

BÁO CÁO THÍ NGHIỆM THIẾT KẾ VI MẠCH
LAB 3: LOGIC SYNTHESIS AND VLSI FRONT-END FLOW

LỚP: L01 ---- NHÓM: 01

STT	Sinh viên thực hiện	Mã số sinh viên
1	Lê Quốc Thái	2114764
2	Nguyễn Khánh Huy	2113510
3	Nguyễn Thành Phát	2114378
4	Nguyễn Ngọc Kiều Duyên	2113053
5	Huỳnh Thịnh Phát	2114369

Thành phố Hồ Chí Minh – 2024

DANH SÁCH THÀNH VIÊN

STT	Sinh viên thực hiện	Mã số sinh viên	Đóng góp
1	Lê Quốc Thái	2114764	100%
2	Nguyễn Khánh Huy	2113510	100%
3	Nguyễn Thành Phát	2114378	100%
4	Nguyễn Ngọc Kiều Duyên	2113053	100%
5	Huỳnh Thịnh Phát	2114369	100%

MỤC LỤC

DANH SÁCH HÌNH ẢNH

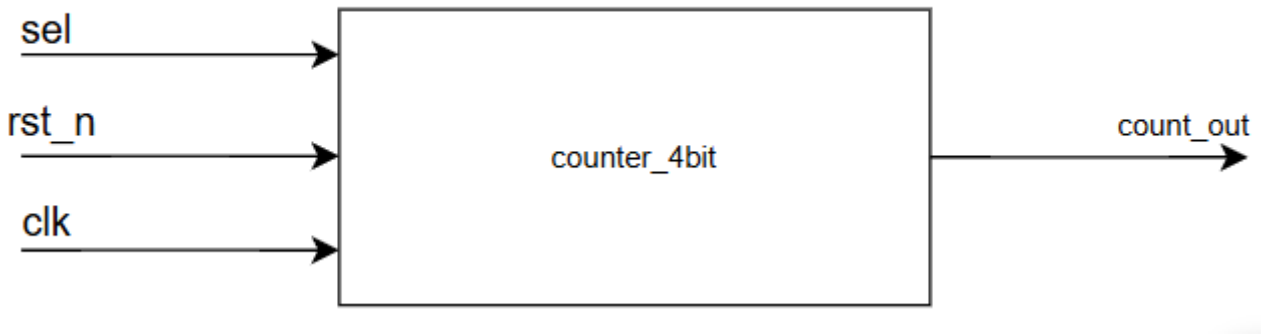
DANH SÁCH BẢNG

LAB 3: DESIGN AND SYNTHESIZE "4-BIT COUNTER"

Requirements

Design a 4-bit counter, sampled at the positive edge of clock signal, with an asynchronously active-low reset. When rst_ni asserted, the output is 0. It can either count up or count down based on the user's needs.

Block diagrams of the design



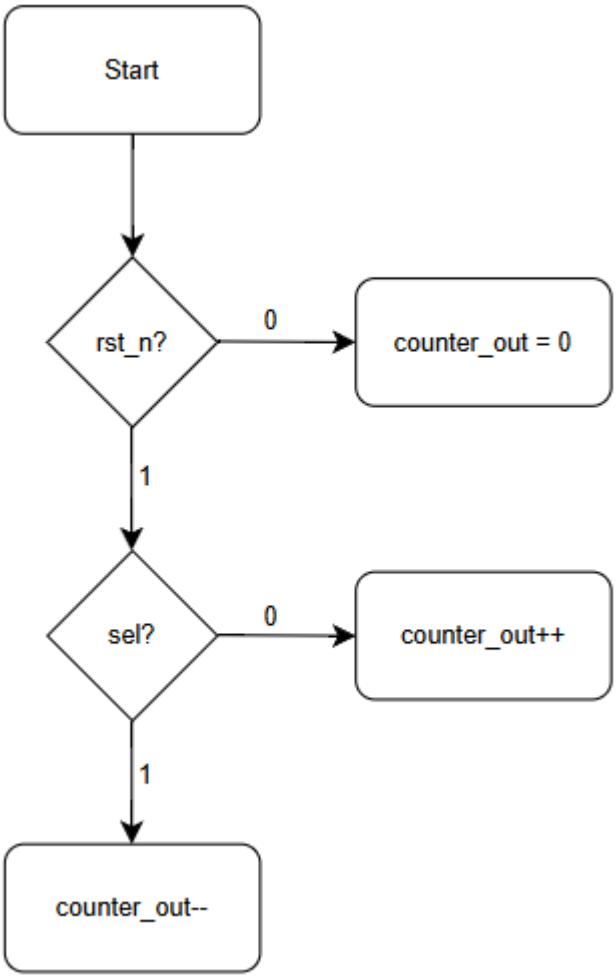
Hình 1: 4-bit counter Diagram

Port definations:

Signal	Width	Type	Description
clk_i	1	input	Positive clock signal
rst_ni	1	input	Negative edge reset. If rst_ni = 0, output will be set to 0. Else, it will start the normal operation
sel_i	1	input	Mode selection signal. If sel_i = 1, the design will start counting up else, it will staer counting down from the current output value.
counter_o	4	output	Result of the design

Bảng 1: Port definations

Flow chart of the design



Hình 2: Flow chart 4-bit counter

Timing report with frequency at 1GHz

```
set FREQ_GHz 1.0
Path 1: MET (0 ps) Setup Check with Pin out_reg[3]/CLK->D
Path 2: MET (80 ps) Late External Delay Assertion at pin out[2]
Path 3: MET (82 ps) Setup Check with Pin out_reg[2]/CLK->D
Path 4: MET (85 ps) Late External Delay Assertion at pin out[0]
Path 5: MET (99 ps) Late External Delay Assertion at pin out[1]
Path 6: MET (112 ps) Late External Delay Assertion at pin out[3]
Path 7: MET (157 ps) Setup Check with Pin out_reg[1]/CLK->D
Path 8: MET (434 ps) Setup Check with Pin out_reg[0]/CLK->D
```

Hình 3: Timing report

Total area

Instance	Cells	Cell Area	Net Area	Total Area
counter	19	205	98	303

Hình 4: Total area

Gates usage

```
          Gate             Instances   Area               Library
------------------------------------------------------------------------------
sky130_fd_sc_hd__clkinv_2           1    5.005    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__dfrtp_1            3   75.072    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__dfrtp_2            1   26.275    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__inv_2              2    7.507    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__nand2_1            3   11.261    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__nand2_2            1    6.256    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__nand3b_1           1    7.507    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__nor2_2             1    6.256    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__o2bb2ai_1          1    8.758    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__xnor2_1            2   17.517    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__xor2_1             2   17.517    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__xor2_2             1   16.266    sky130_fd_sc_hd__tt_025C_1v80
------------------------------------------------------------------------------
total                              19  205.197


   Type    Instances   Area  Area %
-------------------------------------
sequential         4 101.347   49.4
inverter           3  12.512    6.1
logic             12  91.338   44.5
-------------------------------------
total             19 205.197  100.0
```

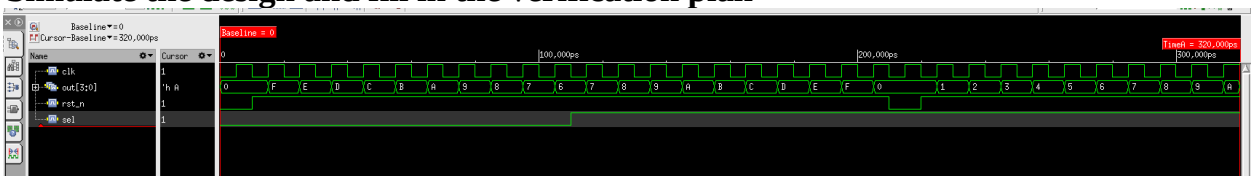
Hình 5: Gate usage

Verification plan

Section	Item	Description	Testcase name	Owner	Status
1	Reset	When rst_n is asserted, the output is 0, when rst_n is de-asserts, the output start to count up each positive edge of clock	cnt_rst_test	N1	PASS
2	Max count	When output is 4’b1111 and the counter is counting up, the next positive edge clock, output will be 4’b0000	cnt_max_count_test	N1	RUNNING
3	Min count	When output is 4’0000 and the counter is counting down, the next positive edge clock, output will be 4’b1111	cnt_min_count_test	N1	RUNNING
4	Count up Count down	When rst_n is de-asserts, the output start to count up is 4’b1010 then rst_n is asserts, when rst_n asserts counting down from 4’b1111	cnt_up_down_test	N1	RUNNING

Bảng 2: Verification plan

Simulate the design and fill in the verification plan



Hình 6: Waveform 4-bit counter

From #0 to #110, sel = 0, so ‘out’ decreases by 1 every 10 ps.

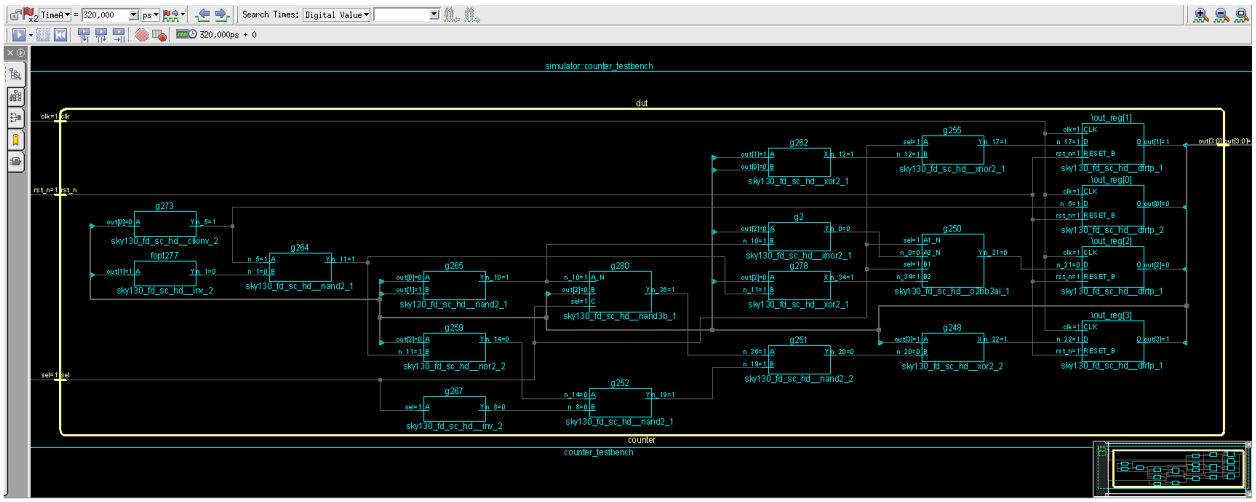
From #110 to #320, sel = 1, so ‘out’ increases by 1 every 10 ps.

At #210, rst_n = 0, so ‘out’ is set to 0.

Section	Item	Description	Testcase name	Owner	Status
1	Reset	When rst_n is asserted, the output is 0, when rst_n is de-asserts, the output start to count up each positive edge of clock	cnt_rst_test	N1	PASS
2	Max count	When output is 4’b1111 and the counter is counting up, the next positive edge clock, output will be 4’b0000	cnt_max_count_test	N1	PASS
3	Min count	When output is 4’0000 and the counter is counting down, the next positive edge clock, output will be 4’b1111	cnt_min_count_test	N1	PASS
4	Count up Count down	When rst_n is de-asserts, the output start to count up is 4’b1010 then rst_n is asserts, when rst_n asserts counting down from 4’b1111	cnt_up_down_test	N1	PASS

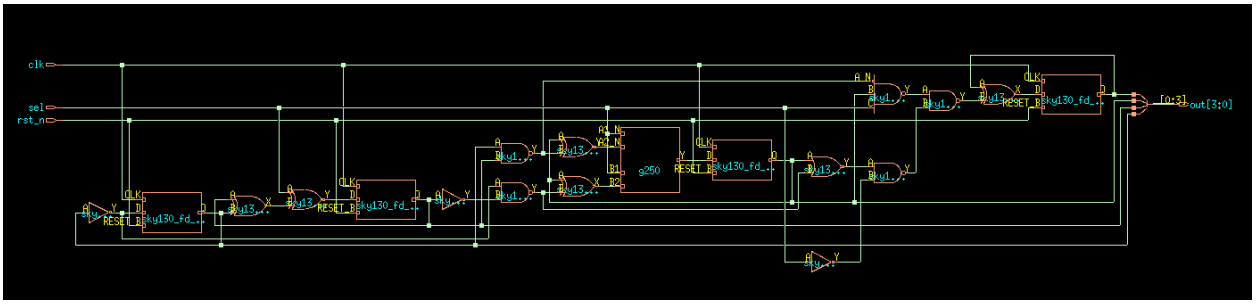
Bảng 3: Verification plan after test

RTL



Hình 7: RTL 4-bit counter

Netlist



Hình 8: Netlist 4-bit counter