ĐẠI HỌC QUỐC GIA THÀNH PHỐ HỒ CHÍ MINH
TRƯỜNG ĐẠI HỌC BÁCH KHOA
KHOA ĐIỆN – ĐIỆN TỬ

BÁO CÁO THÍ NGHIỆM THIẾT KẾ VI MẠCH

MINI PROJECT 3

LỚP: L01 ---- NHÓM: 01

STT	Sinh viên thực hiện	Mã số sinh viên
1	Lê Quốc Thái	2114764
2	Nguyễn Khánh Huy	2113510
3	Nguyễn Thành Phát	2114378
4	Nguyễn Ngọc Kiều Duyên	2113053
5	Huỳnh Thịnh Phát	2114369

Thành phố Hồ Chí Minh – 2024

DANH SÁCH THÀNH VIÊN

STT	Sinh viên thực hiện	Mã số sinh viên	Đóng góp
1	Lê Quốc Thái	2114764	100%
2	Nguyễn Khánh Huy	2113510	100%
3	Nguyễn Thành Phát	2114378	100%
4	Nguyễn Ngọc Kiều Duyên	2113053	100%
5	Huỳnh Thịnh Phát	2114369	100%

MỤC LỤC

DANH SÁCH HÌNH ẢNH

DANH SÁCH BẢNG

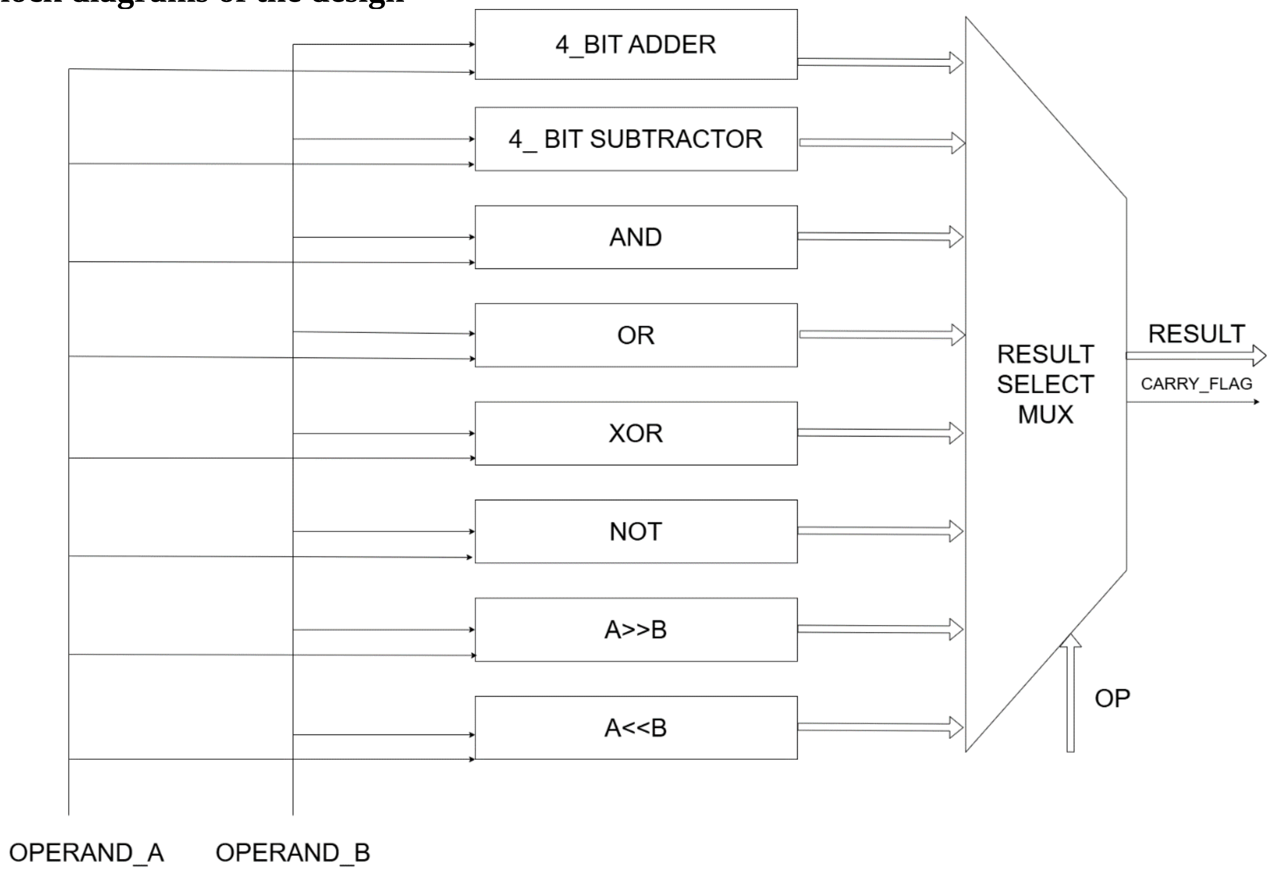
MINI PROJECT 3: DESIGN AND SYNTHESIZE ALU

Requirements

- Design a basic ALU, sampled at positive edge of clock, asynchronous reset, when reset is asserted, result is 0.

  The ALU can perform these operations:
- Addition, Subtraction
- Bitwise AND, OR, XOR, NOT
- Logical shift left, logical shift right.

Block diagrams of the design



Hình 1: ALU Diagram

Port definations

Signal	Width	Type	Description
clk_i	1	input	Positive clock signal
rst_ni	1	input	Negative edge reset. If rst_ni = 0, result and carry will be set to 0. Else, the design will work normally base on the input arguments
a_i	4	input	First argument
b_i	4	input	Second argument
op_i	3	input	Select the operation
result_o	4	output	Result of ALU
carry_o	1	output	Carry flag

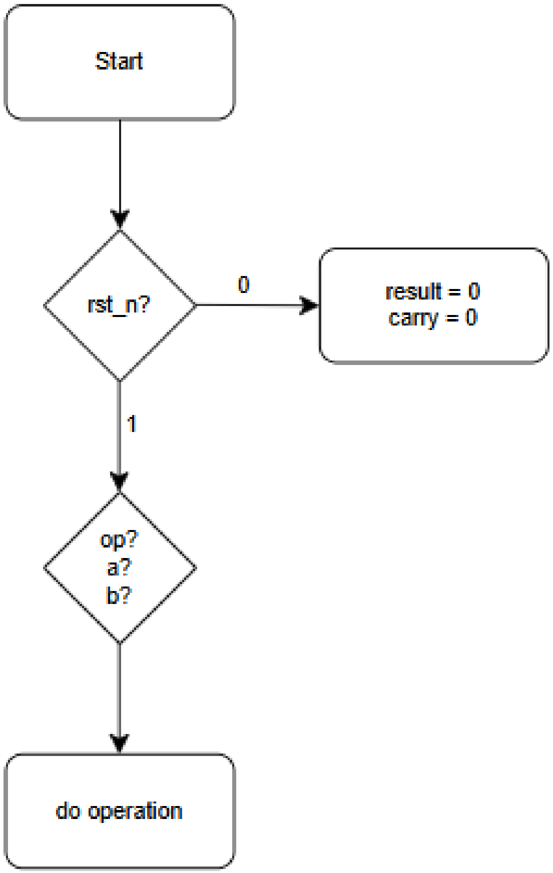
Bảng 1: Port definations

Below table is the detailed function of the ALU design

Operation (op_i)	Description
3’b000	{carry_o,result_o} = a_i + b_i
3’b001	{carry_o,result_o} = a_i - b_i
3’b010	carry_o = 0; result_o = and (a_i,b_i)
3’b011	carry_o = 0; result_o = or (a_i,b_i)
3’b100	carry_o = 0; result_o = xor (a_i,b_i)
3’b101	carry_o = 0; result_o = not (a_i)
3’b110	carry_o = 0; result_o = a_i >> b_i
3’b111	carry_o = 0; result_o = a_i << b_i

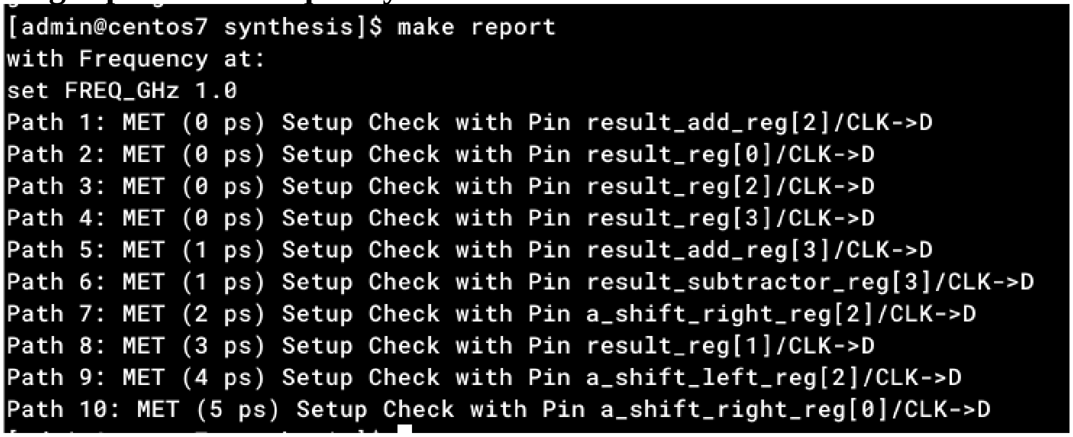
Bảng 2: Detail function of ALU

Flow chart of the design



Hình 2: ALU flow chart

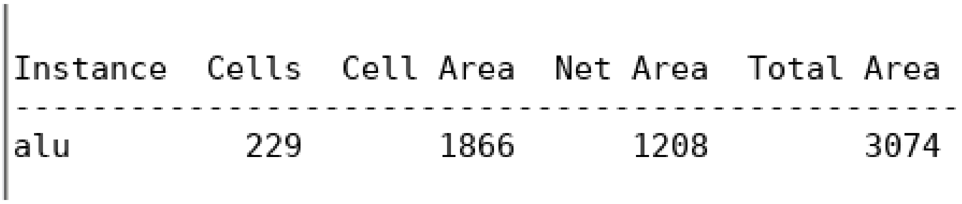
Timing report with frequency at 1GHz



```
[admin@centos7 synthesis]$ make report
with Frequency at:
set FREQ_GHz 1.0
Path 1: MET (0 ps) Setup Check with Pin result_add_reg[2]/CLK->D
Path 2: MET (0 ps) Setup Check with Pin result_reg[0]/CLK->D
Path 3: MET (0 ps) Setup Check with Pin result_reg[2]/CLK->D
Path 4: MET (0 ps) Setup Check with Pin result_reg[3]/CLK->D
Path 5: MET (1 ps) Setup Check with Pin result_add_reg[3]/CLK->D
Path 6: MET (1 ps) Setup Check with Pin result_subtractor_reg[3]/CLK->D
Path 7: MET (2 ps) Setup Check with Pin a_shift_right_reg[2]/CLK->D
Path 8: MET (3 ps) Setup Check with Pin result_reg[1]/CLK->D
Path 9: MET (4 ps) Setup Check with Pin a_shift_left_reg[2]/CLK->D
Path 10: MET (5 ps) Setup Check with Pin a_shift_right_reg[0]/CLK->D
```

Hình 3: Timing report

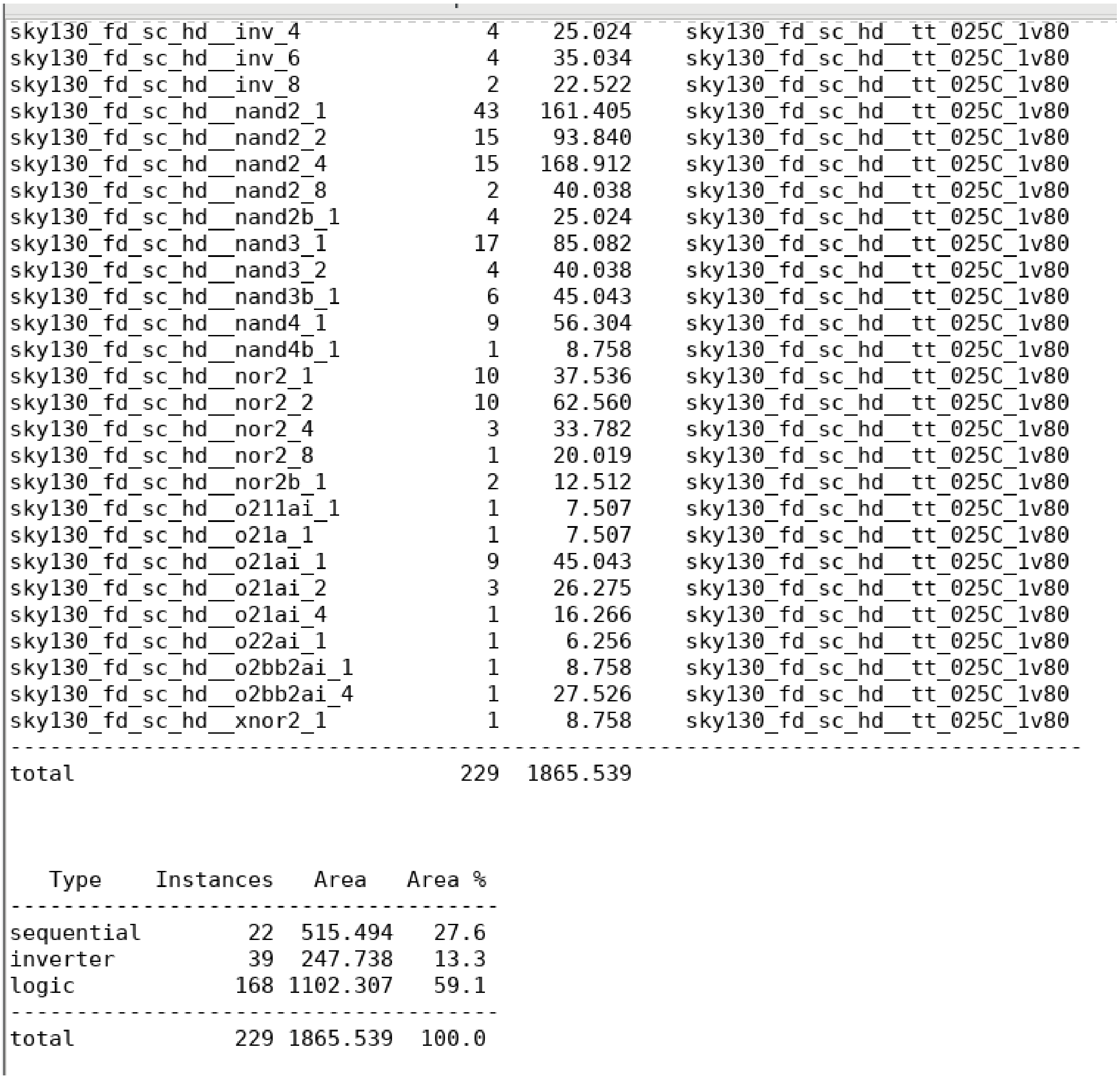
Total area



```
Instance  Cells  Cell Area  Net Area  Total Area
-------------------------------------------------
alu         229       1866      1208        3074
```

Hình 4: Total area

Gates usage



```
sky130_fd_sc_hd__inv_4              4    25.024    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__inv_6              4    35.034    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__inv_8              2    22.522    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__nand2_1           43   161.405    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__nand2_2           15    93.840    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__nand2_4           15   168.912    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__nand2_8            2    40.038    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__nand2b_1           4    25.024    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__nand3_1           17    85.082    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__nand3_2            4    40.038    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__nand3b_1           6    45.043    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__nand4_1            9    56.304    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__nand4b_1           1     8.758    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__nor2_1            10    37.536    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__nor2_2            10    62.560    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__nor2_4             3    33.782    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__nor2_8             1    20.019    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__nor2b_1            2    12.512    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__o211ai_1           1     7.507    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__o21a_1             1     7.507    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__o21ai_1            9    45.043    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__o21ai_2            3    26.275    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__o21ai_4            1    16.266    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__o22ai_1            1     6.256    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__o2bb2ai_1          1     8.758    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__o2bb2ai_4          1    27.526    sky130_fd_sc_hd__tt_025C_1v80
sky130_fd_sc_hd__xnor2_1            1     8.758    sky130_fd_sc_hd__tt_025C_1v80
---------------------------------------------------------------------------------
total                             229  1865.539


   Type    Instances   Area   Area %
-------------------------------------
sequential        22  515.494   27.6
inverter          39  247.738   13.3
logic            168 1102.307   59.1
-------------------------------------
total            229 1865.539  100.0
```

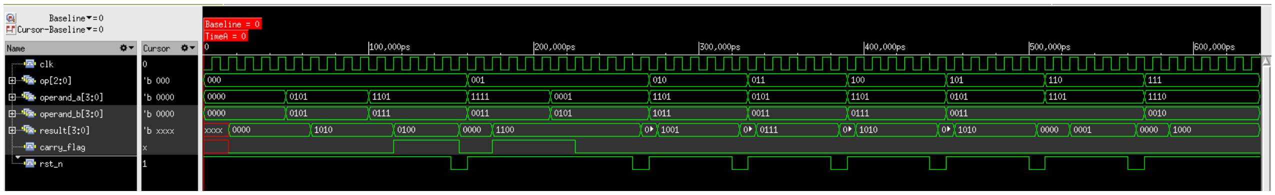
Hình 5: Gate usage

Verification plan

Section	Item	Description	Testcase name	Owner	Status
1	Reset	When rst_ni asserted, the output is 0, when it de-asserts, the design will work normally	rst_test	N1	PASS
2	Operation test	When op_i is set 3’b000 to 3’b111. At the same 2 arguments. Check the result_o and carry_o. The argument will be a_i = 4’b1011 and b_i = 4’b0100	operation_test	N1	RUNNING
3	Carry test	The argument will be a_i = 4’b1111 and b_i = 4’b1111. The op_ i= 3’b000 and 3’b001. Check the result_o and carry_o	cary_test	N1	RUNNING

Bảng 3: Verification plan

Simulate the design and fill in the verification plan



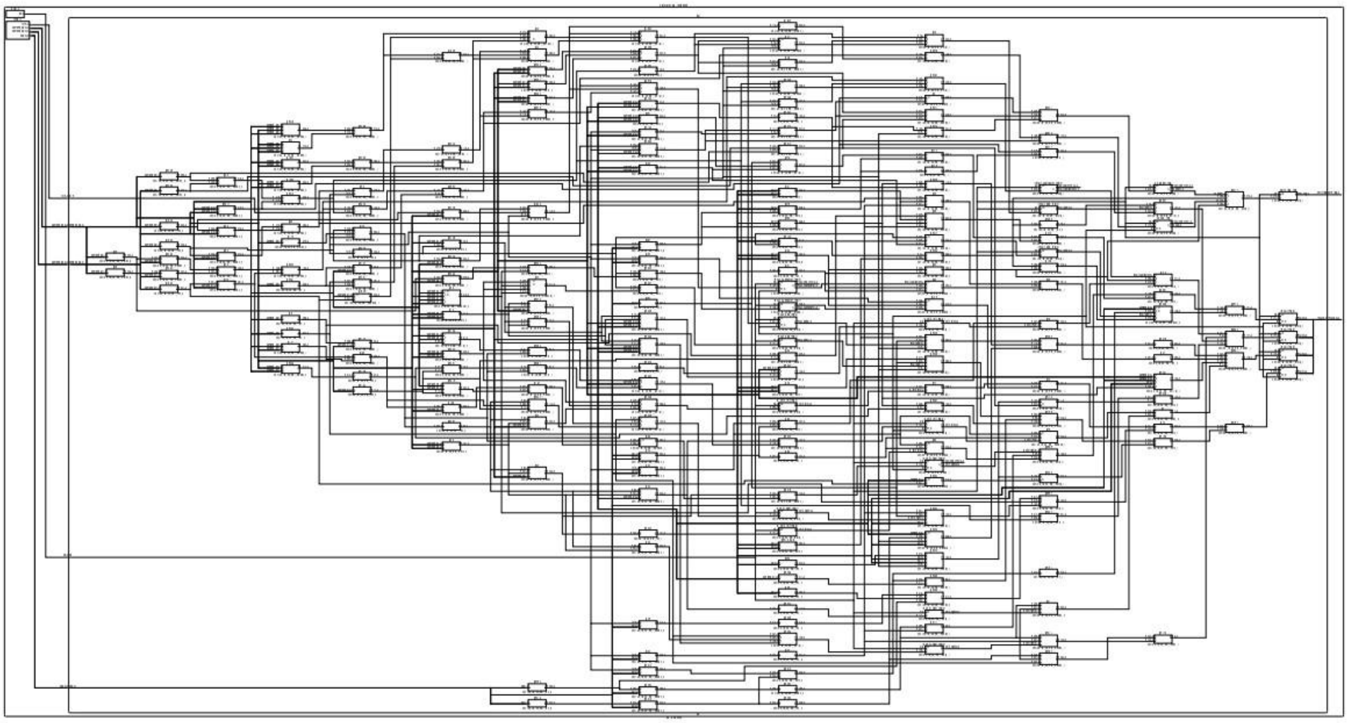
Hình 6: Waveform ALU

Section	Item	Description	Testcase name	Owner	Status
1	Reset	When rst_ni asserted, the output is 0, when it de-asserts, the design will work normally	rst_test	N1	PASS
2	Operation test	When op_i is set 3’b000 to 3’b111. At the same 2 arguments. Check the result_o and carry_o. The argument will be a_i = 4’b1011 and b_i = 4’b0100	operation_test	N1	PASS

3	Carry test	The argument will be a_i = 4’b1111 and b_i = 4’b1111. The op_ i= 3’b000 and 3’b001. Check the result_o and carry_o	cary_test	N1	PASS

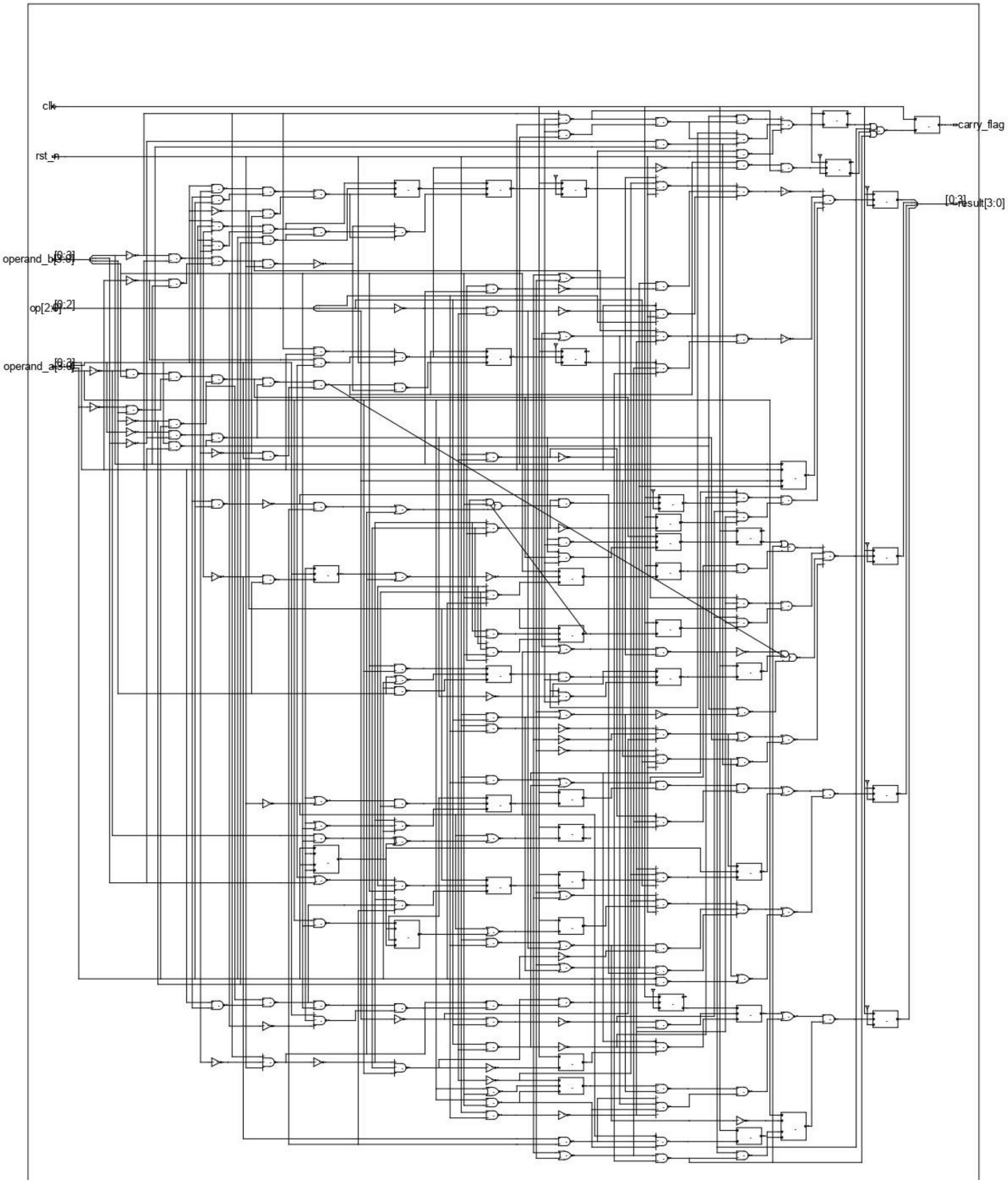
Bảng 4: Verification plan after test

RTL



Hình 7: RTL of ALU

Netlist



Hình 8: Netlist of ALU