DS14C232 Low Power +5V Powered TIA/EIA-232 Dual Driver/Receiver

Check for Samples: DS14C232

FEATURES

- **Pin compatible with industry standard MAX232, LT1081, ICL232 and TSC232**
- **Single +5V power supply**
- **Low power—I_{CC} 3.0 mA maximum**
- **DS14C232C meets TIA/EIA-232-E (RS-232) and CCITT V.28 standards**
- **CMOS technology**
- **Receiver Noise Filter**
- **Package efficiency—2 drivers and 2 receivers**
- **Available in Plastic DIP, Narrow and Wide SOIC packages**
- **TIA/EIA-232 compatible extended temperature range option:**
  - **DS14C232T −40°C to +85°C**
  - **DS14C232E/J: −55°C to +125°C**

DESCRIPTION

The DS14C232 is a low power dual driver/receiver featuring an onboard DC to DC converter, eliminating the need for ±12V power supplies. The device only requires a +5V power supply. I_{CC} is specified at 3.0 mA maximum, making the device ideal for battery and power conscious applications. The drivers' slew rate is set internally and the receivers feature internal noise filtering, eliminating the need for external slew rate and filter capacitors. The device is designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). The driver inputs and receiver outputs are TTL and CMOS compatible. DS14C232C driver outputs and receiver inputs meet TIA/EIA-232-E (RS-232) and CCITT V.28 standards.

Connection Diagram

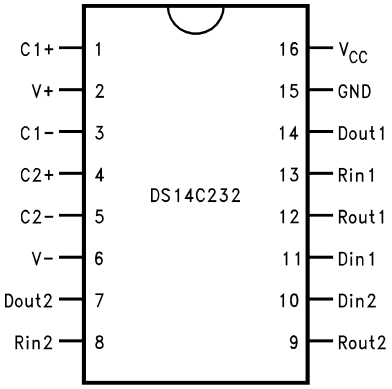


Figure 1. Top View

Functional Diagram

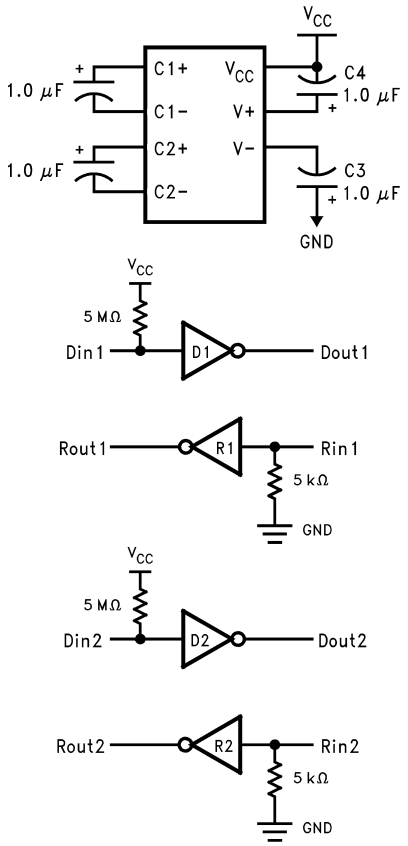


Figure 2. Functional Block Diagram

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Specifications for the 883 version of this product are listed separately on the following pages.

Absolute Maximum Ratings (1)

Supply Voltage, V_{CC}	−0.3V to 6V
V^+ Pin	(V_{CC} − 0.3)V to +14V
V^- Pin	+0.3V to −14V
Driver Input Voltage	−0.3V to (V_{CC} + 0.3V)
Driver Output Voltage	(V^+ + 0.3V) to (V^- − 0.3V)
Receiver Input Voltage	±25V
Receiver Output Voltage	−0.3V to (V_{CC} + 0.3V)
Junction Temperature	+150°C
Maximum Package Power Dissipation @ 25°C (2)	
N Package	1698 mW
M Package	1156 mW
Short Circuit Duration, D_{OUT}	Continuous
Storage Temp. Range	−65°C to +150°C
Lead Temp. (Soldering, 4 sec.)	+260°C
ESD Rating	
(HBM, 1.5 kΩ, 100 pF)	≥ 2.5 kV

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.
(2) Ratings apply to ambient temperature at +25°C. Above this temperature derate: N Package 15.6 mW/°C, and M Package 10.6 mW/°C.

Recommended OperatingConditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Operating Free Air Temp. (T_A)			
DS14C232C	0	+70	°C
DS14C232T	−40	+85	°C

Electrical Characteristics (1)

Over recommended operating conditions, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DC TO DC CONVERTER CHARACTERISTICS							
V^+	Positive Power Supply	R_L = 3 kΩ, C1–C4 = 1.0 µF, D_{IN} = 0.8V			9.0		V
V^-	Negative Power Supply	R_L = 3 kΩ, C1–C4 = 1.0 µF, D_{IN} = 2.0V			−8.5		V
I_{CC}	Supply (V_{CC}) Current	No Load			1.0	3.0	mA
DRIVER CHARACTERISTICS							
V_{IH}	High Level Input Voltage			2		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IH}	High Level Input Current	V_{IN} ≥ 2.0V		−10		+10	µA
I_{IL}	Low Level Input Current	V_{IN} ≤ 0.8V		−10		+10	µA
V_{OH}	High Level Output Voltage	R_L = 3 kΩ		5.0	8.0		V
V_{OL}	Low Level Output Voltage	R_L = 3 kΩ			−7.0	−5.0	V
I_{OS+}	Output High Short Circuit Current	V_O = 0V, V_{IN} = 0.8V(2)		−30	−15	−5.0	mA
I_{OS-}	Output Low Short Circuit Current	V_O = 0V, V_{IN} = 2V(2)		5.0	11	30	mA
R_O	Output Resistance	−2V ≤ V_O ≤ +2V,		300			Ω
		V_{CC} = 0V = GND					
RECEIVER CHARACTERISTICS							
V_{TH}	Input High Threshold Voltage	V_{CC} = 5.0V			1.9	2.4	V
		V_{CC} = 5.0V ±10%			1.9	2.6	V
V_{TL}	Input Low Threshold Voltage			0.8	1.5		V
V_{HY}	Hysteresis			0.2	0.4	1.0	V
R_{IN}	Input Resistance		−15V ≤ V_{IN} ≤ +15V	3.0	4.7	7.0	kΩ
I_{IN}	Input Current	V_{IN} = +15V		+2.14	+3.75	+5.0	mA
		V_{IN} = +3V		+0.43	+0.64	+1.0	mA
		V_{IN} = −3V		−1.0	−0.64	−0.43	mA
		V_{IN} = −15V		−5.0	−3.75	−2.14	mA
V_{OH}	High Level Output Voltage	V_{IN} = −3V, I_O = −3.2 mA		3.5	4.5		V
		V_{IN} = −3V, I_O = −20 µA		4.0	4.9		V
V_{OL}	Low Level Output Voltage	V_{IN} = +3V, I_O = +3.2 mA			0.15	0.4	V

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

(2) IOS_+ and IOS_- values are for one output at a time. If more than one output is shorted simultaneously, the device power dissipation may be exceeded.

Switching Characteristics

Over recommended operating conditions, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
t_{PLH}	Propagation Delay Low to High	R_L = 3 kΩ C_L = 50 pF	Figure 4 and Figure 5		1.0	4.0	µs
t_{PHL}	Propagation Delay High to Low				1.0	4.0	µs
t_{SK}	Skew $\|t_{PLH} - t_{PHL}\|$				0.1	1.0	µs
SR1	Output Slew Rate (1)	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF		4.0		30	V/µs
SR2	Output Slew Rate (1)	R_L = 3 kΩ, C_L = 2500 pF			4.5		V/µs
RECEIVER CHARACTERISTICS							
t_{PLH}	Propagation Delay Low to High	Input Pulse Width > 10 µs			2.9	6.5	µs
t_{PHL}	Propagation Delay High to Low	C_L = 50 pF			2.5	6.5	µs
t_{SK}	Skew $\|t_{PLH} - t_{PHL}\|$	(Figure 6 Figure 7)			0.4	2.0	µs
t_{nw}	Noise Pulse Width Rejected	(Figure 6 Figure 7)			0.7	0.5	µs

(1) Slew rate is defined as ΔV/Δt, measured between ±3V level.

For complete Military Product Specifications, refer to the appropriate SMD or MDS.

Absolute Maximum Ratings (1)

Supply Voltage, V_{CC}	−0.3V to 6V
V^+ Pin	(V_{CC} − 0.3)V to +14V
V^- Pin	+0.3V to −14V
Driver Input Voltage	−0.3V to (V_{CC} + 0.3V)
Driver Output Voltage	(V^+ + 0.3V) to (V^- − 0.3V)
Receiver Input Voltage	±25V
Receiver Output Voltage	−0.3V to (V_{CC} + 0.3V)
Maximum Package Power Dissipation @ 25°C (2)	
J Package	1520 mW
E Package	2000 mW
Short Circuit Duration, D_{OUT}	Continuous
Storage Temp. Range	−65°C to +150°C
Lead Temp. (Soldering, 4 sec.)	+260°C
ESD Rating	
(HMB, 1.5 kΩ, 100 pF)	≥ 2.5 kV

(1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of “Electrical Characteristics” specify conditions for device operation.

(2) Ratings apply to ambient temperature at +25°C. Above this temperature derate: J Package 12.2 mW/°C and E Package 13.3 mW/°C.

Recommended OperatingConditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Operating Free Air Temp. (T_A)			
DS14C232E/J	−55	+125	°C

Electrical Characteristics (1)

Over recommended operating conditions, unless otherwise specified

Symbol	Parameter	Conditions		Min	Max	Units
DEVICE CHARACTERISTICS (C1–C4 = 1.0 µF)						
I_{CC}	Supply (V_{CC}) Current	No Load			8.0	mA
DRIVER CHARACTERISTICS						
V_{IH}	High Level Input Voltage			2		V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IH}	High Level Input Current	$V_{IN} \geq 2.0V$			100	µA
I_{IL}	Low Level Input Current	$V_{IN} = 0V$			100	µA
V_{OH}	High Level Output Voltage	$R_L = 3\ k\Omega$		5.0		V
V_{OL}	Low Level Output Voltage	$R_L = 3\ k\Omega$			−5.0	V
I_{OS+}	Output High Short Circuit Current	$V_O = 0V$	(2)	−25		mA
I_{OS-}	Output Low Short Circuit Current	$V_O = 0V$			25	mA
R_O	Output Resistance	$-2V \leq V_O \leq +2V$, $T_A = 25°C$,		300		Ω
		$V_{CC} = 0V = GND$				
RECEIVER CHARACTERISTICS (C1–C4 = 1.0 µF)						
V_{TH}	Input High Threshold Voltage				3.0	V
V_{TL}	Input Low Threshold Voltage			0.2		V
V_{HY}	Hysteresis	$T_A = 25°C$, $+125°C$		0.1	1.0	V
		$T_A = -55°C$		0.05	1.0	V
R_{IN}	Input Resistance	$V_{IN} = \pm 3V$ and $\pm 15V$, $T_A = 25°C$		3.0	7.0	kΩ
V_{OH}	High Level Output Voltage	$I_O = -3.2$ mA		3.5		V
		$I_O = -20$ µA		4.0		V
V_{OL}	Low Level Output Voltage	$I_O = +3.2$ mA			0.4	V

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

(2) IOS_+ and IOS_- values are for one output at a time. If more than one output is shorted simultaneously, the device power dissipation may be exceeded.

Switching Characteristics

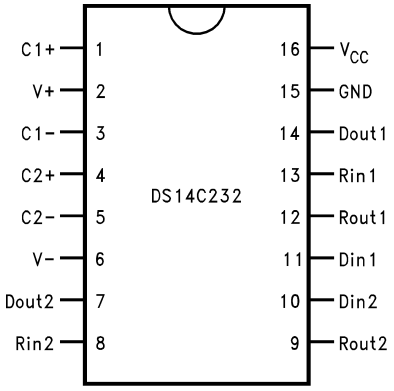
Over recommended operating conditions, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Units
DRIVER CHARACTERISTICS (C1–C4 = 1.0 µF)						
t_{PLH}	Propagation Delay Low to High	R_L = 3 kΩ, C_L = 50 pF	Figure 4 Figure 5		4.0	µs
t_{PHL}	Propagation Delay High to Low				4.0	µs
t_{SK}	Skew $\|t_{PLH} - t_{PHL}\|$				1.0	µs
SR1	Output Slew Rate	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF	(1)	1.5	30	V/µs
RECEIVER CHARACTERISTICS (C1–C4 = 1.0 µF)						
t_{PLH}	Propagation Delay Low to High	Input Pulse Width > 10 µs			8.0	µs
t_{PHL}	Propagation Delay High to Low	C_L = 50 pF			8.0	µs
t_{SK}	Skew $\|t_{PLH} - t_{PHL}\|$	(Figure 6 Figure 7)			2.0	µs

(1) Slew rate is defined as ΔV/Δt, measured between ±3V level.

Connection Diagrams

J Package
16-Lead Dual-In-line Package



E Package
20-Lead Ceramic Leadless Chip Carrier

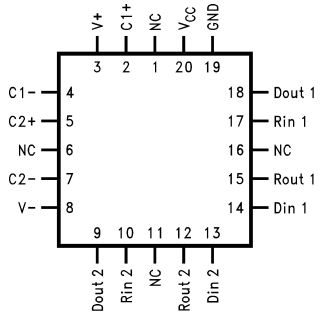


Figure 3. For Complete Military Product Specifications See MDS or SMD

Parameter Measurement Information

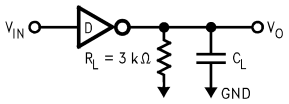


Figure 4. Driver Load Circuit

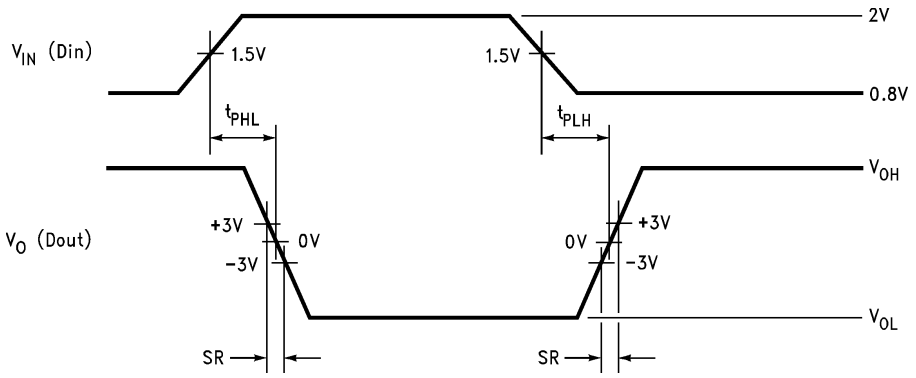


Figure 5. Driver Switching Waveform

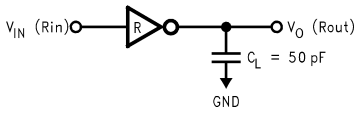


Figure 6. Receiver Load Circuit

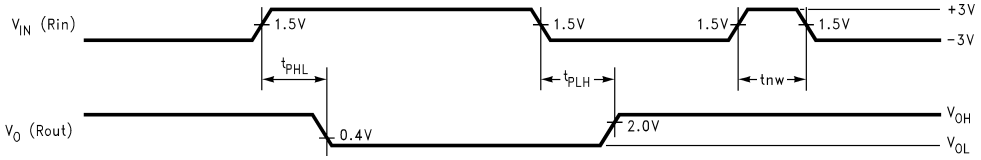


Figure 7. Receiver Propagation Delays and Noise Rejection (2)

Pin Functions

Pin Descriptions

V_{CC} (Pin 16)

Power supply pin for the device, +5V (±10%).

V+ (Pin 2)

Positive supply for TIA/EIA-232-E drivers. Recommended external capacitor: C4-1.0 µF (6.3V). Capacitor value should be larger than 1 µF. This supply is not intended to be loaded externally.

V− (Pin 6)

Negative supply for TIA/EIA-232-E drivers. Recommended external capacitor: C3-1.0 µF (16V). Capacitor value should be larger than 1 µF. This supply is not intended to be loaded externally.

C1+, C1− (Pins 1, 3)

External capacitor connection pins. Recommended capacitor: 1.0 µF (6.3V). Capacitor value should be larger than 1 µF.

C2+, C2− (Pins 4, 5)

External capacitor connection pins. Recommended capacitor: 1.0 µF (16V). Capacitor value should be greater than 1 µF.

D_{IN}1, D_{IN}2 (Pins 11, 10)

Driver input pins are TTL/CMOS compatible. Inputs of unused drivers may be left open, an internal active pull-up resistor (500 kΩ minimum, typically 5 MΩ) pulls input HIGH. Output will be LOW for open inputs.

D_{OUT}1, D_{OUT}2 (Pins 14, 7)

Driver output pins conform to TIA/EIA-232-E levels.

(2) Receiver AC input waveform for test purposes: $t_r = t_f$ = 200 ns, V_{IH} = 3V, V_{IL} = −3V, f = 30 kHz.

Pin Descriptions (continued)

$R_{IN}1$, $R_{IN}2$ (Pins 13, 8)

Receiver input pins accept TIA/EIA-232-E input voltages (±25V). Receivers feature a noise filter and guaranteed hysteresis of 100 mV. Unused receiver input pins may be left open. Internal input resistor 4.7 kΩ pulls input low, providing a failsafe high output.

$R_{OUT}1$, $R_{OUT}2$ (Pins 12, 9)

Receiver output pins are TTL/CMOS compatible. Receiver output HIGH voltage is specified for both CMOS and TTL load conditions.

GND (Pin 15)

Ground Pin.

Typical Application Information

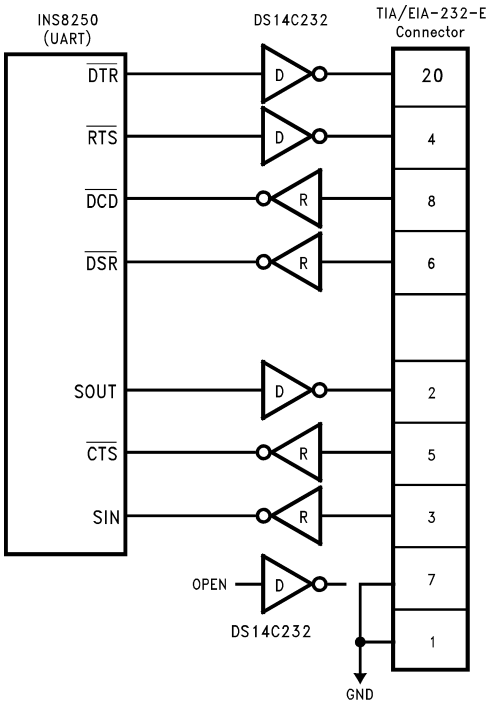


Figure 8. Application of DS14C232 and INS8250

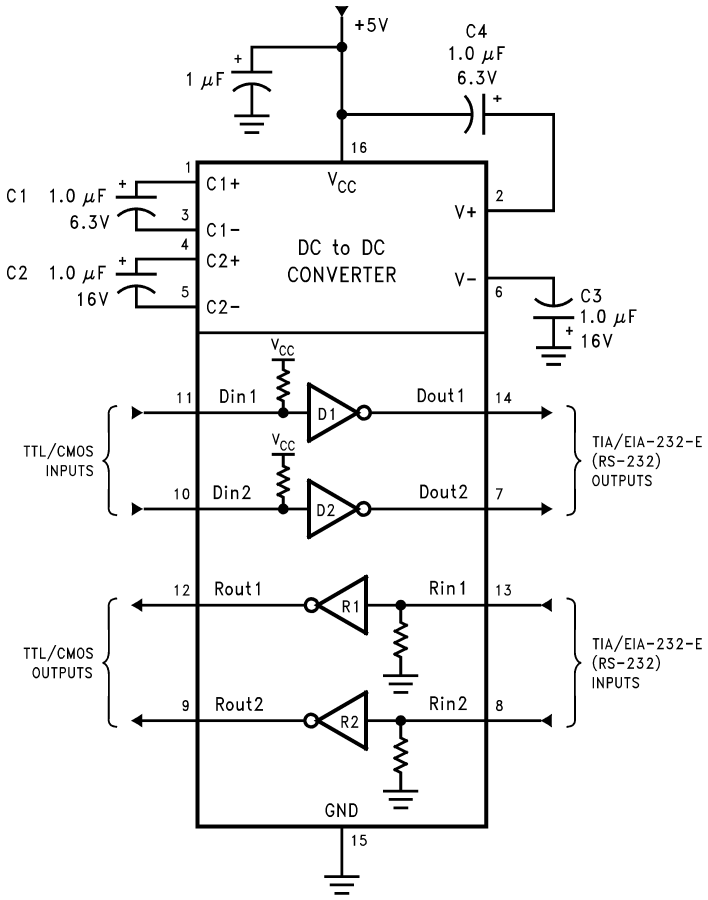
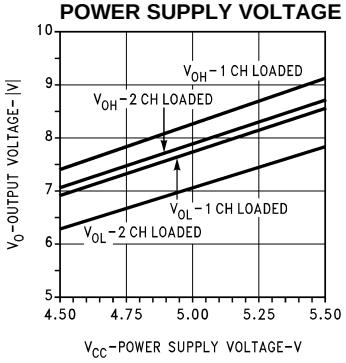


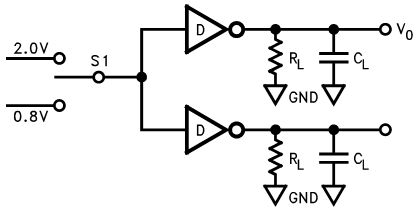
Figure 9. Typical Connection Diagram

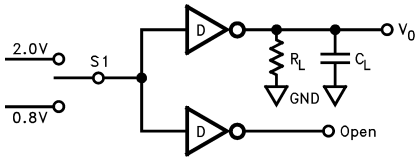
Typical Performance Characteristics

DRIVER V_{OH} & V_{OL} vs POWER SUPPLY VOLTAGE



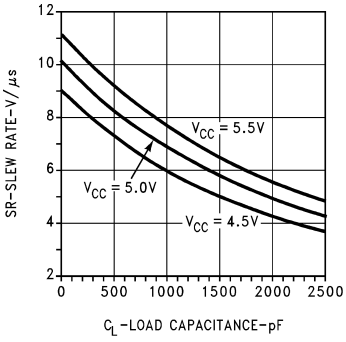
V_{CC} = 5.0V, R_L = 3 kΩ, C_L = 15 pF (includes jig and probe capacitance), C_P = 1 µF





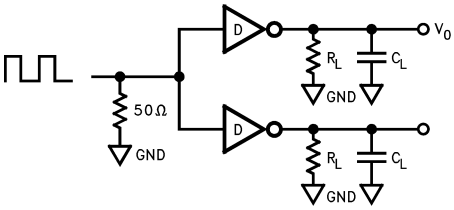
S1	V_O
2.0V	V_{OL}
0.8V	V_{OH}

DRIVER SLEW RATE vs POWER SUPPLY VOLTAGE & LOAD CAPACITANCE



T_a = 25°C, R_L = 5 kΩ, C_P = 1 µF, f = 30 KHz

SR = 6V/t1 or 6V/t2, whichever is greater.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DS14C232CM	ACTIVE	SOIC	D	16	48	TBD	CU SNPB	Level-1-235C-UNLIM	
DS14C232CM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
DS14C232CMX	ACTIVE	SOIC	D	16	2500	TBD	CU SNPB	Level-1-235C-UNLIM	
DS14C232CMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
DS14C232CN	ACTIVE	PDIP	NFG	16	25	TBD	Call TI	Level-1-NA-UNLIM	
DS14C232CN/NOPB	ACTIVE	PDIP	NFG	16	25	Pb-Free (RoHS)	Call TI	Level-1-NA-UNLIM	
DS14C232TM	ACTIVE	SOIC	D	16	48	TBD	CU SNPB	Level-1-235C-UNLIM	
DS14C232TM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
DS14C232TMX	ACTIVE	SOIC	D	16	2500	TBD	CU SNPB	Level-1-235C-UNLIM	
DS14C232TMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	

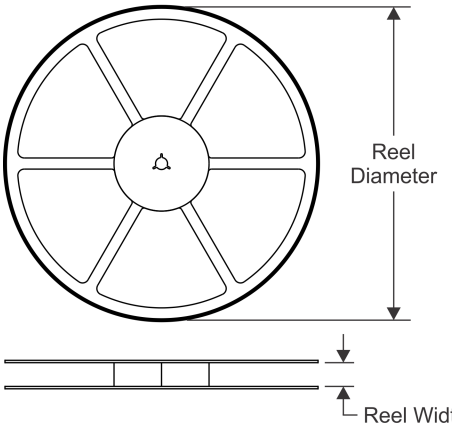
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

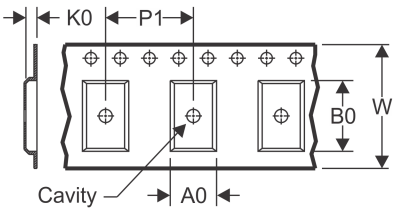
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

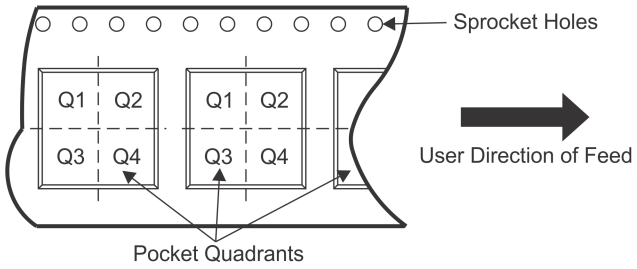


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

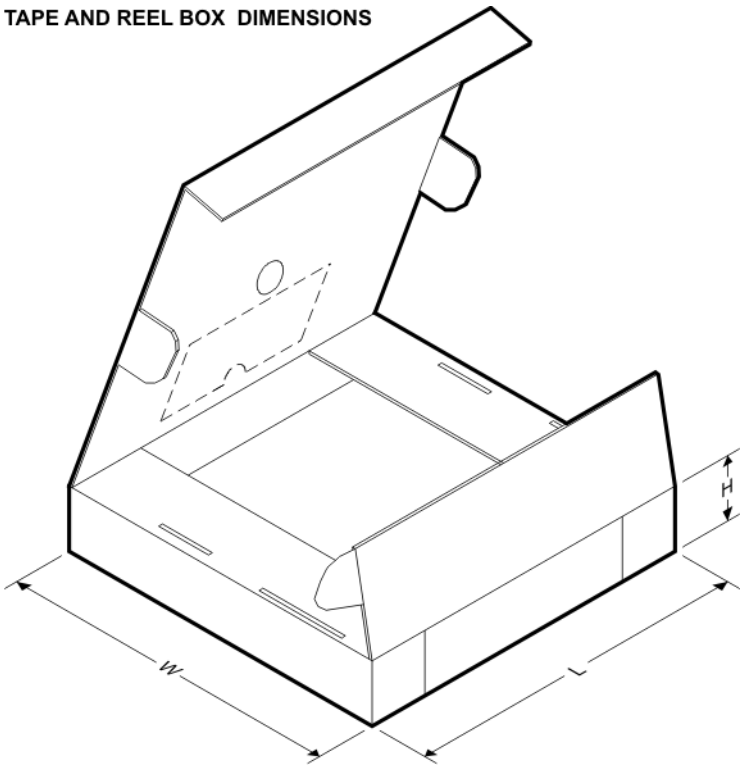
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS14C232CMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS14C232CMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS14C232TMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS14C232TMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

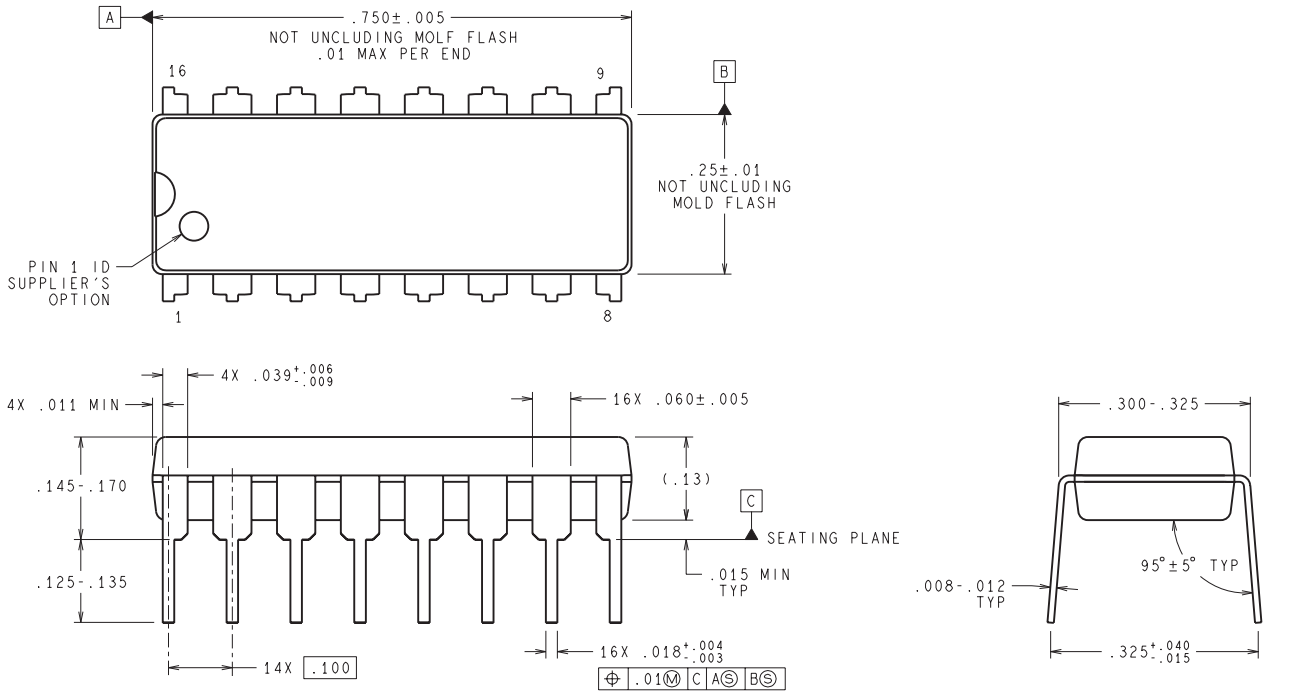
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS14C232CMX	SOIC	D	16	2500	349.0	337.0	45.0
DS14C232CMX/NOPB	SOIC	D	16	2500	349.0	337.0	45.0
DS14C232TMX	SOIC	D	16	2500	349.0	337.0	45.0
DS14C232TMX/NOPB	SOIC	D	16	2500	349.0	337.0	45.0

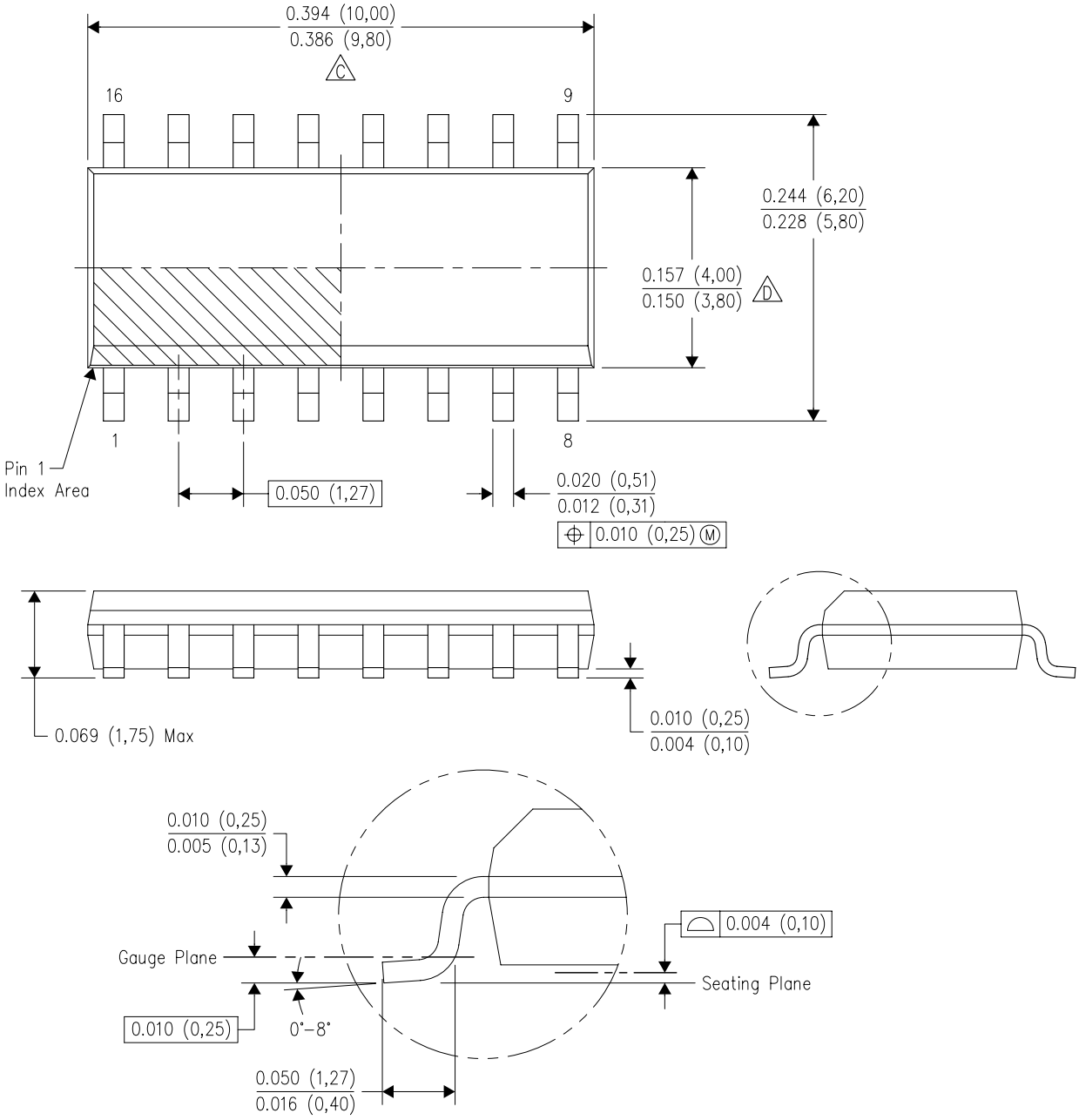
NFG0016E



DIMENSIONS ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

N16E (Rev G)

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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