ENGI21917	Lab 3	Due: End of lab session	Winter 2024

Student
(**PRINT**):_____
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Equipment: FPGA development board, laptop.

Procedures

1. Write separate VHDL codes for an inverter, a three input AND gate, and an XOR gate. Then, using **structural programming approach** instantiate them as components to build a logic gate with the given following function. (1, 1, 1, 5 marks)

$$f = \overline{(\boldsymbol{a}\ AND\ \boldsymbol{b}\ AND\ \boldsymbol{c})\ XOR\ \boldsymbol{d}}$$

2. Modify the VHDL code you developed in question 1 to implement the same logic using a NAND gate instead of the inverter. **Demonstrate your program to instructor and Describe modifications you made.** (2 Marks)