ENGI21917	Lab 2_0	Fall 2024

Student Name and ID_____

Equipment: FPGA development board, laptop.

Creating a new project in Quartus Prime Lite Edition for each of the questions in this lab

Procedures:

1- Write a VHDL code including the Entity part and architecture part to implement a gate with three inputs (a,b,c) and two outputs (f,g). Output f must be logical NOR of inputs a and c and output g must be logical XNOR of inputs b and c. (5 marks)

Load the program to your board and demonstrate it to the instructor to get full mark!

2. Write VHDL code to implement a full adder function. The truth table of the full adder is given below. You can use this truth table to obtain logical functions of sum and carry outputs. Assign a,b,c to switch 0, switch1, and switch 2 respectively. Assign LED0 to sum and LED1 to carry. **Load the program to your board and demonstrate it to the instructor to get full mark!** (5 marks)

Inputs			Outputs	
A	B	C – IN	Sum	C - Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1