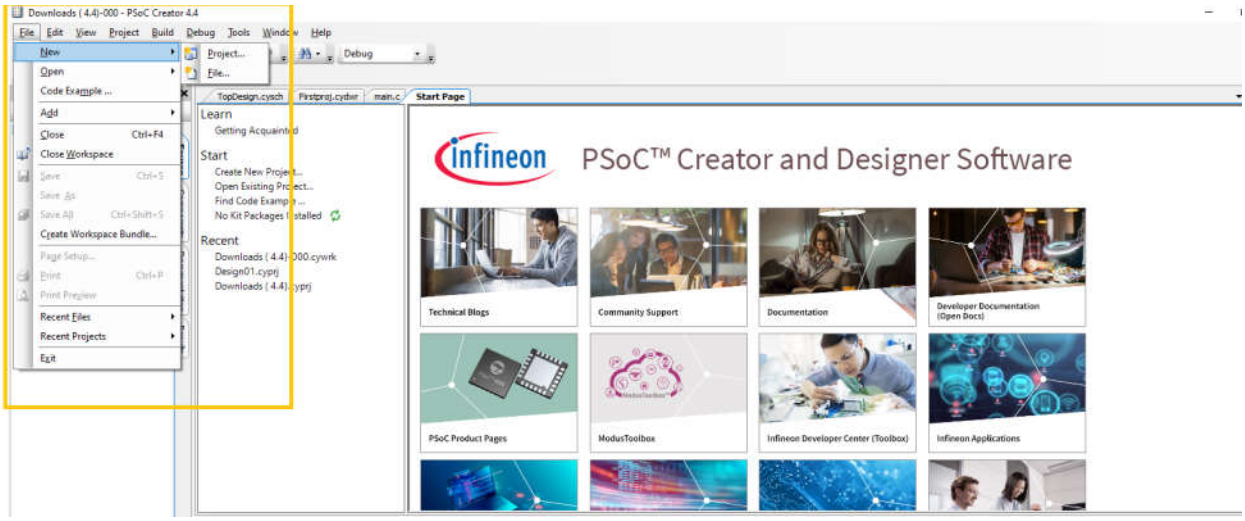
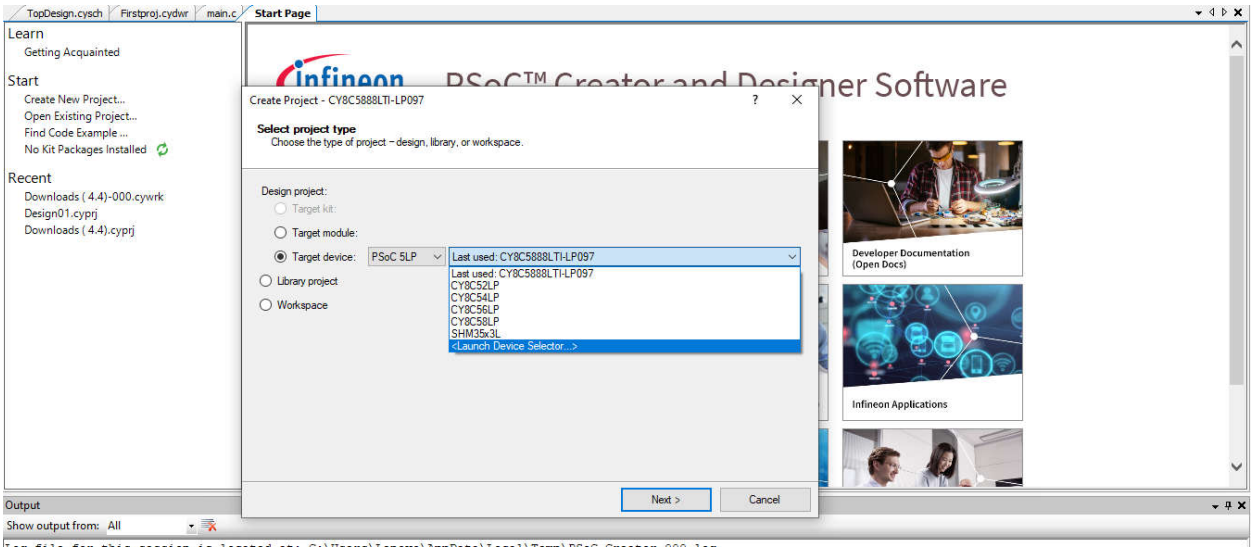
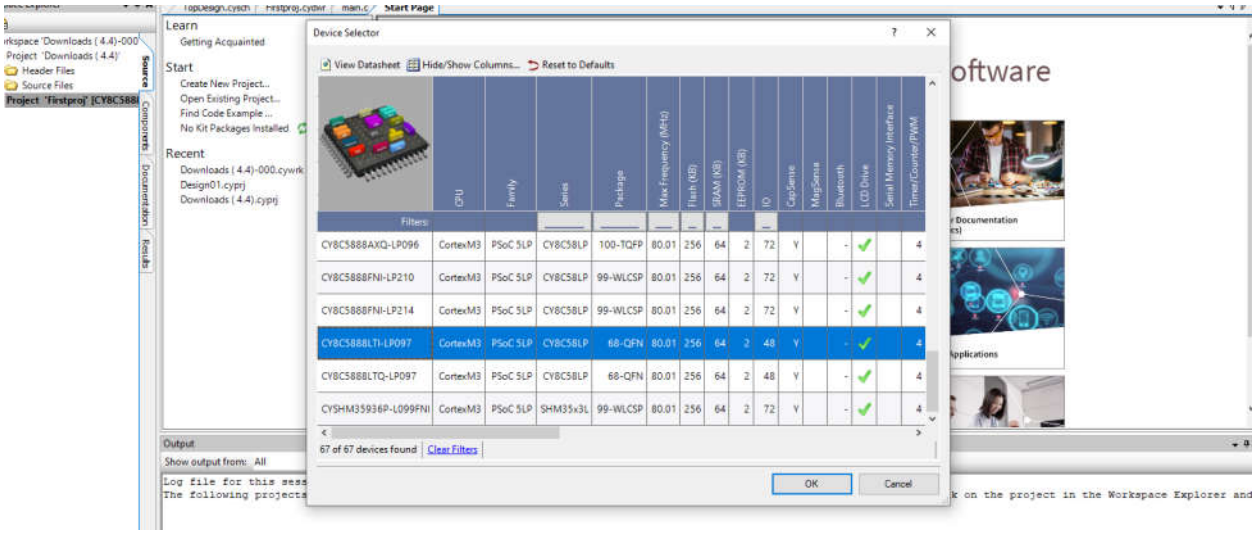
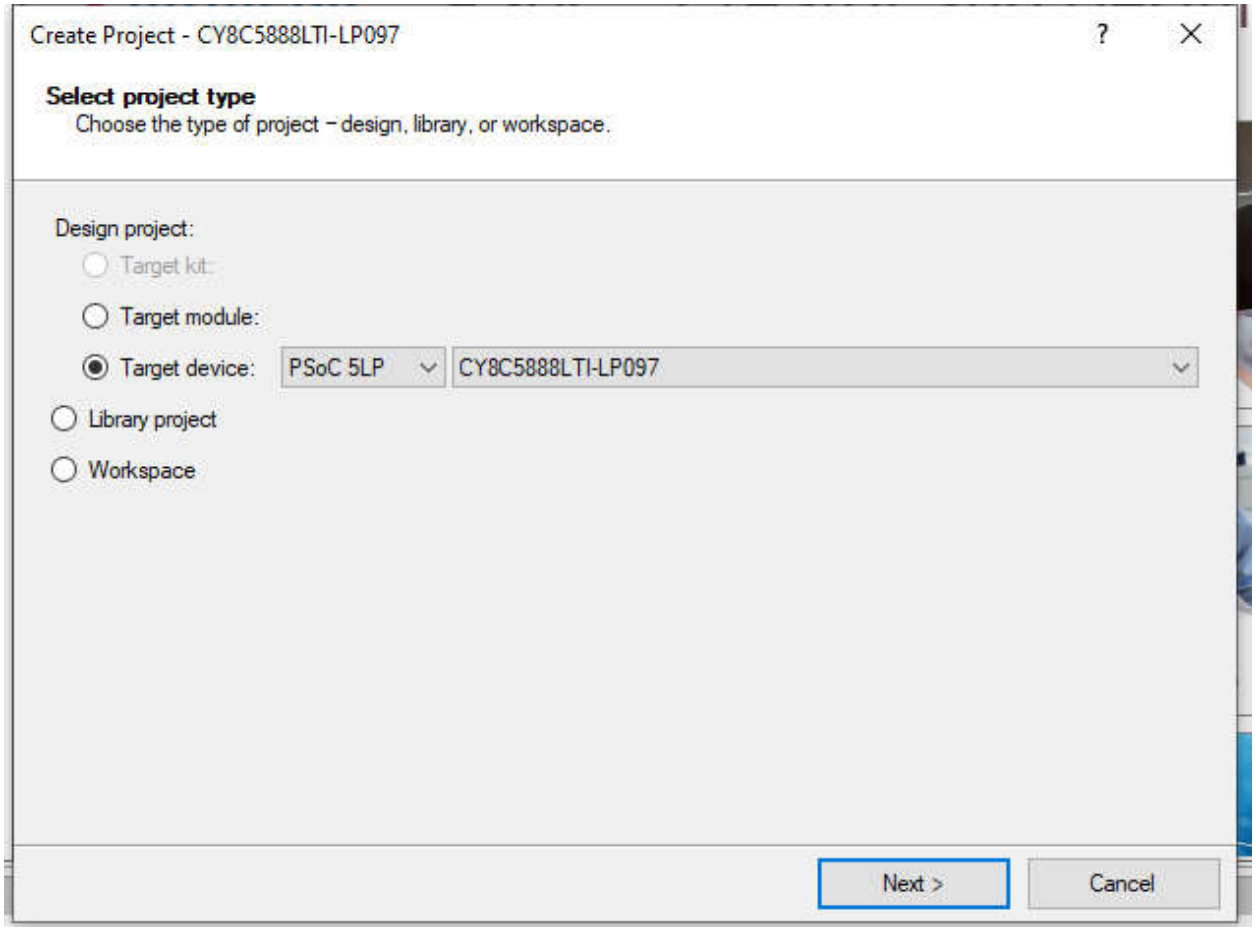
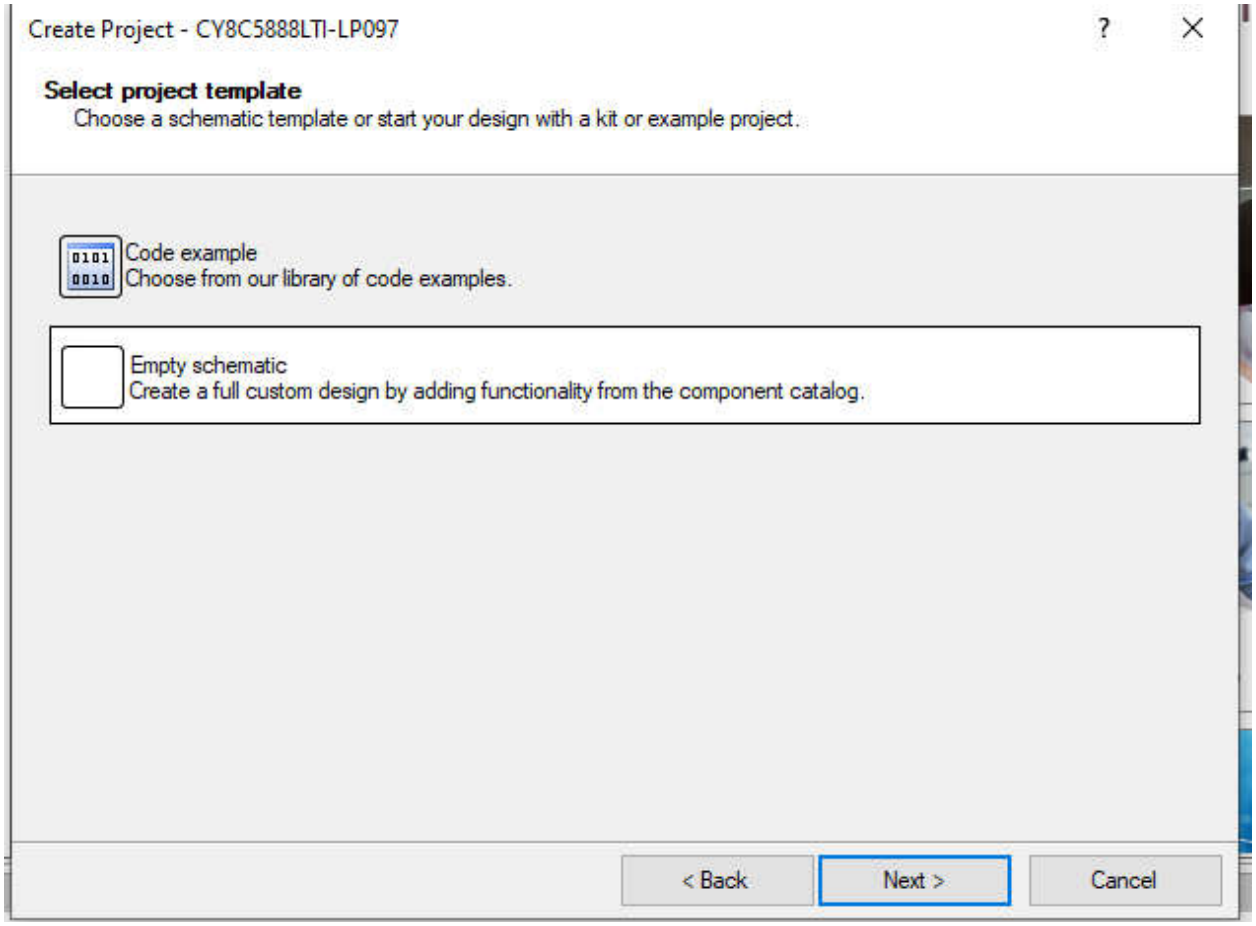
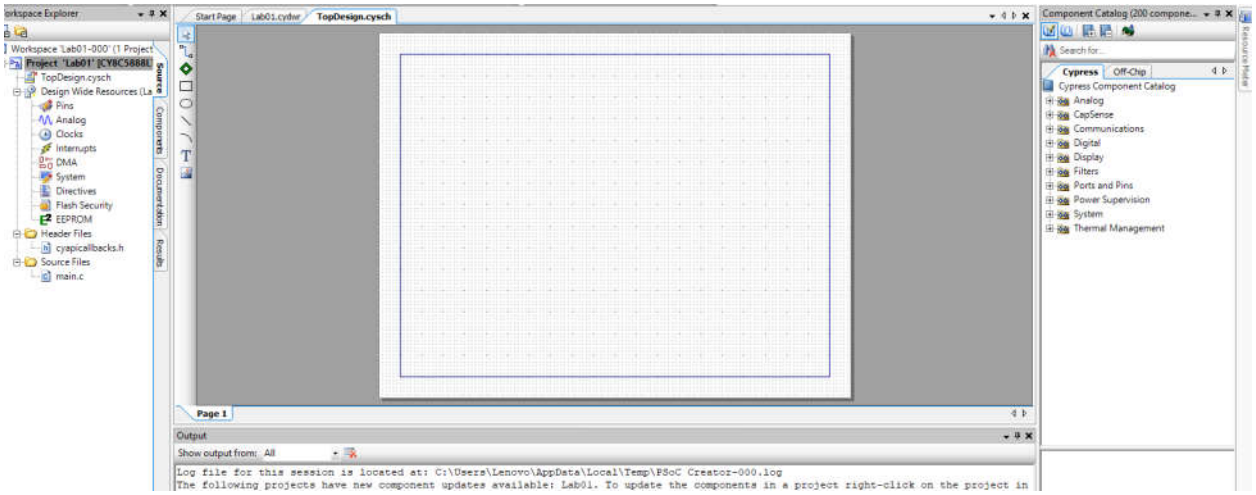

Downloads (4.4)-000 - PSoC Creator 4.4
File Edit View Project Build Debug Tools Window Help
New
Open
Code Example ...
Add
Close Ctrl+F4
Close Workspace
Create Workspace Bundle...
Recent Files
Recent Projects
Exit
Project...
File...
Debug
TopDesign.cysch
Firstproj.cydwr
main.c
Start Page
Learn
Getting Acquainted
Start
Create New Project...
Open Existing Project...
Find Code Example ...
No Kit Packages Installed
Recent
Design01.cyprj
Infineon
PSoC™ Creator and Designer Software
Technical Blogs
Community Support
Documentation
Developer Documentation (Open Docs)
PSoC Product Pages
ModusToolbox
Infineon Developer Center (Toolbox)
Infineon Applications

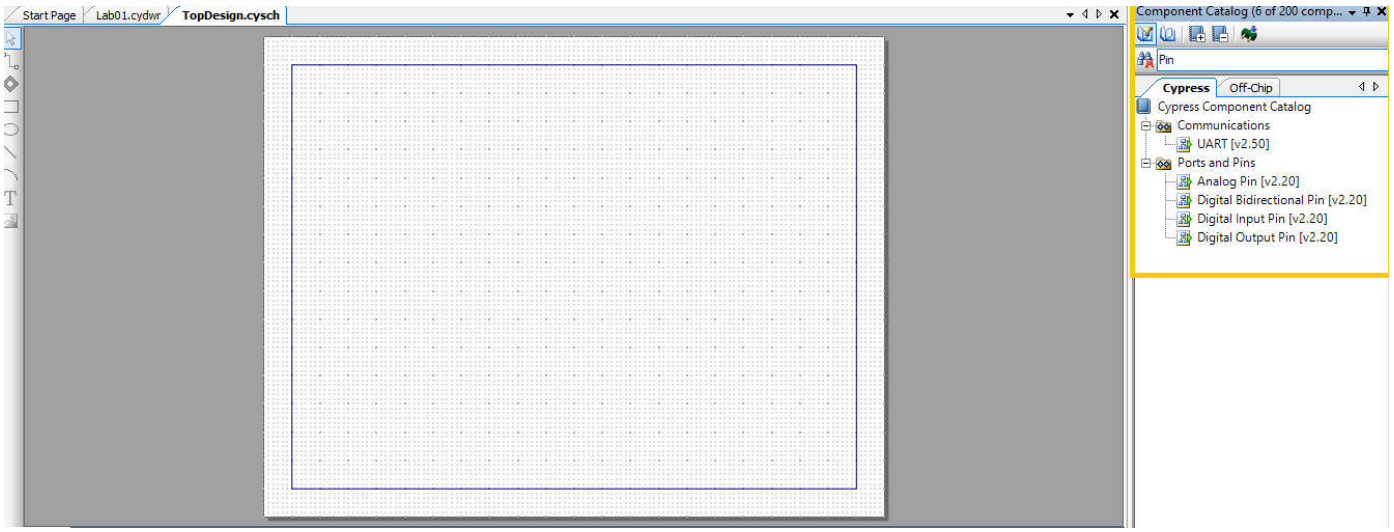

TopDesign.cysch
Firstproj.cydwr
main.c
Start Page
Learn
Getting Acquainted
Start
Create New Project...
Open Existing Project...
Find Code Example ...
No Kit Packages Installed
Recent
Downloads (4.4)-000.cywrk
Design01.cyprj
Downloads (4.4).cyprj
Create Project - CY8C5888LTI-LP097
Select project type
Choose the type of project – design, library, or workspace.
Design project:
Target kit:
Target module:
Target device:
PSoC 5LP
Last used: CY8C5888LTI-LP097
Last used: CY8C5888LTI-LP097
CY8C52LP
CY8C54LP
CY8C56LP
CY8C58LP
SHM35x3L
<Launch Device Selector...>
Library project
Workspace
Next >
Cancel
Developer Documentation (Open Docs)
Infineon Applications
Output
Show output from: All

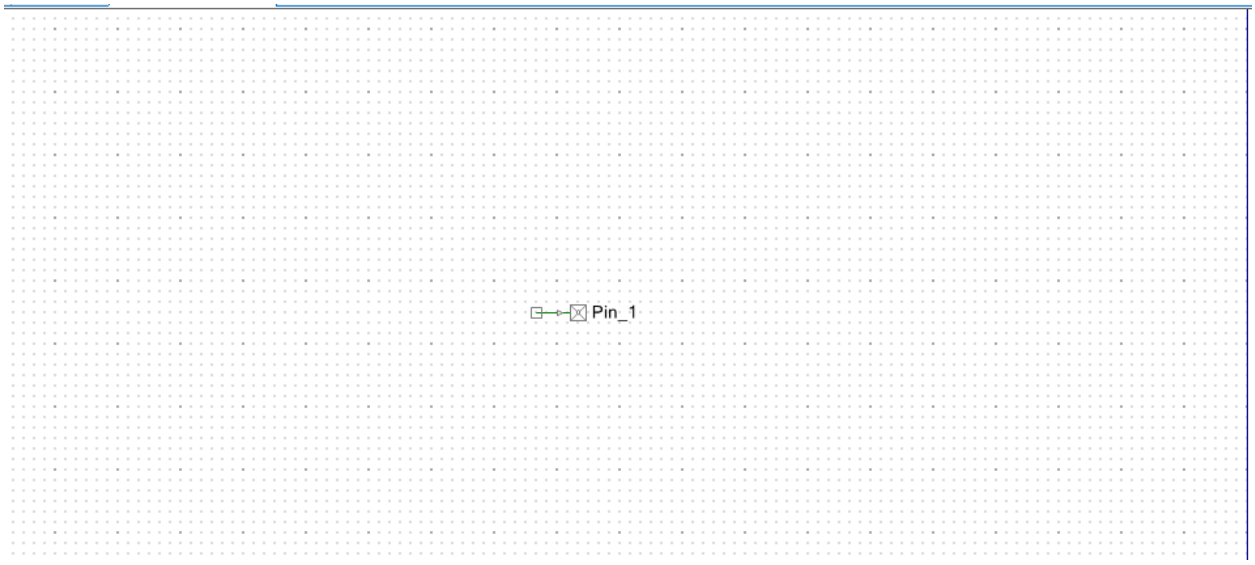

Device Selector
View Datasheet
Hide/Show Columns...
Reset to Defaults
CPU
Family
Series
Package
Max Frequency (MHz)
Flash (KB)
SRAM (KB)
EEPROM (KB)
IO
CapSense
MagSense
Bluetooth
LCD Drive
Serial Memory Interface
Timer/Counter/PWM
Filters:
CY8C5888AXQ-LP096 CortexM3 PSoC 5LP CY8C58LP 100-TQFP 80.01 256 64 2 72 Y - 4
CY8C5888FNI-LP210 CortexM3 PSoC 5LP CY8C58LP 99-WLCSP 80.01 256 64 2 72 Y - 4
CY8C5888FNI-LP214 CortexM3 PSoC 5LP CY8C58LP 99-WLCSP 80.01 256 64 2 72 Y - 4
CY8C5888LTI-LP097 CortexM3 PSoC 5LP CY8C58LP 68-QFN 80.01 256 64 2 48 Y - 4
CY8C5888LTQ-LP097 CortexM3 PSoC 5LP CY8C58LP 68-QFN 80.01 256 64 2 48 Y - 4
CYSHM35936P-L099FNI CortexM3 PSoC 5LP SHM35x3L 99-WLCSP 80.01 256 64 2 72 Y - 4
67 of 67 devices found
Clear Filters
OK
Cancel
Learn
Getting Acquainted
Start
Create New Project...
Open Existing Project...
Find Code Example ...
No Kit Packages Installed
Recent
Downloads (4.4)-000.cywrk
Design01.cyprj
Downloads (4.4).cyprj
Output
Show output from: All

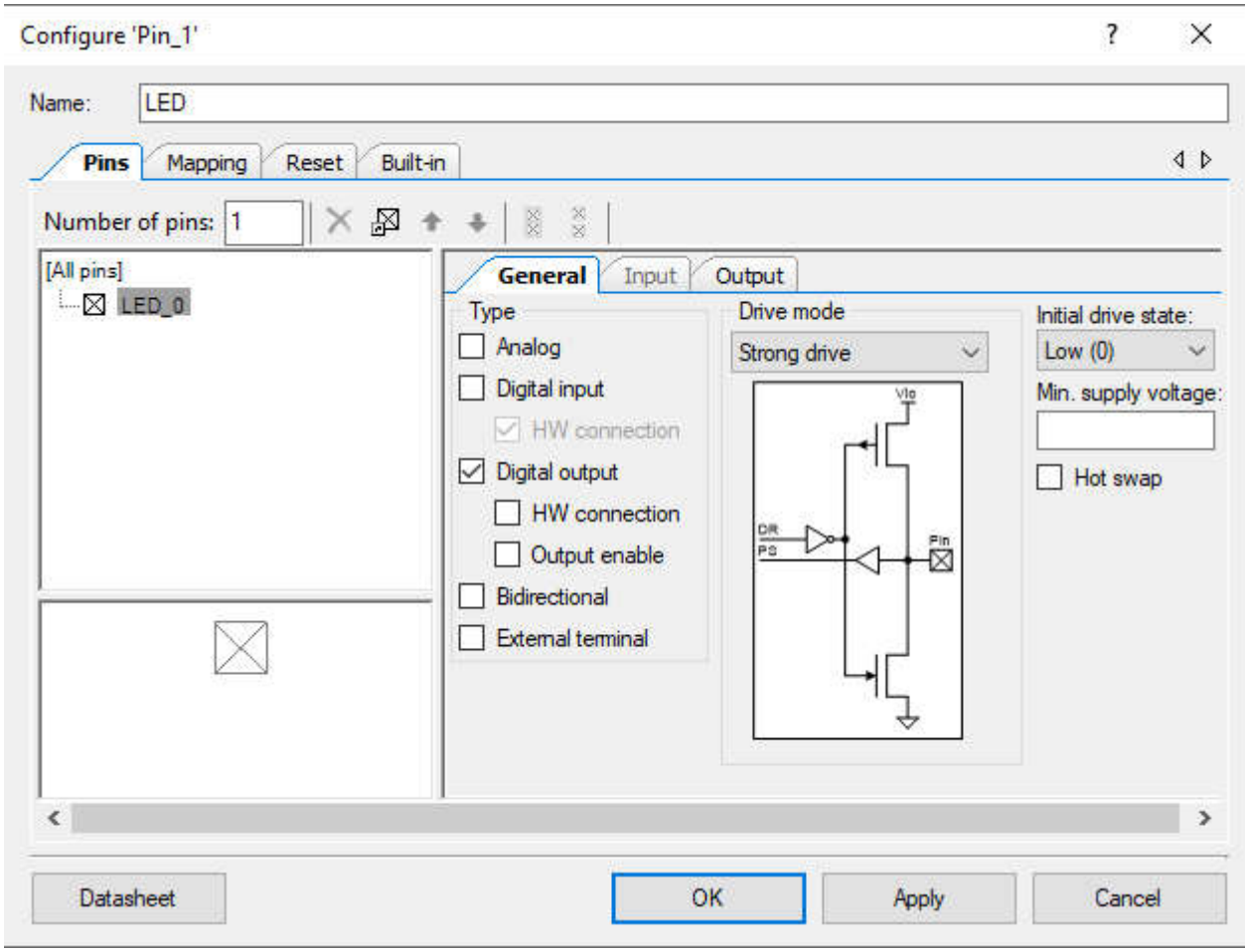

Create Project - CY8C5888LTI-LP097
Select project type
Choose the type of project – design, library, or workspace.
Design project:
Target kit:
Target module:
Target device:
PSoC 5LP
CY8C5888LTI-LP097
Library project
Workspace
Next >
Cancel

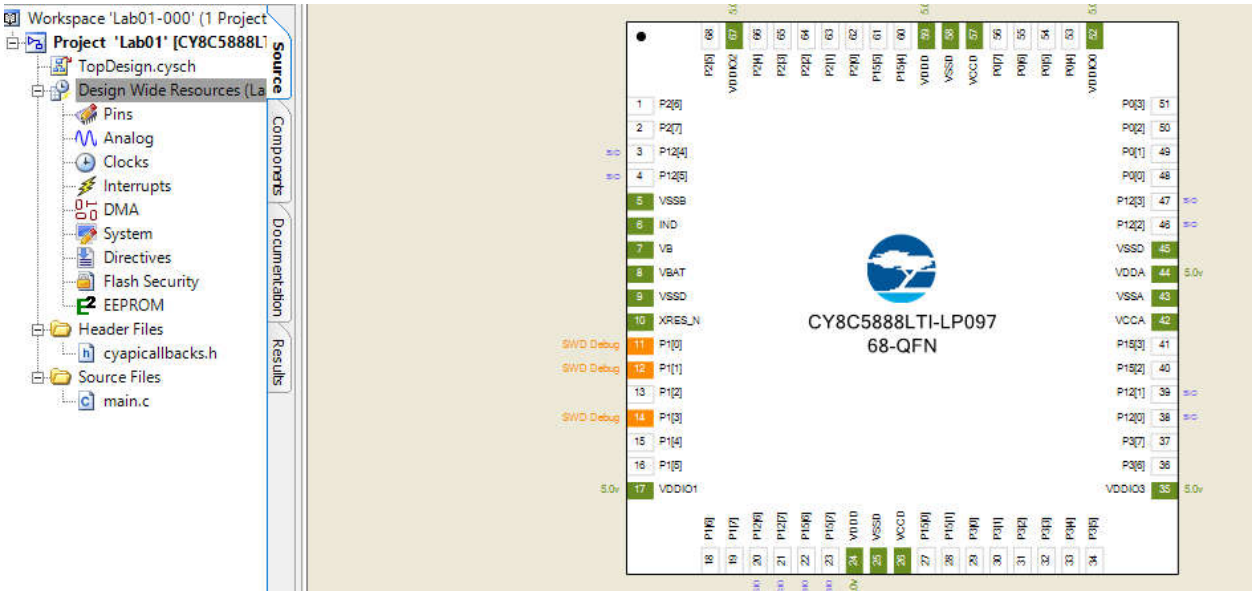

Create Project - CY8C5888LTI-LP097
Select project template
Choose a schematic template or start your design with a kit or example project.
Code example
Choose from our library of code examples.
Empty schematic
Create a full custom design by adding functionality from the component catalog.
< Back
Next >
Cancel

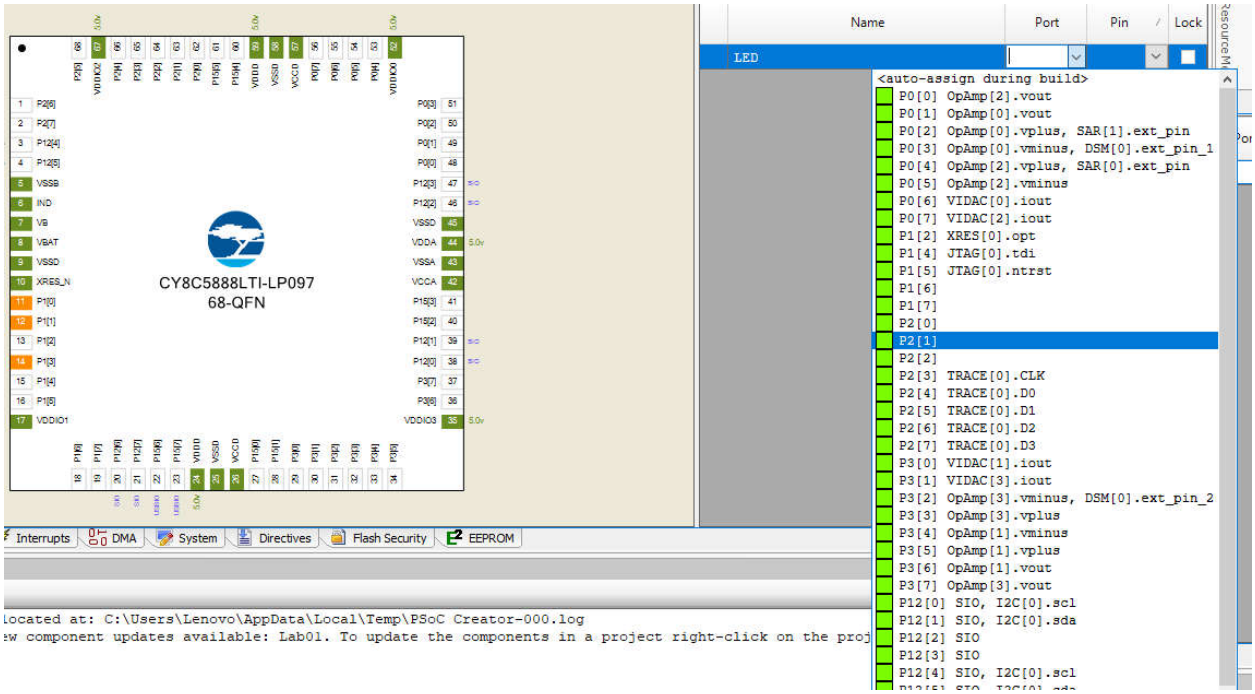

Workspace Explorer
Start Page
Lab01.cydwr
TopDesign.cysch
Component Catalog
Page 1
Output
Show output from: All

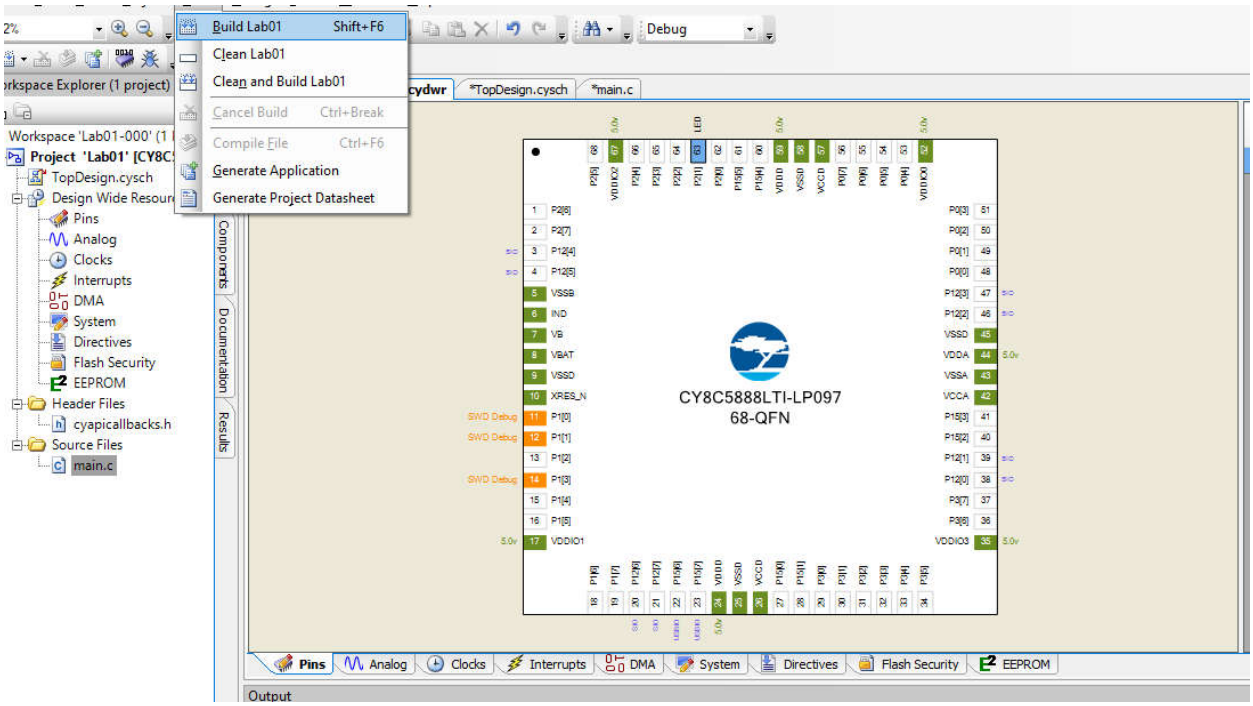

Start Page
Lab01.cydwr
TopDesign.cysch
Component Catalog (6 of 200 comp...
Pin
Cypress
Off-Chip
Cypress Component Catalog
Communications
UART [v2.50]
Ports and Pins
Analog Pin [v2.20]
Digital Bidirectional Pin [v2.20]
Digital Input Pin [v2.20]
Digital Output Pin [v2.20]


Pin_1


Configure 'Pin_1'
Name:
LED
Pins
Mapping
Reset
Built-in
Number of pins:
1
[All pins]
LED_0
General
Input
Output
Type
Analog
Digital input
HW connection
Digital output
HW connection
Output enable
Bidirectional
External terminal
Drive mode
Strong drive
Vio
DR
PS
Pin
Initial drive state:
Low (0)
Min. supply voltage:
Hot swap
Datasheet
OK
Apply
Cancel


Workspace 'Lab01-000' (1 Project
Project 'Lab01' [CY8C5888L
TopDesign.cysch
Design Wide Resources (La
Pins
Analog
Clocks
Interrupts
DMA
System
Directives
Flash Security
EEPROM
Header Files
cyapicallbacks.h
Source Files
main.c
Source
Components
Documentation
Results
CY8C5888LTI-LP097
68-QFN


Name
Port
Pin
Lock
LED
<auto-assign during build>
P0[0] OpAmp[2].vout
P0[1] OpAmp[0].vout
P0[2] OpAmp[0].vplus, SAR[1].ext_pin
P0[3] OpAmp[0].vminus, DSM[0].ext_pin_1
P0[4] OpAmp[2].vplus, SAR[0].ext_pin
P0[5] OpAmp[2].vminus
P0[6] VIDAC[0].iout
P0[7] VIDAC[2].iout
P1[2] XRES[0].opt
P1[4] JTAG[0].tdi
P1[5] JTAG[0].ntrst
P1[6]
P1[7]
P2[0]
P2[1]
P2[2]
P2[3] TRACE[0].CLK
P2[4] TRACE[0].D0
P2[5] TRACE[0].D1
P2[6] TRACE[0].D2
P2[7] TRACE[0].D3
P3[0] VIDAC[1].iout
P3[1] VIDAC[3].iout
P3[2] OpAmp[3].vminus, DSM[0].ext_pin_2
P3[3] OpAmp[3].vplus
P3[4] OpAmp[1].vminus
P3[5] OpAmp[1].vplus
P3[6] OpAmp[1].vout
P3[7] OpAmp[3].vout
P12[0] SIO, I2C[0].scl
P12[1] SIO, I2C[0].sda
P12[2] SIO
P12[3] SIO
P12[4] SIO, I2C[0].scl
CY8C5888LTI-LP097
68-QFN
Interrupts
DMA
System
Directives
Flash Security
EEPROM
located at: C:\Users\Lenovo\AppData\Local\Temp\PSoC Creator-000.log
ew component updates available: Lab01. To update the components in a project right-click on the proj


Build Lab01 Shift+F6
Clean Lab01
Clean and Build Lab01
Cancel Build Ctrl+Break
Compile File Ctrl+F6
Generate Application
Generate Project Datasheet
Debug
Workspace 'Lab01-000' (1
Project 'Lab01' [CY8C
TopDesign.cysch
Design Wide Resour
Pins
Analog
Clocks
Interrupts
DMA
System
Directives
Flash Security
EEPROM
Header Files
cyapicallbacks.h
Source Files
main.c
*TopDesign.cysch
*main.c
CY8C5888LTI-LP097
68-QFN
Components
Documentation
Results
Pins
Analog
Clocks
Interrupts
DMA
System
Directives
Flash Security
EEPROM
Output

Open main.c and type the following

```
11  */
12  #include "project.h"
13
14  int main(void)
15  {
16      CyGlobalIntEnable; /* Enable global interrupts. */
17
18      /* Place your initialization/startup code here (e.g. MyInst_Start()) */
19
20      for(;;)
21      {
22          LED_Write(1);
23          CyDelay(1000);
24          LED_Write(0);
25          CyDelay(1000);
26      }
27  }
28
29  /* [] END OF FILE */
30
```

void CyDelay(**uint32 milliseconds**)

Connect the PSoC and run the program.