Vijay Thakkar

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I Education

PhD student, Computer Science, Georgia Institute of Technology, 2021-Present.

Research area: Software-Hardware Codesign for Next Generation Linear Algebra Libraries

Advisor: Richard Vuduc

M.S., Computer Science, Georgia Institute of Technology, 2019-2021.

NOTE: Matriculated into a PhD program.

Advisor: Richard Vuduc

B.S. cum Laude, Computer Engineering, Boston University, 2019.

II Employment History

July 2022-present	NVIDIA , Compute Architect. Role: Lead designer for CUTLASS 3 and PIC for CUDA C++ Programming Model exposure of tensor cores.
Jan-July 2022	NVIDIA Research , Intern, Programming Systems and Applications group. Role: Hardware acceleration and software algorithms for spGEMM acceleration.
Jan-Aug 2021	NVIDIA , Deep Learning Compute Architecture Intern. Role: Lead designer for CUTLASS 3.0 prototype and PTX/CUDA C++ exposure of Hopper tensor core features.
Summer 2020	Cerebras Systems , Parallel and distributed algorithms intern. Role: High performance compute kernels (fast kernels) team.
2020-present	HPC Garage Lab, GTA and GRA, Georgia Institute of Technology.
Summer 2019	Arm Holdings , Software engineering Intern. Role: Cycle accurate models compiler team.
Summer 2018	Bloomberg L.P., Software Engineering Intern.

- 2016-2019 **Undergraduate Researcher** in deep learning, advisor: Brian Kulis.
- 2016-2018 **Boston University College of Engineering** Teaching Assistant for various engineering courses.

III Honors and Awards

November 2022	Gordon Bell Prize Finalist, ACM/IEEE Conf. Supercomputing 2022 (SC22).
November 2020	Gordon Bell Prize Finalist, ACM/IEEE Conf. Supercomputing 2020 (SC20).
November 2020	3rd Place, Virtual Student Cluster Competition , ACM/IEEE Conf. Supercomputing 2020 (SC20).
May 2020	Daniel V. Jackson Fellowship , College of Computational Science and Engineering, Georgia Tech.
May 2019	Undergraduate Student Service Award , Boston University College Of Engineering.
2016-2019	Dean's List , 7x awardee, Boston University College of Engineering.

IV Research

For citation counts per web-based indices, see

https://scholar.google.com/citations?user=XTVUpYcAAAAJ

IV-A Conference Presentations with Proceedings

- [P1] R. Kannan, P. Sao, H. Lu, J. Kurzak, G. Schenk, Y. Shi, S.-H. Lim, S. Israni, Vijay Thakkar, G. Cong, R. Patton, S. E. Baranzini, R. Vuduc, and T. Potok, "Exaflops biomedical knowledge graph analytics," in Proceedings of the ACM/IEEE International Conference for High-Performance Computing, Networking, Storage, and Analysis ("Supercomputing" or SC), Dallas, TX, USA, Nov. 2022. Finalist, Gordon Bell Prize
- [P2] P. Sao, H. Lu, R. Kannan, **Vijay Thakkar**, R. Vuduc, and T. Potok, "Scalable all-pairs shortest paths for huge graphs on multi-GPU clusters," in *Proceedings of the 30th International Symposium on High-Performance Parallel and Distributed Computing (HPDC)*, Stockholm, Sweden: ACM, Jun. 2021. [19%]
- [P3] R. Kannan, P. Sao, H. Lu, D. Herrmannova, **Vijay Thakkar**, R. Patton, T. E. Potok, and R. Vuduc, "Scalable knowledge-graph analytics at 136 petaflop/s," in *Proceedings of the ACM/IEEE International Conference for High-Performance Computing, Networking, Storage, and Analysis ("Supercomputing" or SC),* Atlanta, GA, USA, Nov. 2020. **Finalist, Gordon Bell Prize**
- [P4] **Vijay Thakkar**, R. Manzelli, A. Siahkamari, and B. Kulis, "Conditioning deep generative raw audio models for structured automatic music," in *Proceedings of the International Society for Music Information Retrieval (ISMIR)*, Paris, France, Sep. 2018.

IV-B Workshop Papers

[W1] R. Manzelli, **Vijay Thakkar**, A. Siahkamari, and B. Kulis, "An end to end model for automatic music generation: Combining deep raw and symbolic audio networks," in *Proceedings of the 6th International Workshop on Musical Metacreation (MUME 2018)*, Salamanca, Spain, Jun. 2018.

IV-C Posters

[Q1] R. Manzelli, **Vijay Thakkar**, and B. Kulis, "Combining deep symbolic and raw audio models for improved automatic music generation," in *Proceedings of the 12th Women in Machine Learning Workshop (WiML 2017)*, Long Beach, California, Dec. 2017.

IV-D Talks

- [T1] **Vijay Thakkar** and R. Vuduc, "Dense semiring linear algebra on modern cuda hardware," Mar. 2021. [Online]. Available: https://bit.ly/thakkar-cse-21.
- [T2] *Hpc industry roundup: 1st half 2020,* HPC & GPU Supercomputing Group of Boston, Aug. 2020. [Online]. Available: https://bit.ly/hpc1h20.
- [T3] *Hpc industry roundup: 2nd half 2019,* HPC & GPU Supercomputing Group of Boston, Aug. 2019. [Online]. Available: https://bit.ly/hpc2h19.

IV-E Submitted Papers

[S1] P. Sao, L. Hao, **Vijay Thakkar**, R. Kannan, D. Herrmannova, R. Patton, R. Vuduc, and T. Potok, Communication and memory-efficient all-pair shortest path (APSP) computation on GPU-accelerated clusters, Aug. 2020.

V Volunteering

V-A Conference Program Committee Activities

- August 2022 IEEE Hot Chips 34, Student volunteer.
- November 2021 12th IEEE International Workshop on Performance Modeling, Benchmarking and Simulation of High Performance Computer Systems, Program committee.
 - August 2021 **IEEE Hot Chips 33**, Student volunteer.
- November 2020 ACM/IEEE Conf. Supercomputing 2020 (SC20), Lead student volunteer.
 - August 2020 IEEE Hot Chips 32, Student volunteer.
- November 2019 ACM/IEEE Conf. Supercomputing 2019 (SC19), Student volunteer.

V-B Mentoring and Leadership

- 2019-2021 Graduate Mentor, Georgia Tech Student Cluster Competition Team Phoenix
- November 2019 **Peer Mentor**, ACM/IEEE Conf. Supercomputing 2020 (SC20).
 - 2017-2019 Founder and President, Boston University High Performance Computing Club.

V-C Open Source Projects

- [F1] **NVIDIA CUTLASS**.
- [F2] **Linux kernel contributions**. perf PMU counter support for AMD Zen1 and Zen2 processors.
- [F3] **RoB Size Tool** by Travis Downs A microbenchmark reverse engineering tool for out of order CPUs.
- [F4] **MemeOS** 32bit x86 operating system built from the bootloader up with thread creation and management, curses like 4bit VGA color terminal, and UFS file system.