Tamanna Thakral

Entry Number: 2023EE10747
B.Tech.(Electrical Engineering)
IIT-Delhi

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Education

Degree/Certificate	Institute/Board	CGPA/Percentage	Year
B.Tech	Indian Institute of Technology, Delhi	7.38	2023 - Present
CBSE	Tiny Tots School, Rajasthan	93.8%	2023
CBSE	Tiny Tots School, Rajasthan	94.2%	2021

Academic Achievements

- **All India Rank (GE) 1538**,in Joint Entrance Examination (JEE) Advanced, out of around 180,000 candidates. *2023*
- **All India Rank (GE) 1722**, Joint Entrance Examination (JEE) Main, out of around 930,000 candidates. *2023*
- **Completed Coding Ninjas' 60+ hour course on DSA** ,mastering key concepts and problem-solving techniques. *2024*
- **Ranked 144 in the National Science Olympiad** ,out of 50,000 students, showcasing strong scientific aptitude. *2022*

Projects

- **Flight Planner** *Feb, 2025*
  Prof. Parag Singla (CSE Dept. IIT-D)
  – Designed a flight planner using graph-based algorithms (Dijkstra, BFS) to find **cheapest**, **fewest flights**, and **earliest arrival** routes between cities.
  – Optimized for large inputs using adjacency lists and priority queues, with clean modular code for different query types.
  – Built a Python GUI using Tkinter for intuitive user interaction, allowing dynamic input and visual route outputs.

- **Digital Library System** *October, 2024*
  Prof. Parag Singla (CSE Dept. IIT-D)
  – Developed a system for efficient digitization and keyword search using custom hash tables with **O(1)** complexity.
  – Applied O(n log n) merge sort with **collision handling** (chaining, linear probing, double hashing) for efficiency
  – Utilized dynamic resizing to maintain **O(1)** amortized insertion, ensuring efficient space-time tradeoff.

- **Autonomous Robot Pathfinding** *August, 2024*
  Prof. Parag Singla (CSE Dept. IIT-D)
  – Developed a stack-based navigation system for robots in a grid environment with obstacles.
  – Implemented pathfinding algorithms to find efficient routes with time complexity of **O(n * m)**.
  – Applied recursive backtracking and stack data structures to prevent revisiting nodes.

- **Synchronous 4-bit Gray-Code Counter Design** *November, 2024*
  Prof. Manan Suri (Electrical Dept. IIT-D)
  – Designed and implemented the counter logic using **Verilog/VHDL** for cyclic 16-state Gray-Code counting.
  – Verified functionality through simulation and debugging in a hardware description language environment.
  – Applied **Karnaugh map** optimization to derive minimized input expressions for **SR flip-flops** in HDL.

Relevant courses undertaken

- **Computer Science**: Introduction to Computer Science, Data Structures and Algorithms
- **Maths**: Linear Algebra and Differential equation, Calculus
- **Electrical engineering**: Signal and Systems, Digital Electronics, Circuit Theory
- **Others**: EM Waves and Quantum Mechanics, Engineering Mechanics

Technical Skills

- **Programming Languages**: C/C++, Python, Matlab, SQL
- **Tools**: Verilog, LT-Spice, Autodesk Inventor, GDB Debugger, Git
- **Others**: Linux, MS office

Extra Curricular Activities

- **Activity Head, Rendezvous'24**,Handled coordination a cultural event at the institute's annual fest *Aug'24-Present*
- **Executive, eDC IIT Delhi**,Organized entrepreneurial events, fostered startup initiatives *Apr'24-Present*
- **Activity Head, BECon'25**,Managed event operations at India's largest student-run E-Summit. *Nov'24-Present*