```
TITLE "PROGRAPE-1 CONTROL CPLD";
            용
                    Controllers for PROGRAPE-1 Board
                  Copyright(c) 1997 by Tsuyoshi Hamada
                      July. 97 First Version
         FUNCTION dropdiff (clk ,in)
                              -- differential circuit (react to dropping edge)
RETURNS (out);
                              -- asynchronous delay generator (about 20.7ns)
FUNCTION delay (in)
RETURNS (out);
CONSTANT
               DWIDTH = 32;
               AWIDTH = 19;
CONSTANT
SUBDESIGN ctrl
       clk, rst
                                      : INPUT;
                                      : INPUT;
       /io_req
       hdata[DWIDTH-1..0]
                                      : BIDIR;
       /dma_ack
                                      : INPUT;
       /d read
                                      : OUTPUT:
       data[DWIDTH-1..0]
                                      : BIDIR;
       /dma_r
                                      : OUTPUT;
        /dma w
                                      : OUTPUT;
       index[AWIDTH-6..0]
                                      : OUTPUT;
       adrs[7..0]
                                      : OUTPUT;
       mwe[3..0]
                                      : OUTPUT;
                                                     -- Memory Write Enable
                                      : OUTPUT;
                                                     -- Pipeline Write Enable
       /pwe
        /pcs[15..0]
                                      : OUTPUT;
                                                     -- Pipeline Chip Select
       prun
                                      : OUTPUT:
        /d write
                                      : OUTPUT;
VARIABLE
       gclk,grst
                                      : NODE;
                                                     -- GLOBAL
       pdata[DWIDTH-1..0]
                                      : DFF;
       pdatad[DWIDTH-1..0]
                                      : DFF;
       result[DWIDTH-1..0]
                                      : DFF;
       phase: MACHINE WITH STATES (crt, dmar, dmaw, run);
       p_y[1..0]
                                      : DFF:
                                      : NODE;
       p z[1..0]
                                      : DFF;
        /pipcs[15..0]
        /pcs[15..0]
                                      : DFF;
       hibtri[DWIDTH-1..0]
                                      : TRI;
       piptri[DWIDTH-1..0] : TRI;
                                      : DFF; -- GND:HIB => PRO, VCC:PRO =>HIB
       tri_oe
       index[AWIDTH-6..0]
                                      : DFF:
                                      : DFF;
       adrs[7..0]
-- COMMAND READ TIMING
        /d read
                              : DFF;
       drop_req
                              : dropdiff;
       get
                              : dropdiff;
       getd
                              : DFF;
       getdd
                              : DFF;
                              : dropdiff;
       end_crt
                              : DFF:
       drop_reqd
       comnd[DWIDTH-1..0]
                              : DFF;
-- DMA_READ
       /dma r
                              : DFF;
        /dma_ackd
                              : DFF;
       hwords[11..0]
                              : DFF;
```

```
nset[15..0]
                                : DFF:
        /pipwe
                                : DFF;
                                : DFF;
        /pwe
        mwe[3..0]
                                : DFF;
        dclk
                                : delay;
-- DMA WRITE
        drop_ack
                                : dropdiff;
        /dma w
                                : DFF;
        start_w
                                : DFF;
                                : DFF;
        pwords[7..0]
        end dmaw
                                : DFF;
        /pd_write[5..0]
                                : DFF;
-- RUN
                                : DFF;
        rn_count[15..0]
                                : DFF;
        end run
        rn_cd[15..0]
                                : DFF;
                                : DFF;
        prun
        pprun
                                : DFF;
                                : DFF;
        ppprun
        BEGIN
        DEFAULTS
                /pd_write[] = VCC;
        END DEFAULTS;
        gclk = GLOBAL(clk);
        grst = GLOBAL(rst);
        phase.clk
                        = gclk;
        phase.reset
                        = !grst;
        p_y[].clk
                        = gclk;
                        = grst;
        p_y[].clrn
        index[].clk = gclk;
        index[].clrn = grst;
        adrs[].clk = gclk;
        adrs[].clrn = grst;
                       = gclk;
        pdata[].clk
        pdata[].clrn = grst;
        pdatad[].clk = gclk;
        pdatad[].clrn = grst;
        result[].clk = gclk;
        result[].clrn = grst;
        -- only used in DMA READ and DMA WRITE
                                    % _ | in common between DMA_READ and DMA_WEITE. _
% _ | in common between DMA_READ and DMA_WEITE. _
        /dma_ackd.clk = gclk;
        /dma_ackd.prn = grst;
                                    % _|_| in common between DMA_READ and DMA_WEITE. _|_|%
        /dma ackd.d = /dma ack;
        /pipcs[].clk = gclk;
        IF !((p_z[] == 1) # (p_z[] == 2)) THEN
                /pipcs[].prn
                /pipcs[].d = VCC;
        END IF:
        -- Tri State Buffer control --
        tri oe.clk
                        = gclk;
        tri oe.clrn
                        = grst;
        IF !/dma_w.q THEN
                tri oe.d = VCC;
        ELSE
                tri oe.d = GND;
        END IF;
        -- Tri State Buffer connection --
        hibtri[].oe = tri_oe.q;
        piptri[].oe = !tri_oe.q;
        pdata[].d = hdata[];
```

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ctrl.tdf
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                                                                                                                                                      Page 3
       pdatad[].d = pdata[].q;
      piptri[].in = pdatad[].q;
      data[] = piptri[].out;
      result[].d = data[];
      hibtri[].in = result[].q;
      hdata[] = hibtri[].out;
TABLE
             phase, p_y[].q
                                 => p_z[],
                                                      phase;
             crt,
                                                                   crt;
             crt,
                                        =>
                                                                   dmar;
                           1
                                                      1,
             crt,
                                                                   dmaw;
                                                      2,
             dmar,
                                        =>
                                                      1,
                                                                   dmar;
             dmar,
                                                                   crt;
             dmar,
                                        =>
                                                                   run;
                                        =>
                                                                   run;
             run,
                                        =>
             run,
                                                                   crt;
                                        =>
             dmaw,
                           0
                                                      2,
                                                                   dmaw;
             dmaw,
                                                                   crt;
      END TABLE;
/d_read.prn
                   = grst;
       drop req.clk = gclk;
      drop_req.in = /io_req;
      get.clk
                    = gclk;
       get.in
                    = !/d_read;
      getd.clk
                    = gclk;
                    = get.out;
      getd.d
                    = gclk;
      getdd.clk
      getdd.d
                     = getd.q;
      end crt.in
                    = getd.q;
      end crt.clk
                    = gclk;
      drop_reqd.clk
                    = gclk;
      drop reqd.d
                           = drop req.out;
      comnd[].clk
                           = gclk;
      comnd[].clrn
                    = grst;
IF p_z[] == 0 THEN
       /d_read.d = !(drop_req.out # drop_reqd.q);
       IF getdd.q THEN
             comnd[].d = pdata[].q;
      ELSE
             comnd[].d = comnd[].q;
      END IF:
      TABLE
             end_crt.out,
                          comnd[DWIDTH-1].q
                                                      p_y[].d;
                    0,
                    1,
                                                                          =>
                                                                                       1;
                    1,
                                                                                       2;
      END TABLE;
ELSE
      comnd[].d = comnd[].q;
      /d read.d = /d read.q;
END IF;
% _/_/_/_/_/_/_/
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/dma_r.clk
       /dma r.prn
                     = grst;
       hwords[].clk
                    = gclk;
       end dmar.clk
                    = gclk;
       end dmar.clrn = grst;
       nset[].clk
                           = gclk;
       nset[].clrn
                            = grst;
       /pipwe.clk
                            = gclk;
       /pipwe.prn
                            = grst;
       dclk.in
                            = gclk;
                            = gclk;
       mwe[].clk
       mwe[].prn
       /pwe.clk
                            = gclk;
                            = grst;
       /pwe.prn
       /pcs[].clk
                            = gclk;
                            = grst;
       /pcs[].prn
       /pwe.d = /pipwe.q;
       /pcs[].d = /pipcs[].q;
IF p z[] == 1 THEN
       hwords[].clrn = VCC; -- counter is available
       /dma r.d = GND;
       -----| XXXXXXXX C A U T I O N ! XXXXXXXX
       % requirement of transition to phase 'crt'.% -- X If HIB send a extra low signal X
                                                     -- | X of /dma_ack to PROGRAPE-1, X
       end_dmar.d = (hwords[].q == comnd[11..0]+1);
       IF end dmar.q THEN
                                                         -- | X PROGRAPE-1 writes a wrong data X
              p_y[].d = 1;
                                                             X into own Memory.
       ELSE
                                                             XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
              IF !/dma_ackd.q THEN
                     \overline{h}words[].d = hwords[].q + 1;
              ELSE
                     hwords[].d = hwords[].q;
              END IF;
              IF comnd[DWIDTH-2..DWIDTH-6] == B"01110" THEN
                                                              --> RUN
                     p y[].d = 2;
              ELSE
                     p_y[].d = 0;
              END IF;
       END IF;
       %=*=*=*=*=*=*=*=*= command decode =*=*=*=*=*=*=*=*=*=*
              comnd[DWIDTH-2..DWIDTH-6] == B"00000" THEN -- 0000..03FFF --
              mwe0.d = /dma ackd.q;
       ELSE
              mwe0.d = VCC;
       END IF:
       IF comnd[DWIDTH-2..DWIDTH-6] == B"00001" THEN -- 04000..07FFF
              mwe1.d = /dma_ackd.q;
       ELSE
              mwe1.d = VCC;
       IF comnd[DWIDTH-2..DWIDTH-6] == B"00010" THEN -- 08000..0BFFF
              mwe2.d = /dma_ackd.q;
       ELSE
              mwe2.d = VCC;
       IF comnd[DWIDTH-2..DWIDTH-6] == B"00011" THEN -- 0C000..0FFFF
              mwe3.d = /dma ackd.q;
                                                                      --
       ELSE
              mwe3.d = VCC;
       END IF;
       IF (comnd[DWIDTH-2] == B"1") THEN
              /pipwe.d = /dma ack; -- Write Enable of ALL Pipelines
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/pipcs12.d = VCC;
       END IF:
                                                                    --
       IF comnd[DWIDTH-2..DWIDTH-6] == B"11101" THEN -- pipline13 CS
              /pipcs13.d = /dma_ack;
       ELSE
              /pipcs13.d = VCC;
       END IF;
       IF comnd[DWIDTH-2..DWIDTH-6] == B"11110" THEN -- pipline14 CS
              /pipcs14.d = /dma ack;
       ELSE
                                                                     --
              /pipcs14.d = VCC;
                                                                    --
       END IF;
       IF comnd[DWIDTH-2..DWIDTH-6] == B"11111" THEN -- pipline15 CS
              /pipcs15.d = /dma ack;
       ELSE
              /pipcs15.d = VCC;
       END IF;
       IF
              comnd[DWIDTH-2..DWIDTH-6] == B"01100" THEN -- set N
              IF !/dma ackd.q THEN
                     nset[].d = pdata[15..0].q;
              ELSE
                     nset[].d = nset[].q;
              END IF;
       ELSE
                                                                    __
              nset[].d = nset[].q;
       END IF;
       index[] = (comnd[25..24], hwords[].q);
       adrs[] = hwords[7..0].q;
ELSE
       /dma r.d = VCC;
       mwe[] = grst;
       hwords[].clrn = GND; -- counter is disabailable
       nset[].d = nset[].q; -- This N is constant during other state.
       /pipwe.d = VCC;
END IF:
drop_ack.clk = gclk;
       /dma w.clk
                    = qclk;
       /dma w.prn
                     = grst;
       start w.clk
                           = gclk;
       start w.clrn = grst;
       pwords[].clk = gclk;
       end dmaw.clk = gclk;
       end_dmaw.clrn = grst;
       /pd write[].clk = gclk;
       /pd_write1.d = /pd_write0.q;
       /pd write2.d = /pd write1.q;
       /pd_write3.d = /pd_write2.q;
       /pd write4.d = /pd write3.q;
       /pd write5.d = /pd write4.q;
       /d write = /pd write5.q;
IF p_z[] == 2 THEN
  /dma \ w.d = GND;
  drop ack.in = /dma ack;
  IF drop_ack.out THEN
              start_w.d = VCC;
  ELSE
              start_w.d = start_w.q;
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pwords[].clrn = VCC; -- counter is available
      end_dmaw.d = (pwords[].q == comnd[7..0] + 1);
     IF end dmaw.q THEN
             p_y[].d = 1;
      ELSE
             pwords[].d = pwords[].q + 1;
      END IF;
     adrs[].d = pwords[].q - 1;
IF !end_dmaw.q THEN
      /pipcs[].prn = VCC;
      /pd write0.prn = VCC;
      %=*=*=*=*=*=*=*=
                            IF comnd[DWIDTH-2] == B"1" THEN -- /d write pulse
             /pd write0.d = GND;
     ELSE
             /pd write0.d = VCC;
     END IF;
     IF comnd[DWIDTH-2..DWIDTH-6] == B"10000" THEN -- pipline0 CS
                                                                         --
             /pipcs0.d = GND;
     ELSE
             /pipcs0.d = VCC;
     END IF;
     IF comnd[DWIDTH-2..DWIDTH-6] == B"10001" THEN -- pipline1 CS
             /pipcsl.d = GND;
     ELSE
             /pipcs1.d = VCC;
     END IF:
                                                                         --
     IF comnd[DWIDTH-2..DWIDTH-6] == B"10010" THEN -- pipline2 CS
             /pipcs2.d = GND;
      ELSE
             /pipcs2.d = VCC;
     END IF;
     IF comnd[DWIDTH-2..DWIDTH-6] == B"10011" THEN -- pipline3 CS
             /pipcs3.d = GND;
     ELSE
             /pipcs3.d = VCC;
      END IF;
     IF comnd[DWIDTH-2..DWIDTH-6] == B"10100" THEN -- pipline4 CS
             /pipcs4.d = GND;
     ELSE
                                                                         __
             /pipcs4.d = VCC;
     END IF;
     IF comnd[DWIDTH-2..DWIDTH-6] == B"10101" THEN -- pipline5 CS
             /pipcs5.d = GND;
     ELSE
             /pipcs5.d = VCC;
     END IF;
     IF comnd[DWIDTH-2..DWIDTH-6] == B"10110" THEN -- pipline6 CS
             /pipcs6.d = GND;
                                                                         --
     ELSE
                                                                         --
             /pipcs6.d = VCC;
     END IF:
      IF comnd[DWIDTH-2..DWIDTH-6] == B"10111" THEN -- pipline7 CS
             /pipcs7.d = GND;
      ELSE
             /pipcs7.d = VCC;
     END IF;
     IF comnd[DWIDTH-2..DWIDTH-6] == B"11000" THEN -- pipline8 CS
             /pipcs8.d = GND;
                                                                         --
     ELSE
             /pipcs8.d = VCC;
      END IF;
     IF comnd[DWIDTH-2..DWIDTH-6] == B"11001" THEN -- pipline9 CS
             /pipcs9.d = GND;
```