ISA MCU ST10 FAMILY

Quantidade de formatos para operações

Immediate	Cópia entre Regs	ADD*	SUB*	Inconditional Jump	FLAG
4 MOV	4 MOV	28 ADD(B) e ADDC(B)	28 SUB(B) e SUBC(B)	JMPS	N, C, V, Z e E
8 ADD					"S", "-", "0"
					"NOR"
					"AND"
					"OR"
					"XOR"
					"B", "B'"

*ADD e SUB com extensão word ou byte (B)

Data addressing modes

Abbreviation	Meaning
Rw	Word GPR (R0, R1, ... , R15)
Rb	Byte GPR (RL0, RH0, ..., RL7, RH7)
reg	SFR or GPR (in case of a byte operation on an SFR, only the low byte can be accessed via 'reg')
mem	Direct word or byte memory location
#datax	Immediate constant (the number of significant bits that can be user-specified is given by the appendix "x")
caddr	Direct 8-bit segment address (Updates the Code Segment Pointer)
seg	Direct 8-bit segment address (Updates the Code Segment Pointer)

**Immediate

Instruction set ordered by Hex code (without operand)

Mnemonic	Hex code
ADD	00-08
ADDC	10-19
JMPS	FA
MOV	(C0, D0, F0-F1), (E0-E1, E6-E7)
SUB	20-29
SUBC	30-39

Instruction set ordered by Hex code ADD

Hex code	Mnemonic	Operand
0 0	ADD	Rwn, Rwm
0 1	ADDB	Rbn, Rbm
0 2	ADD	reg, mem
0 3	ADDB	reg, mem
0 4	ADD	mem, reg
0 5	ADDB	mem, reg
0 6**	ADD	reg, #data16
0 7**	ADDB	reg, #data16
0 8	ADD	Rwn, [Rwi +] or Rwn, [Rwi] or Rwn, #data3
0 9	ADDB	Rwn, [Rwi +] or Rwn, [Rwi] or Rwn, #data3

Instruction set ordered by Hex code ADDC

Hex code	Mnemonic	Operand
1 0	ADDC	Rwn, Rwm
1 1	ADDCB	Rbn, Rbm
1 2	ADDC	reg, mem
1 3	ADDCB	reg, mem
1 4	ADDC	mem, reg
1 5	ADDCB	mem, reg
1 6**	ADDC	reg, #data16
1 7**	ADDCB	reg, #data16
1 8	ADDC	Rwn, [Rwi +] or Rwn, [Rwi] or Rwn, #data3
1 9	ADDCB	Rwn, [Rwi +] or Rwn, [Rwi] or Rwn, #data3

Instruction set ordered by Hex code SUB

Hex code	Mnemonic	Operand
C 0	MOVBZ	Rbn, Rbm
D 0	MOVBS	Rbn, Rbm
E 0**	MOV	Rwn, #data4
E 1**	MOVB	Rwn, #data4
E 6**	MOV	reg, #data16
E 7**	MOVB	reg, #data16
F0	MOV	Rwn, Rwm
F1	MOVB	Rbn, Rbm

Instruction set ordered by Hex code JMPS

Hex code	Mnemonic	Operand
F A	JMPS	seg, caddr

Instruction set ordered by Hex code SUB

Hex code	Mnemonic	Operand
2 0	SUB	Rwn, Rwm
2 1	SUBB	Rbn, Rbm
2 2	SUB	reg, mem
2 3	SUBB	reg, mem
2 4	SUB	mem, reg
2 5	SUBB	mem, reg
2 6	SUB	reg, #data16
2 7	SUBB	reg, #data16
2 8	SUB	Rwn, [Rwi +] or Rwn, [Rwi] or Rwn, #data3
2 9	SUBB	Rwn, [Rwi +] or Rwn, [Rwi] or Rwn, #data3

Instruction set ordered by Hex code SUBC

Hex code	Mnemonic	Operand
3 0	SUBC	Rwn, Rwm
3 1	SUBBC	Rbn, Rbm
3 2	SUBC	reg, mem
3 3	SUBBC	reg, mem
3 4	SUBC	mem, reg
3 5	SUBBC	mem, reg
3 6*	SUBC	reg, #data16
3 7	SUBBC	reg, #data16
3 8	SUBC	Rwn, [Rwi +] or Rwn, [Rwi] or Rwn, #data3
3 9	SUBBC	Rwn, [Rwi +] or Rwn, [Rwi] or Rwn, #data3

FLAG

Symbol	Description
	N = 1 : Most significant bit of the result is set C = 1 : Carry occurred during operation V = 1 : Arithmetic Overflow occurred during operation Z = 1 : Result equals zero E = 1 : Source operand represents the lowest negative number, either 8000h for word data or 80h for byte data.
"S"	The flag is set according to non-standard rules. Individual instruction pages or the ALU status flags descripion.
"-"	The flag is not affected by the operation
"0"	The flag is cleared by the operation.
"NOR"	The flag contains the logical NORing of the two specified bit operands.
"AND"	The flag contains the logical ANDing of the two specified bit operands.
"OR"	The flag contains the logical ORing of the two specified bit operands.
"XOR"	The flag contains the logical XORing of the two specified bit operands.
"B"	The flag contains the original value of the specified bit operand.
"B"'	The flag contains the complemented value of the specified bit operand

Datasheets

https://www.st.com/resource/en/datasheet/st10f272e.pdf

https://www.st.com/content/ccc/resource/technical/document/programming_manual/20/09/13/1c/cf/32/4b/ce/CD00004609.pdf/files/CD00004609.pdf/jcr:content/translations/en.CD00004609.pdf