Multiple Choice Questions

1. What is the primary role of an Instruction Set Architecture (ISA)?

   (A) To execute machine code
   (B) To define the interface between hardware and software
   (C) To manage memory allocation
   (D) To provide graphical user interfaces
   (E) To control input/output operations
   (F) To encrypt and decrypt data

2. Which of the following is NOT a common ISA architecture?

   (A) Intel x86
   (B) ARM
   (C) RISC-V
   (D) MIPS
   (E) SPARC
   (F) JSON

3. In RISC-V, what is the purpose of the 'jal' instruction?

   (A) To jump and link
   (B) To load a word from memory
   (C) To store a word in memory
   (D) To perform an arithmetic operation
   (E) To compare two registers
   (F) To clear a register

4. What is the size of a 'word' in RISC-V 32-bit architecture?

   (A) 8 bits
   (B) 16 bits
   (C) 32 bits
   (D) 64 bits
   (E) 128 bits
   (F) 256 bits

5. Which register is used as the stack pointer in RISC-V?

   (A) x0
   (B) x1

(C) x2

(D) x3

(E) x4

(F) x5

6. What does the 'addi' instruction do in RISC-V?

   (A) Adds two registers and stores the result in a register

   (B) Adds an immediate value to a register

   (C) Subtracts an immediate value from a register

   (D) Multiplies two registers

   (E) Divides a register by an immediate value

   (F) Compares two immediate values

7. Which addressing mode uses a base register and an offset to calculate the effective address?

   (A) Immediate Addressing

   (B) Direct Addressing

   (C) Indirect Addressing

   (D) Register Addressing

   (E) Base Addressing

   (F) Indexed Addressing

8. In RISC-V, which instruction is used to store a word in memory?

   (A) lw

   (B) sw

   (C) add

   (D) sub

   (E) and

   (F) or

9. What is the purpose of the 'beq' instruction in RISC-V?

   (A) To branch if equal

   (B) To branch if not equal

   (C) To branch if greater than

   (D) To branch if less than

   (E) To branch unconditionally

   (F) To load a byte

10. Which of the following is a characteristic of RISC architectures?

    (A) Complex instruction set
    (B) Variable-length instructions
    (C) Few general-purpose registers
    (D) Load/store architecture
    (E) Extensive use of microcode
    (F) Hardware-based instruction decoding

11. What is the function of the Program Counter (PC) in a CPU?

    (A) To store data temporarily
    (B) To hold the address of the next instruction to execute
    (C) To perform arithmetic operations
    (D) To manage input/output operations
    (E) To decode instructions
    (F) To store the results of computations

12. What does the 'lw' instruction do in RISC-V?

    (A) Loads a word from memory into a register
    (B) Loads a byte from memory into a register
    (C) Stores a word from a register into memory
    (D) Stores a byte from a register into memory
    (E) Loads an immediate value into a register
    (F) Loads a halfword from memory into a register

13. Which register in RISC-V always holds the constant value 0?

    (A) x0
    (B) x1
    (C) x2
    (D) x3
    (E) x4
    (F) x5

14. What is the purpose of the 'sub' instruction in RISC-V?

    (A) To add two registers
    (B) To subtract one register from another
    (C) To multiply two registers
    (D) To divide one register by another

(E) To compare two registers

(F) To load a word from memory

15. In RISC-V, which instruction is used to load a halfword from memory?

    (A) lh

    (B) lw

    (C) lb

    (D) lbu

    (E) sh

    (F) sw

16. What is the function of the 'jalr' instruction in RISC-V?

    (A) To jump and link register

    (B) To load a word from memory

    (C) To store a word in memory

    (D) To perform an arithmetic operation

    (E) To compare two registers

    (F) To clear a register

17. Which of the following is a type of instruction in RISC-V?

    (A) R-Type

    (B) I-Type

    (C) S-Type

    (D) B-Type

    (E) U-Type

    (F) All of the above

18. What does the 'andi' instruction do in RISC-V?

    (A) Performs a bitwise AND operation between a register and an immediate value

    (B) Performs a bitwise OR operation between a register and an immediate value

    (C) Performs a bitwise XOR operation between a register and an immediate value

    (D) Shifts the bits of a register to the left

    (E) Shifts the bits of a register to the right

    (F) Rotates the bits of a register

19. In RISC-V, which instruction is used to store a halfword in memory?

    (A) sh
    (B) sw
    (C) lh
    (D) lw
    (E) lb
    (F) sb

20. What is the purpose of the 'lui' instruction in RISC-V?

    (A) To load an upper immediate value into a register
    (B) To load a lower immediate value into a register
    (C) To load a word from memory into a register
    (D) To store a word from a register into memory
    (E) To perform an arithmetic operation
    (F) To compare two registers

21. Which register in RISC-V is used as the return address register?

    (A) x0
    (B) x1
    (C) x2
    (D) x3
    (E) x4
    (F) x5

22. What does the 'slli' instruction do in RISC-V?

    (A) Shifts the bits of a register to the left by an immediate value
    (B) Shifts the bits of a register to the right by an immediate value
    (C) Rotates the bits of a register
    (D) Performs a bitwise AND operation between two registers
    (E) Performs a bitwise OR operation between two registers
    (F) Performs a bitwise XOR operation between two registers

23. In RISC-V, which instruction is used to load a byte from memory?

    (A) lb
    (B) lbu
    (C) lh
    (D) lw

(E) sh

(F) sw

24. What is the purpose of the 'bne' instruction in RISC-V?

    (A) To branch if equal

    (B) To branch if not equal

    (C) To branch if greater than

    (D) To branch if less than

    (E) To branch unconditionally

    (F) To load a word from memory

25. Which of the following is a characteristic of CISC architectures?

    (A) Simple instruction set

    (B) Fixed-length instructions

    (C) Few general-purpose registers

    (D) Load/store architecture

    (E) Complex instruction set

    (F) Extensive use of microcode

26. Which of the following RISC-V instructions correctly calculates the effective address for an array element A[i], assuming the base address of A is in register `s1` and the index `i` is in register `s2`?

    (A)
    ```
    add t0, s1, s2
    ```

    (B)
    ```
    slli t0, s2, 2
    add t0, t0, s1
    ```

    (C)
    ```
    mul t0, s2, 4
    add t0, t0, s1
    ```

    (D)
    ```
    add t0, s2, s2
    add t0, t0, s1
    ```

    (E)
    ```
    add t0, s2, 4
    add t0, t0, s1
    ```

    (F)
    ```
    slli t0, s2, 3
    add t0, t0, s1
    ```

27. Given the RISC-V assembly code below, what is the value in register `t0` after execution?

    ```
    li t0, 10
    li t1, 3
    div t0, t0, t1
    ```

(A) 0

(B) 1

(C) 3

(D) 3.33

(E) 10

(F) 30

28. Which of the following statements about the RISC-V instruction set is TRUE?

(A) All instructions are 64 bits long.

(B) RISC-V supports both little-endian and big-endian formats natively.

(C) The instruction set is fixed and cannot be extended.

(D) RISC-V allows for custom extensions to the base instruction set.

(E) RISC-V does not support floating-point operations.

(F) RISC-V is only used in academic settings and not in industry.

29. What is the result of executing the following RISC-V code snippet if `a0` initially contains the value 5?

```
addi a0, a0, -2
slli a0, a0, 1
```

(A) 6

(B) 8

(C) 10

(D) 12

(E) 16

(F) 18

30. In RISC-V, what does the following instruction sequence do?

```
lui t0, 0x1000
addi t0, t0, 0x234
```

(A) Loads the value 0x1000234 into `t0`

(B) Loads the value 0x10002340 into `t0`

(C) Loads the value 0x100234 into `t0`

(D) Loads the value 0x1234 into `t0`

(E) Loads the value 0x234 into `t0`

(F) Loads the value 0x1000 into `t0`

31. Consider the following RISC-V loop. What is the purpose of this loop?

```
  addi t0, zero, 0
  addi t1, zero, 10
loop:
  beq t0, t1, end
  addi t0, t0, 1
  j loop
end:
```

(A) It increments `t0` by 10.

(B) It decrements `t0` by 10.

(C) It sets `t0` to 0.

(D) It counts from 0 to 9 in `t0`.

(E) It counts from 1 to 10 in `t0`.

(F) It does nothing.

32. What is the effect of the following RISC-V instruction sequence on the value in register `t0`?

```
  li t0, 0x12345678
  srai t0, t0, 4
```

(A) `t0` becomes 0x1234567

(B) `t0` becomes 0x12345678

(C) `t0` becomes 0x12345679

(D) `t0` becomes 0x12345670

(E) `t0` becomes 0x12345671

(F) `t0` becomes 0x12345672

33. Which of the following RISC-V instructions is used to load a 32-bit value from memory into a register?

(A) `lw`

(B) `lh`

(C) `lb`

(D) `lbu`

(E) `ld`

(F) `sd`

34. What is the purpose of the `jalr` instruction in RISC-V?

(A) To jump to a label

(B) To jump and link to a label

(C) To jump and link to a register

(D) To load a value from memory

(E) To store a value in memory

(F) To perform an arithmetic operation

35. Given the RISC-V assembly code below, what is the value in register `t0` after execution?

```
li t0, 10
li t1, 2
mul t0, t0, t1
```

(A) 10

(B) 20

(C) 30

(D) 40

(E) 50

(F) 60