# ZHENGQI, GAO

Tel: +86-15121152186 | Email: zqgao18@fudan.edu.cn
Homepage: https://zhengqigao.github.io/

## EDUCATION

**Fudan University** Shanghai, China

*M.S. in Microelectronics and Solid State Electronics* Sep 2018 – Jun 2021(Expected)

- GPA: 3.82/4.00 (Rank: NA); worked with Prof. Jun Tao and Prof. Xin Li (Duke Univ.)
- Research interests: electronic design automation (EDA), statistical methods (e.g., Bayesian methods), numerical optimization, and machine learning

*B.E. in Microelectronic Science and Engineering* Sep 2014 – Jun 2018

- GPA: 3.84/4.00 (Rank: 4/71); selected to Elite Engineering Program (top 5%)
- Relevant coursework: Mathematical Analysis, Probability, Mathematical Statistics and Stochastic Process, Signal and System, Data Structure and Algorithm Design, Design of Analog Integrated Circuits

## PUBLICATIONS

1. **Z. Gao**, J. Tao, Y. Su, D. Zhou, X. Zeng and X. Li, "Fast statistical analysis of rare failure events with truncated normal distribution in high-dimensional variation space," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*IEEE TCAD*, under review).
2. **Z. Gao**, Z. Chen, J. Tao, Y. Sun, D. Zhou, and X. Zeng, "Bayesian inference on introduced general region: an efficient parametric yield estimation method for integrated circuits," *ACM/IEEE Asia and South Pacific Design Automation Conference* (*ASPDAC*), Jan. 2021.
3. **Z. Gao**, J. Tao, D. Zhou, X. Zeng and X. Li, "Efficient rare failure analysis over multiple corners via correlated Bayesian inference," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*IEEE TCAD*), Oct. 2020. [PDF] [Code]
4. **Z. Gao**, J. Tao, D. Zhou and X. Zeng, "Efficient parametric yield estimation over multiple process corners via Bayesian inference based on Bernoulli distribution," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*IEEE TCAD*), Oct. 2020. [PDF] [Code]
5. J. Shi, **Z. Gao**, J. Tao, Y. Su, D. Zhou and X. Zeng, "Multi-corner parametric yield estimation via Bayesian inference on Bernoulli distribution with conjugate prior," *IEEE International Symposium on Circuits and Systems* (*ISCAS*), Oct. 2020. [PDF]
6. Y. Li, X. Zeng, **Z. Gao**, L. Lin, J. Tao, J. Han, X. Cheng, M. Tahoori and X. Zeng, "Exploring a Bayesian optimization framework compatible with digital standard flow for soft-error-tolerant circuit," *IEEE/ACM Design Automation Conference* (*DAC*), Jul. 2020. [PDF]
7. **Z. Gao**, J. Tao, Y. Su, D. Zhou and X. Zeng, "Projection based active Gaussian process regression for Pareto Front modeling," *Arxiv Preprint*. [PDF]
8. **Z. Gao**, J. Tao, F. Yang, Y. Su, D. Zhou and X. Zeng, "Efficient performance trade-off modeling for analog circuit based on Bayesian neural network," *IEEE/ACM International Conference on Computer Aided Design* (*ICCAD*), Nov. 2019. [PDF]
9. J. Tao, **Z. Gao**, D. Zhou and X. Zeng, "Efficient statistical analysis for correlated rare failure events," *IEEE International Conference on Solid-State and Integrated Circuit Technology* (*ICSICT*), Nov. 2018. [PDF]

## RESEARCH EXPERIENCE

**Southern Methodist University** Remotely

*Research Assistant to Prof. Ron Rohrer (a preeminent EDA researcher)* May 2020 – Present

- Built a power grid DC simulator for the electromigration problem
- Analyzed parametric yield based on the adjoint method

**Fudan University (State Key Laboratory of ASIC & System)** Shanghai, China

*Research Assistant to Prof. Jun Tao (in collaboration with Prof. Xin Li)* Sep 2016 – Present

- Exploited a graph neural network for graph similarity tasks
- Improved post-silicon yield estimation with the domain adaptation technique (published in *ASPDAC*'21)
- Estimated multi-corner failure rate and yield with Bayesian inference (both published in *IEEE TCAD*)

- Modeled performance trade-off of analog circuits based on a Bayesian neural network (published in *ICCAD*'19)
- Optimized a time variant analog filter by hierarchical clustering (bachelor thesis)
- Developed an SRAM failure-rate estimation tool in collaboration with Prof. Xuan Zhang (WUSTL) [see here]

## TEACHING AND INTERNSHIPS

**Fudan University (FDU) and Duke Kunshan University (DKU)** China
*Teaching Assistant* Sep 2019 – Mar 2020

- Performed TA duties for Design of Analog Integrated Circuits at FDU (instructor: Prof. Jun Xu) and Introduction to Programming & Data Structure at DKU (instructor: Prof. Dennis Quan [Duke Univ.])

**Baidu Inc.** Shanghai, China
*Quality Assurance (QA) Engineering Intern* Jun 2017 – Sep 2017

- Measured the robustness of programs and took charge of the FEEDS project

## SELECTED AWARDS AND HONORS

- National Scholarship, Fudan University (top 1%) 2020
- Rising Star of Academic, Fudan University (awarded to 11 graduate students majoring in Sci. & Engi.) 2020
- Pacemaker to Merit Student, Fudan University (awarded to 15 graduate students) 2019
- First Prize Scholarship, Fudan University (top 5%) 2019
- National Gold Award, China "Internet+" College Student Innovation & Entrepreneur Competition(top 5%) 2018
- National 2nd Prize, China Post-Graduate Mathematical Contest in Modeling (top 15%) 2018
- Outstanding Undergraduates of Shanghai (top 5%) 2018
- Meritorious Winner, American Mathematical Contest in Modeling (top 13%) 2017
- Top 11%, 2017 IEEE Xtreme Global Programming Competition (out of 3,350 teams worldwide) 2017
- First Prize Scholarship, Fudan University (top 5%) 2015, 2016, 2017
- National 2nd prize, China Mathematical Contest in Modeling (top 15%) 2016

## REPRESENTATIVE PROJECTS

***PRML* Solution Manual (GitHub 500+ Stars)** Shanghai, China
*An Original Solution Manual for Pattern Recognition and Machine Learning (PRML)* Sep 2017 – Present

- Solved nearly all exercises in *PRML* [see here]
- Communicated with people globally via email, helping them solve problems relevant to *PRML*

**Auto-Grading System** Kunshan, China
*An Auto-Grading System Developed at DKU* Jan 2020 – Mar 2020

- Led a small TA group to peruse the source code of Submitty
- Developed a fully automatic grading system based on Submitty

**"Dr. Stanley's House" (Puzzle Video Game) Written in Haskell** Shanghai, China
*Final Project for Introduction to Functional Programming: From C/C++ to Haskell* Sep 2018 – Jan 2019

- Implemented the game with a complete plot via Haskell [see here]
- Organized the program structure, sorted the logic, and set the schedule as the team leader
- Exploited Haskell libraries (e.g., SDL2, SDL2-ttf, and SDL2-mixer) to add music and animation

**Real-Time Temperature Monitoring System Design** Shanghai, China
*Final Project for Electronic System Design* Mar 2017 – Jun 2017

- Designed and created a double bridge circuit on PCB for temperature signal amplification and filtering
- Programmed STC single-chip microcomputer to sample and quantize temperature signal
- Designed host computer application using MATLAB to monitor and visualize temperature record

## ADDITIONAL INFORMATION

**Computer and Language Skills**

- **Programming languages & Software**: C/C++, MATLAB, Python, Linux, Java, Haskell, HSPICE, SPECTRE
- **Languages**: Mandarin Chinese (native), English (proficient, TOEFL: 104 [Speaking: 23], GRE: 330+3.5)

**Academic Service**

- Independent reviewer for *IEEE TCAD*