ID	Item	Sub item 1	Sub item 2	Test sequence	Pass condition
1	Register access	TCR Register	Reset value check	After reset is released, perform read access to TCR Register (offset= 0x0).	Read value = 32'h0000_0100
2			R/W access	1.Write 0000_0000 & read back and compare 2. Write FFFF_FFFF & readback & compare 3.Write 5555_5555 & readback & compare 4.Write AAAA_AAAA & readback & compare 5.Write 0000_0500 & readback & compare	Read value = 32'h0000_0000 Read value = 32'h0000_0000 Read value = 32'h0000_0501 Read value = 32'h0000_0501 Read value = 32'h0000_0500
3		TDR0 Register	Reset value check	After system reset is released, perform read access to TDR0 (offset= 0x4).	Read value = 32'h0000_0000
4			R/W access	1.Write 0000_0000 & read back and compare 2.Write FFFF_FFFF & readback & compare 3.Write 5555_5555 & readback & compare 4.Write AAAA_AAAA & readback & compare 5.Write 3333_3333 & readback & compare	read value is same as write value
5		TDR1 Register	Reset value check	After reset is released, perform read access to TDR1 (offset= 0x8).	Read value = 32'h0000_0000
6			R/W access	1.Write 0000_0000 & read back and compare 2. Write FFFF_FFFF & readback & compare 3.Write 5555_5555 & readback & compare 4.Write AAAA_AAAA & readback & compare 5.Write 3333_3333 & readback & compare	read value is same as write value
7		TCMP0 Register	Reset value check	After reset is released, perform read access to TCMP0 (offset= 0xC).	Read value = 32'hFFFF_FFFF
8			R/W access	1.Write 0000_0000 & read back and compare 2. Write FFFF_FFFF & readback & compare 3.Write 5555_5555 & readback & compare 4.Write AAAA_AAAA & readback & compare 5.Write 3333_333a & readback & compare	read value is same as write value
9		TCMP1 Register	Reset value check	After reset is released, perform read access to TCMP1 (offset= 0x10).	Read value = 32'hFFFF_FFFF
10			R/W access	1.Write 0000_0000 & read back and compare 2. Write FFFF_FFFF & readback & compare 3.Write 5555_5555 & readback & compare 4.Write AAAA_AAAA & readback & compare 5.Write 3333_3333 & readback & compare	read value is same as write value
11		TIER Register	Reset value check	After reset is released, perform read access to TIER (offset= 0x14).	Read value = 32'h0000_0000
12			R/W access	1.Write 0000_0000 & read back and compare 2. Write FFFF_FFFF & readback & compare 3.Write 5555_5555 & readback & compare 4.Write AAAA_AAAA & readback & compare 5.Write 3333_3333 & readback & compare	Read value = 32'h0000_0000 Read value = 32'h0000_0001 Read value = 32'h0000_0001 Read value = 32'h0000_0000 Read value = 32'h0000_0001
13		TISR Register	Reset value check	After reset is released, perform read access to TISR (offset= 0x18).	Read value = 32'h0000_0000
14			R/W access	1.Write 0000_0000 & read back and compare 2. Write FFFF_FFFF & readback & compare 3.Write 5555_5555 & readback & compare 4.Write AAAA_AAAA & readback & compare 5.Write 3333_3333 & readback & compare	Read value = 32'h0000_0000 Read value = 32'h0000_0000 Read value = 32'h0000_0000 Read value = 32'h0000_0000 Read value = 32'h0000_0000
15		THCSR Register	Reset value check	After reset is released, perform read access to THCSR (offset= 0x1C).	Read value = 32'h0000_0000
16			R/W access	1.Write 0000_0000 & read back and compare 2. Write FFFF_FFFF & readback & compare 3.Write 5555_5555 & readback & compare 4.Write AAAA_AAAA & readback & compare 5.Write 3333_3333 & readback & compare	Read value = 32'h0000_0000 Read value = 32'h0000_0001 Read value = 32'h0000_0001 Read value = 32'h0000_0000 Read value = 32'h0000_0001
9	Reserved access	1. Address at 12'h015 2. Address at 12'aaa 3. Address at 12'h567 4. Address at 12'h111 5. Address at 12'hfff	R/W reserved	1.Write 0000_1234 & read back and compare 2. Write FFFF_FFFF & readback & compare 3.Write 5555_5555 & readback & compare 4.Write AAAA_AAAA & readback & compare 5.Write 0000_0050 & readback & compare	Read value = 32'h0000_0000 Read value = 32'h0000_0000 Read value = 32'h0000_0000 Read value = 32'h0000_0000 Read value = 32'h0000_0000
10	One-hot check			1.Write 1111_1813 to TCR Register 2.Write 3333_3333 to TDR0 Register 3.Write AAAA_AAAA to TDR1 Register 4.Write FFFF_FFFF to TCMP0 Register 5.Write 5555_5555 to TCMP1 Register 6.Write 0101_1010 to TIER Register 7.Write 0505_0505 to TISR Register 8.Write FFFF_FFFF to THCSR Register 9.Read TCR Register and compare 10.Read TDR0 Register and compare 11.Read TDR1 Register and compare 12.Read TCMP0 Register and compare 13.Read TCMP1 Register and compare 14.Read TIER Register and compare 15.Read TISR Register and compare 16.Read THCSR Register and compare	Read value_TCR= 32'h0000_0803 Read value_TDR0 = 32'h3333_3333 Read value_TDR1 = 32'hAAAA_AAAA Read value_TCMP0 = 32'hFFFF_FFFF Read value_TCMP1 = 32'h5555_5555 Read value_TIER = 32'h0000_0000 Read value_TISR = 32'h0000_0000 Read value_THCSR = 32'h0000_0001
11	Check byte access	TCR check	Write access byte 0	1. Write pstrb = 4'b0001 2. Write 0000_0802 to TCR Register & read and compare	Read value_TCR= 32'h0000_0102
12			Write access byte 1	1. Write pstrb = 4'b0010 2. Write 0000_0503 to TCR Register & read and compare	Read value_TCR= 32'h0000_0502
13			Write access byte 2	1. Write pstrb = 4'b0100 2. Write 0000_0503 to TCR Register & read and compare	Read value_TCR= 32'h0000_0502
14			Write access byte 3	1. Write pstrb = 4'b1000 2. Write 0000_0803 to TCR Register & read and compare	Read value_TCR= 32'h0000_0502
15		TDR0 check	Write access byte 0	1. Write pstrb = 4'b0001 2. Write 0000_0802 to TDR0 Register & read and compare	Read value_TDR0= 32'h0000_0002

16			Write access byte 1	1. Write pstrb = 4'b0010 2. Write 0000_0503 to TDR0 Register & read and compare	Read value_TDR0= 32'h0000_0502
17			Write access byte 2	1. Write pstrb = 4'b0100 2. Write ffff_ffff to TDR0 Register & read and compare	Read value_TDR0= 32'h00ff_0502
18			Write access byte 3	1. Write pstrb = 4'b1000 2. Write aaaa_0803 to TDR0 Register & read and compare	Read value_TDR0= 32'haaff_0502
19		TDR1 check	Write access byte 0	1. Write pstrb = 4'b0001 2. Write 0000_0802 to TDR1 Register & read and compare	Read value_TDR1= 32'h0000_0002
20			Write access byte 1	1. Write pstrb = 4'b0010 2. Write 0000_0503 to TDR1 Register & read and compare	Read value_TDR1= 32'h0000_0502
21			Write access byte 2	1. Write pstrb = 4'b0100 2. Write ffff_ffff to TDR1 Register & read and compare	Read value_TDR1= 32'h00ff_0502
22			Write access byte 3	1. Write pstrb = 4'b1000 2. Write aaaa_0803 to TDR1 Register & read and compare	Read value_TDR1= 32'haaff_0502
23		TCMP0 check	Write access byte 0	1. Write pstrb = 4'b0001 2. Write 1111_1111 to TCMP0 Register & read and compare	Read value_TCMP0= 32'hffff_ff11
24			Write access byte 1	1. Write pstrb = 4'b0010 2. Write ffff_ffff to TCMP0 Register & read and compare	Read value_TCMP0= 32'hffff_ff11
25			Write access byte 2	1. Write pstrb = 4'b0100 2. Write aaaa_aaaa to TCMP0 Register & read and compare	Read value_TCMP0= 32'hffaa_ff11
26			Write access byte 3	1. Write pstrb = 4'b1000 2. Write 0505_0505 to TCMP0 Register & read and compare	Read value_TCMP0= 32'h05aa_ff11
27		TCMP1 check	Write access byte 0	1. Write pstrb = 4'b0001 2. Write 1111_1111 to TCMP1 Register & read and compare	Read value_TCMP1= 32'hffff_ff11
28			Write access byte 1	1. Write pstrb = 4'b0010 2. Write ffff_ffff to TCMP1 Register & read and compare	Read value_TCMP1= 32'hffff_ff11
29			Write access byte 2	1. Write pstrb = 4'b0100 2. Write aaaa_aaaa to TCMP1 Register & read and compare	Read value_TCMP1= 32'hffaa_ff11
30			Write access byte 3	1. Write pstrb = 4'b1000 2. Write 0505_0505 to TCMP1 Register & read and compare	Read value_TCMP1= 32'h05aa_ff11
31		TIER check	Write access byte 0	1. Write pstrb = 4'b0001 2. Write 1111_1111 to TIER Register & read and compare	Read value_TIER= 32'h0000_0001
32			Write access byte 1	1. Write pstrb = 4'b0010 2. Write ffff_ffff to TIER Register & read and compare	Read value_TIER= 32'h0000_0001
33			Write access byte 2	1. Write pstrb = 4'b0100 2. Write aaaa_aaaa to TIER Register & read and compare	Read value_TIER= 32'h0000_0001
34			Write access byte 3	1. Write pstrb = 4'b1000 2. Write 0505_0505 to TIER Register & read and compare	Read value_TIER= 32'h0000_0001
35		TISR check	Write access byte 0	1. Write pstrb = 4'b0001 2. Write 1111_1111 to TISR Register & read and compare	Read value_TISR= 32'h0000_0000
36			Write access byte 1	1. Write pstrb = 4'b0010 2. Write ffff_ffff to TISR Register & read and compare	Read value_TISR= 32'h0000_0000
37			Write access byte 2	1. Write pstrb = 4'b0100 2. Write aaaa_aaaa to TISR Register & read and compare	Read value_TISR= 32'h0000_0000
38			Write access byte 3	1. Write pstrb = 4'b1000 2. Write 0505_0505 to TISR Register & read and compare	Read value_TISR= 32'h0000_0000
39		THCSR check	Write access byte 0	1. Write pstrb = 4'b0001 2. Write 1111_1111 to THCSR Register & read and compare	Read value_THCSR= 32'h0000_0001
40			Write access byte 1	1. Write pstrb = 4'b0010 2. Write ffff_ffff to THCSR Register & read and compare	Read value_THCSR= 32'h0000_0001
41			Write access byte 2	1. Write pstrb = 4'b0100 2. Write aaaa_aaaa to THCSR Register & read and compare	Read value_THCSR= 32'h0000_0001
42			Write access byte 3	1. Write pstrb = 4'b1000 2. Write 0505_0505 to THCSR Register & read and compare	Read value_THCSR= 32'h0000_0001
43	Check_ABP_Multi_access	TDR0 & TDR1	R/W access	1.Write 3333_3333 to TDR0 Register 2.Write 5555_5555 to TDR1 Register 3.Read TDR0 Register and compare 4.Read TDR1 Register and compare	Read value_TDR0= 32'h3333_3333 Read value_TDR1= 32'h5555_5555
44	Check_ABP_Pready	TCR	R/W access	1.Read at TCR Register & Compare pready signal	check signal = 1'b1
45		TDR0 & TDR1	R/W access	1.Write 0000_0003 to TDR0 Register & Compare pready signal 2.Read at TDR1 Register & Compare pready signal	check signal = 1'b1 check signal = 1'b1
46		TCMP0 & TCMP1	R/W access	1.Write 0000_0002 to TCMP0 Register & Compare pready signal 2.Read at TCMP1 Register & Compare pready signal	check signal = 1'b1 check signal = 1'b1
47	Check_ABP_Protocol	TDR0	R/W access	1. Write FFFF_FFFF & readback & compare 2. Write 5555_5555 without Psel & readback & compare 3. Write 3333_3333 without Pneable & readback & compare 4.Read at TDR0 Register	Read value= 32'hFFFF_FFFF Read value= 32'h0000_0000 Read value= 32'h0000_0000 Read value= 32'hFFFF_FFFF

48	Check_ABP_Pslverr	TCR	R/W access	1. TCR = 32'h0000_0100 2. div_val = i, (i = 9 ; i<16 ; i = i+1) & readback & Compare pslverr signal	tim_pslverr = 1'b1 tim_pslverr = 1'b1 tim_pslverr = 1'b1 tim_pslverr = 1'b1 tim_pslverr = 1'b1 tim_pslverr = 1'b1 tim_pslverr = 1'b1 tim_pslverr = 1'b1
49			R/W access	1.Write 0000_0102 to TCR Register 2.Write 0000_0103 to TCR Register 3.Write 0000_0903 to TCR Register & readback & compare pslverr signal 4.Write 0000_0102 to TCR Register	tim_pslverr = 1'b1
50			R/W access	1. Write 0000_0003 to TCR Register 2. div_val = i, (i = 1 ; i<9 ; i = i+1) & readback & Compare pslverr signal 3.Write 0000_0002 to TCR Register	tim_pslverr = 1'b1 tim_pslverr = 1'b1 tim_pslverr = 1'b1 tim_pslverr = 1'b1 tim_pslverr = 1'b1 tim_pslverr = 1'b1 tim_pslverr = 1'b1 tim_pslverr = 1'b1
51			R/W access	1. Write 0000_0003 to TCR Register 2. div_val = i, (i = 9 ; i<16 ; i = i+1) & readback & Compare pslverr signal	tim_pslverr = 1'b1 tim_pslverr = 1'b1 tim_pslverr = 1'b1 tim_pslverr = 1'b1 tim_pslverr = 1'b1 tim_pslverr = 1'b1 tim_pslverr = 1'b1 tim_pslverr = 1'b1
52	Check_ABP_Unaligned	TDR0	R/W access	1. Write aaaa_aaaa to TDR0 Register & read and compare	Read value_TDR0= 32'haaaa_aaaa
53		12'h005	R/W access	1. Write aaaa_aaaa to addr 12'h005 & read and compare 2.Read at TDR0 Register & read and compare	Read value = 32'h0000_0000 Read value_TDR0= 32'haaaa_aaaa
54		12'h006	R/W access	1. Write 3333_5555 to addr 12'h006 & read and compare 2.Read at TDR0 Register & read and compare	Read value = 32'h0000_0000 Read value_TDR0= 32'haaaa_aaaa
55		12'h007	R/W access	1. Write 2222_2222 to addr 12'h007 & read and compare 2.Read at TDR0 Register & read and compare	Read value = 32'h0000_0000 Read value_TDR0= 32'haaaa_aaaa
56	Check_counter_counting	TDR0 & TDR1	R/W access	1. Write ffff_fff0 to TDR0 Register 2. Write ffff_ffff to TDR1 Register 3. Write 0000_0001 to TCR Register 4. wait 15 cycles & read and compare 5. Write 0000_0000 to TCR Register	Read value_counter= 64'hffff_ffff_ffff_ffff
57		TDR0 & TDR1	R/W access	1. Write ffff_fff0 to TDR0 Register 2. Write ffff_ffff to TDR1 Register 3. Write 0000_0003 to TCR Register 4. wait 15 cycles & read and compare 5. Write 0000_0002 to TCR Register	Read value_counter= 64'hffff_ffff_ffff_ffff
58		TDR0 & TDR1	R/W access	1. Write ffff_fff0 to TDR0 Register 2. Write ffff_ffff to TDR1 Register 3. Write 0000_0003 to TCR Register 4.(i=1 ; i<9 ; i=i+1) 5. wait (((1 << i))*15 -1) cycles & read and compare 6. Write 0000_0002 to TCR Register	Read value_counter= 64'hffff_ffff_ffff_ffff Read value_counter= 64'hffff_ffff_ffff_ffff Read value_counter= 64'hffff_ffff_ffff_ffff Read value_counter= 64'hffff_ffff_ffff_ffff Read value_counter= 64'hffff_ffff_ffff_ffff Read value_counter= 64'hffff_ffff_ffff_ffff Read value_counter= 64'hffff_ffff_ffff_ffff Read value_counter= 64'hffff_ffff_ffff_ffff
59		TDR0 & TDR1	R/W access	1. Write ffff_ffff to TDR0 Register 2. Write ffff_ffff to TDR1 Register 3. Write 0000_0003 to TCR Register 4. (i=1 ; i<9 ; i=i+1) 5. wait (2**i -1) cycles & read and compare 6. Write 0000_0002 to TCR Register	Read value_counter= 64'h0000_0000_0000_0000 Read value_counter= 64'h0000_0000_0000_0000 Read value_counter= 64'h0000_0000_0000_0000 Read value_counter= 64'h0000_0000_0000_0000 Read value_counter= 64'h0000_0000_0000_0000 Read value_counter= 64'h0000_0000_0000_0000 Read value_counter= 64'h0000_0000_0000_0000 Read value_counter= 64'h0000_0000_0000_0000
60	Check_cnt_ctrl	TCR	Check_timer_count	1.Write 0000_0001 to TCR Register 2. data_before = counter_64bit 3. (n =0 ; n <9; n = n+1) 4. Wait (2 **n) cycles 5. data_after = counter_64bit 6. Compare data_after vs data_before	data_after = data_before + 1
61	Cnt_halt_check	THCSR	R/W access	1.Write 0 to debug_mode 2.Write 0000_0001 to THCSR Register 3.Write 0000_0001 to TCR Register 4.Read and Compare THCSR[0] signal 5.Read and Compare THCSR[1] signal 6.Wait 5 cycles 7.data_before = counter_64bit 8.Wait 1 cycles 9.data_after = counter_64bit 10. Compare data_after vs data_before 11.Write 0000_0000 to THCSR Register 12.Write 0000_0000 to TCR Register	Read value_THCSR= 32'h0000_0001 Read value_THCSR= 32'h0000_0001 data_after = data_before + 1

62		THCSR	R/W access	1.Write 0000_0303 to TCR Register 2.Write 1 to debug_mode 3.Write 0000_0001 to THCSR Register 4.Read and Compare THCSR[0] signal 5.Read and Compare THCSR[1] signal 6.Wait 25 cycles 7.data_before = counter_64bit 8.Wait 20 cycles 9.data_after = counter_64bit 10. Compare data_after vs data_before 11.Write 0 to debug_mode 12.Write 0000_0000 to THCSR Register 13.Wait ((2*3) -1) cycles 14.data_after = counter_64bit 15. Compare data_after vs data_before	Read value_THCSR= 32'h0000_0003 Read value_THCSR= 32'h0000_0003 data_after = data_before data_after = data_before + 1
63	Interrupt_check	TISR	R/W access	1.Write ffff_ffff to TDR0 Register 2.Write ffff_ffff to TDR1 Register 3.Write 0000_0001 to TIER Register 4.Write 0000_0001 to TCR Register 6.Wait 5 cycles 7.Read & compare tim_int signal 8.Wait 5 cycles 9.Write 0000_0000 to TIER Register 10.Read & compare TISR[0] signal 11.Wait 5 cycles 12.data_before = counter_64bit 13.Wait 1 cycles 14.data_after = counter_64bit 15. Compare data_after vs data_before 16.Write 0000_0001 to TISR Register 17.Read & compare TISR[0] signal	tim_int = 1 Read value_TISR= 32'h0000_0001 data_after = data_before + 1 Read value_TISR= 32'h0000_0000